Trapping and Detrapping Mechanisms in β-Ga_2O_3 Vertical FinFETs Investigated by Electro-Optical Measurements

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***Abstract*— We present a detailed investigation of the trapping and detrapping mechanisms that take place in the gate region of β-Ga_2O_3 vertical finFETs and describe the related processes. This analysis is based on combined pulsed characterization, transient measurements, and tests carried out under monochromatic light, with photon energies between 1.5 and 5 eV. The original results presented in this article demonstrate that: (i) when submitted to positive gate stress with $V_{GS} > 3$ V, the devices show a significant threshold voltage variation; (ii) this effect is not recoverable in 10 000 s in rest condition (zero bias, dark condition). (iii) V_{TH} can quickly recover its initial value when the device is illuminated with UV-C light at 280 nm. (iv) Stress-recovery experiments carried out at different photon energies allowed us to estimate the threshold energy for the release of carriers from the Al_2O_3/Ga_2O_3 interface, and for the injection of electrons from metal to the Al_2O_3 insulator (conduction band discontinuity at the metal/Al_2O_3 interface).**

***Index Terms*— FinFET, Ga_2O_3, gate stability, trapping, vertical transistor.**

I. Introduction

β-Ga_2O_3 is an attractive material to be used in power electronics applications due to its ultrawide bandgap (~4.6–4.9 eV [1]–[4]) and its critical electric field, around ~8 MV/cm, significantly higher than that of GaN (~3.4 MV/cm) or SiC (~3.3 MV/cm) [5].

In the last years, devices based on β-Ga_2O_3 with high breakdown voltage and high current were demonstrated [6]–[10], thus paving the way for the successful development of this technology. To fabricate β-Ga_2O_3 transistors, the lateral configuration has been initially considered. Several device structures have been evaluated in this direction, including the standard MOSFET [11], [12], the gate-recessed or trench-MOSFET [13], the nanomembrane FET [14], and the FinFET [15]. For many material systems (including Si, SiC, and, more recently, GaN), it was demonstrated that passing from a lateral to a vertical device configuration can be beneficial in terms of breakdown voltage, dynamic performance, and reliability. Following this trend, vertical gallium oxide transistors have recently been proposed based on a planar structure with vertical aperture [16] and on the vertical FinFET or trench-MOSFET topology [17], [18]. The latter structure consists of a vertical power metal–insulator FETs, having the schematic structure represented in Fig. 1, and using an Al_2O_3/β-Ga_2O_3 heterojunction as a gate-stack. This topology is particularly interesting; recent studies demonstrated for the first time normally-OFF Ga_2O_3 transistor with a breakdown voltage over 1 kV [6], and the first multi-fin Ga_2O_3 transistor, with the highest power figure-of-merit [19].

Despite the great potential of this topology, these vertical Ga_2O_3 FinFETs show a positive shift in the threshold voltage with positive gate swings [19]; therefore, the stability of these FinFETs needs to be investigated in detail. In addition, the threshold energies for detrapping electrons from the Al_2O_3/β-Ga_2O_3 heterojunction and the band discontinuity between metal and insulator have not been described in detail.

The aim of this article is to fill this gap, by presenting a comprehensive study of the threshold instabilities in β-Ga_2O_3 vertical FinFETs. The analysis was carried out by pulsed and transient measurements. The results indicate the following.

1) The devices show a significant positive shift of the threshold voltage, which is not recoverable with zero

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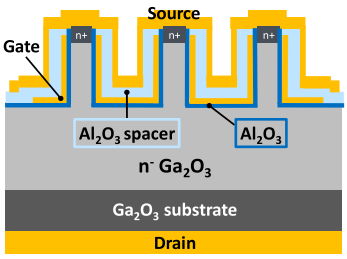

Fig. 1. Schematic of the Ga_2O_3 vertical FinFET under test [19].

bias applied in dark condition and is ascribed to the trapping of electrons at the Al_2O_3/β-Ga_2O_3 interface.

2) UV (280 nm) light can significantly accelerate the detrapping, thus leading to a substantial recovery.
3) Moreover, the study of the trapping and detrapping phenomena under the gate allowed to obtain an experimental estimation of threshold energy for detrapping electrons from the Al_2O_3/β-Ga_2O_3 heterojunction (2.2 eV) and the band discontinuity between metal and insulator (3.5 eV). The latter was found to be in good agreement with results reported in previous reports [20], [21].

II. Experimental Details

The schematic of the devices under test is shown in Fig. 1. The tested devices are Ga_2O_3 vertical FinFETs, in which 10 μm of n^--Ga_2O_3 are grown by hydride vapor phase epitaxy (HVPE) on an n-type (001) Ga_2O_3 substrate. The multi-fin structures are then fabricated, by shaping the FET channel via dry etching; the height of the fin is 1.39 μm, and samples with widths in the range from 100 to 400 nm were fabricated. A 35-nm Al_2O_3 layer is then deposited by atomic layer deposition (ALD). The source contact (Ti/Al/Pt) is deposited on a 400-nm-layer of n^+-Ga_2O_3, obtained through ion implantation, by using Si as a donor. Ti is widely used as ohmic contact metal due to the low workfunction and excellent adhesion property, Al is as an interlayer for better conductivity, and Pt is used as a capping layer for probing and prevention of oxidation of Al. A 50-nm Cr gate metal is then deposited via sputtering. Cr is used due to the excellent adhesion and because it can be easily dry etched. Finally, the drain consists of Ti/Au contact, in which Au is for prevention of oxidation and for probing. Different stacks for source and drain contacts were chosen because the source contact is also a part of the source-connected field plate (FP). Since source-connected FP needs to conformally cover the fin channels, the metal stack is deposited by sputtering. As a result, Pt is used as the top noble metal layer instead of Au, which is not available in the sputtering system. Moreover, the devices have 10-μm FP structures outside the gate edges that allow to significantly increase the breakdown voltage [7]. The analyzed FinFETs have multiple fin fingers in a 50 μm $\times$ 50 μm active area. More information about the device structure and fabrication process can be found in [19].

III. Gate Stability

The threshold stability was analyzed combining pulsed I_D–V_{GS} measurements and threshold voltage transient measurements. The results indicated that significant trapping mechanisms take place in the gate region, as described in detail in the following.

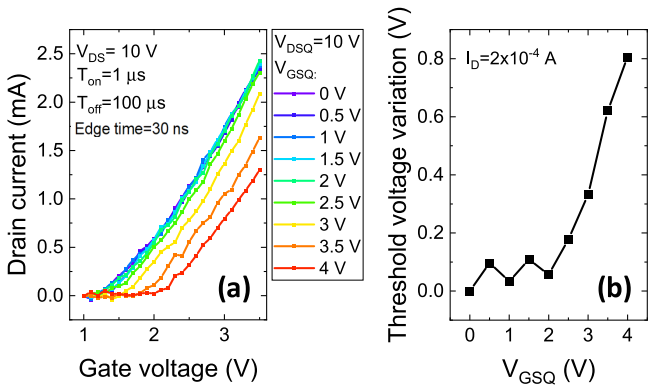

Fig. 2. (a) Pulsed I_D–V_{GS} measurements performed for different quiescent bias points (V_{GSQ} is increased by 0.5 V starting from 0 up to 4 V, whereas V_{DSQ} is maintained at 10 V) in multi-fin Ga_2O_3 transistor with a fin width of 200 nm. (b) Threshold voltage variation as a function of V_{GSQ} extracted at $I_D = 2 \times 10^{-4}$ A.

A. Pulsed Measurements

Pulsed measurements allow to investigate the dynamic response of the devices and the possible presence of traps. The measurement procedure is as follows [22].

1) *Trapping Phase:* The device is kept in a trapping condition [quiescent bias point (V_{GSQ}, V_{DSQ})], capable of inducing a significant charge trapping. To investigate the trapping processes induced by a positive gate bias, we increased V_{GSQ} by 0.5 V from 0 up to 4 V.
2) *Measurement Phase:* After this trapping phase, the device is turned on quickly, and the I_D–V_{GS} characteristics are measured with short (1 μs) pulses. Such timing is reasonable since it is representative for power devices to be operated in the 100 kHz–1 MHz range.

The results of the pulsed characterization are reported in Fig. 2(a). In the pulsed measurements, very short (1 μs) pulses are used, and this sets a limit to the current resolution of the system; for this reason, the threshold voltage is calculated as the gate voltage corresponding to a drain current $I_D = 2 \times 10^{-4}$ A. As can be noticed [see also Fig. 2(b)], the threshold voltage is stable up to a trapping voltage equal to $V_{GSQ} = 2$ V and then increases for increasing V_{GSQ}. These results indicate the presence of a trapping mechanism in the gate region that strongly affects the performance of the devices. In Fig. 3, we schematically report the band diagram of the FinFET [20], [21], [23]–[25]; the cross section of the drain side cut normal to the channel is shown. The threshold voltage shift is ascribed to the trapping of electrons to interface/border traps located at the Al_2O_3/Ga_2O_3 interface, consistently with previous reports on silicon and GaN transistors [26]–[30]. The impact of fixed charge and the interfacial charge in Ga_2O_3 vertical FinFETs was deeply investigated in [31]; Hu *et al.* [31] analyzed and extracted the fixed charge density at the interface Al_2O_3/Ga_2O_3, concluding that this charge causes the electric field in the gate oxide to point in the opposite direction

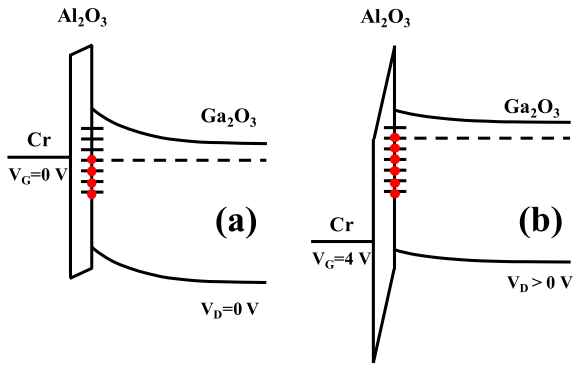

Fig. 3. Schematic of the trapping mechanism responsible for the threshold voltage variation observed during the pulsed I_D–V_{GS} measurements. (a) Band diagram at the equilibrium. (b) Band diagram with a positive gate bias (corresponding to the trapping phase of pulsed I_D–V_{GS} measurements).

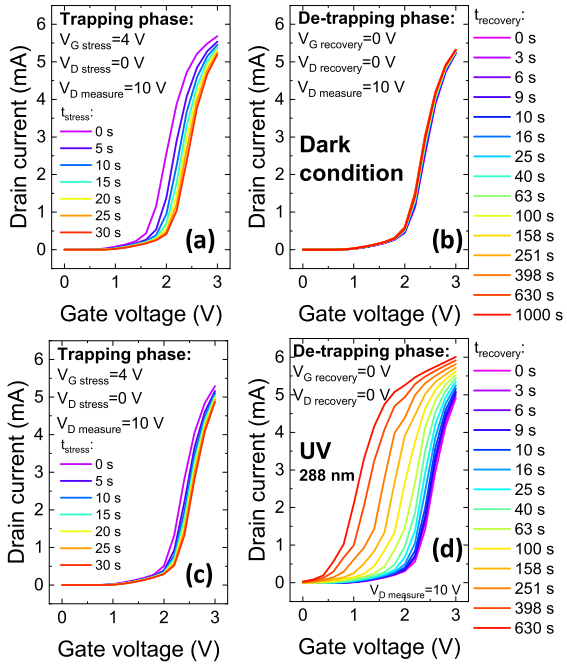

Fig. 4. (a) and (c) Fast I_D–V_{GS} characterizations performed during the trapping phase ($V_G = 4$ V and $V_D = 0$ V) carried out in the dark condition. (b) and (d) Fast I_D–V_{GS} characterizations performed during the detrapping phase ($V_G = 0$ V and $V_D = 0$ V) in the dark condition and under UV light, respectively.

from that in the channel, as shown in Fig. 3. It is worth noticing that the observed V_{TH} variation is less than 1 V and is comparable to what observed in other wide bandgap semiconductors [29], [32].

B. Transients Measurements

To understand whether the positive shift of the threshold voltage observed during the pulsed measurements is permanent or recoverable, threshold voltage transient characterization was carried out.

This characterization consists in monitoring the threshold voltage during two phases, namely, the trapping phase and the detrapping phase, by means of fast I_D–V_{GS} measurements.

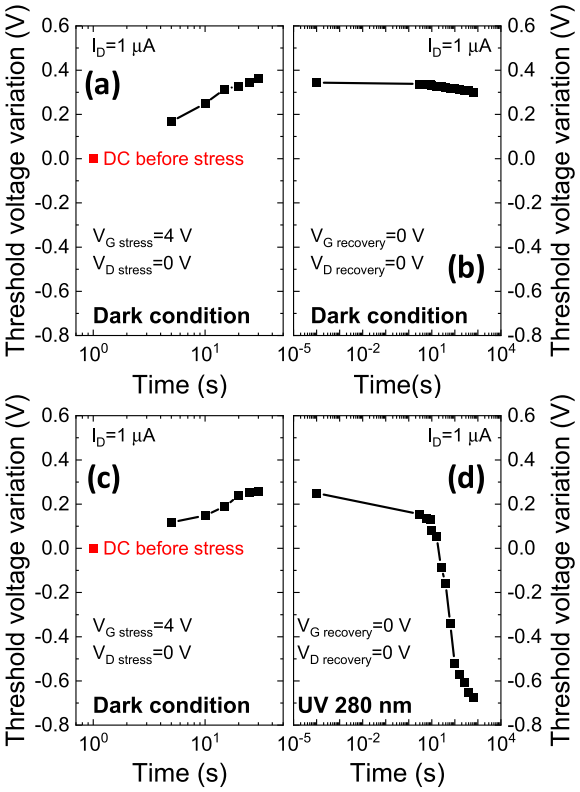

Fig. 5. Threshold voltage variation during (a) and (c) stress phase and (b) and (d) recovery phase, extracted by analyzing the measurements reported in Fig. 4 at a drain current equal to 1 μA.

During the trapping phase, a stress condition (with $V_G = 4$ V and $V_D = 0$ V) was maintained for 30 s to favor trapping, and fast I_D–V_{GS} characterization was periodically carried out, to monitor the time dependence of the V_{TH} variation. After the stress was induced, the detrapping kinetics was analyzed, by keeping the gate and the drain terminal at zero bias for 10 000 s while performing periodic fast I_D–V_{GS} characterization. The results of the transient measurements are reported in Fig. 4(a) and (b), which show the I_D–V_{GS} curves during the two phases, and in Fig. 5(a) and (b), which show the corresponding threshold voltage variations extracted at $I_D = 1$ μA. As can be noticed, the stress condition causes a positive shift of the threshold voltage, which does not recover within the second phase in dark.

To induce a recovery in the threshold voltage, the same measurement was repeated by executing the recovery phase under UV light on the very same device. It is worth noticing that during the trapping phase [see Fig. 4(c)], the initial value of the threshold voltage is higher than on the fresh device [see Fig. 4(a)]; this is due to the fact that the trapping induced in dark was not recoverable [see Fig. 4(a) and (b)]. By illuminating the device with a UV LED with a wavelength of 280 nm during the second phase (with an optical power equal to 100 μW), the threshold was found to significantly recover [see Figs. 4(c) and (d) and 5(c) and (d)], demonstrating that light can promote the release of the electrons trapped at the Al_2O_3/Ga_2O_3 interface (see Fig. 3). As can be observed, the exposure to UV light leads to an overcompensation of

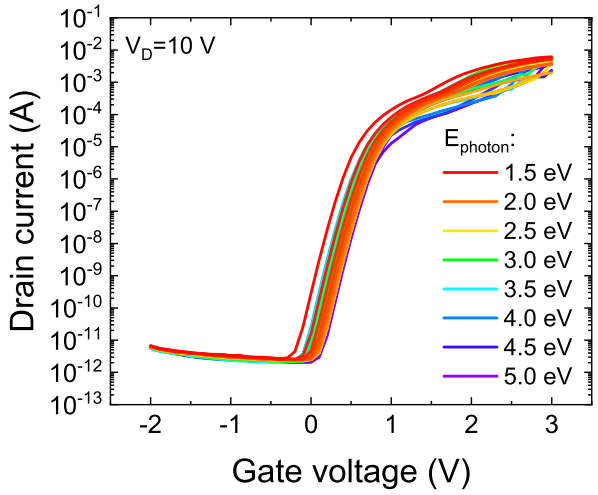

Fig. 6. I_D–V_{GS} characterizations carried out under monochromatic light. The gate voltage is increased from −2 up to 3 V, the drain is maintained at 10 V, and E_{ph} is increased by 0.1 eV starting from 1.5 up to 5 eV.

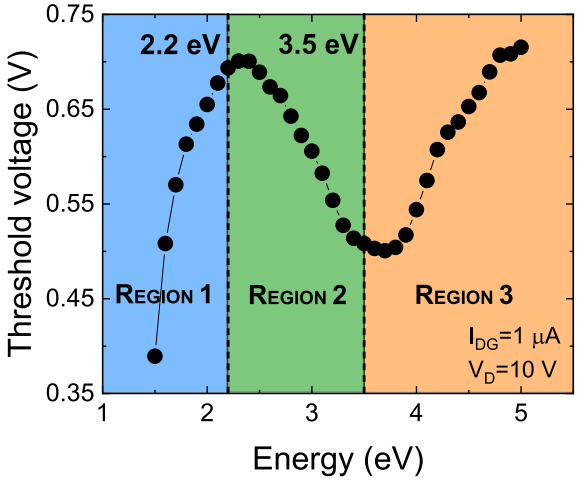

Fig. 7. Threshold voltage shift as a function of E_{ph} extracted from the I_D–V_{GS} measurements carried out with monochromatic light, at a drain current equal to 1 μA.

the threshold voltage; 280-nm photons favor the detrapping of both the electrons trapped during stress and pre-existing electrons trapped deeper (in energy and/or spatially) in the gate insulator.

IV. Study of the Trapping/Detrapping Processes

To further investigate the trapping/detrapping phenomena occurring under the gate, we carried out I_D–V_{GS} measurements and drain-to-gate current transient measurements under monochromatic light. We analyzed the effect of light in a wide range of photon energies E_{ph} (i.e., from 1.5 up to 5 eV with a step of 0.1 eV), by using a Xe-lamp and a monochromator. Fig. 6 shows the results of repeated transfer characteristics measured (with gate voltages between −2 and 3 V and a drain voltage of 10 V) in dark condition, after 5 min under monochromatic light at zero bias condition. By analyzing the corresponding threshold voltage variation extracted at I_D = 1 μA, three different regions can be identified (see Fig. 7); for

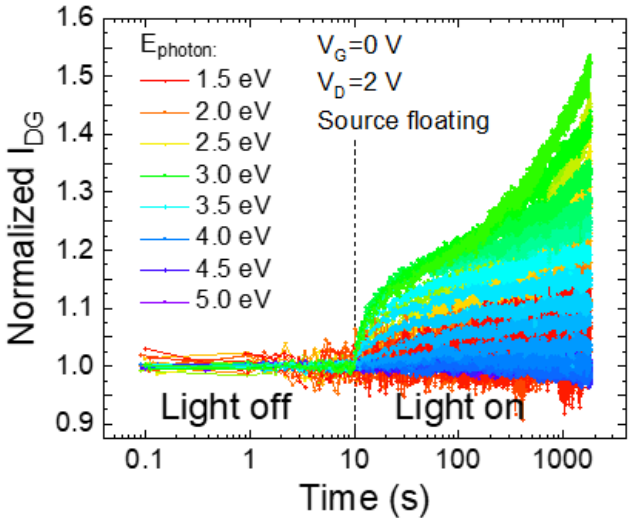

Fig. 8. Drain-to-gate current transient measurements performed with V_D = 2 V, V_G = 0 V and with the source floating under monochromatic light. The measurements are normalized with respect to the value of the drain currents in dark condition for each photon energy.

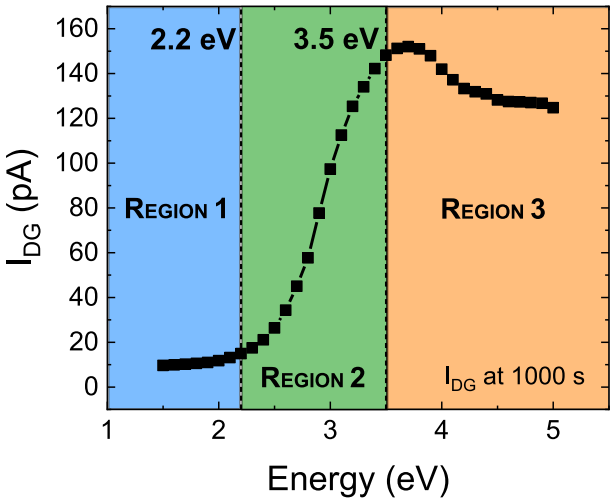

Fig. 9. Drain-to-gate current variation as a function of E_{ph}. I_{DG} is extracted starting from the transient measurements, at the instant t = 1000 s.

E_{ph} lower than 2.2 eV, a positive shift in the threshold voltage is observed (region 1). As discussed in the following, in this case, photon energy is lower than a "threshold" energy, and the positive V_{TH} shift is ascribed to the effect of cumulative I_D–V_{GS} measurements repeated several times, due to the trapping process described in Fig. 3. For E_{ph} between 2.2 and 3.5 eV, the threshold voltage shows a negative shift (region 2), indicating a release of the trapped electrons. Finally, for E_{ph} higher than 3.5 eV, we can observe a positive shift again (region 3).

To better describe the physical origin of the trapping process, we carried out light-induced current transient measurements; this measurement is similar to internal photoemission spectroscopy (IPS), in which light is applied to a sample to induce the transition of a mobile carrier from one material/interface to a positively biased terminal, and the

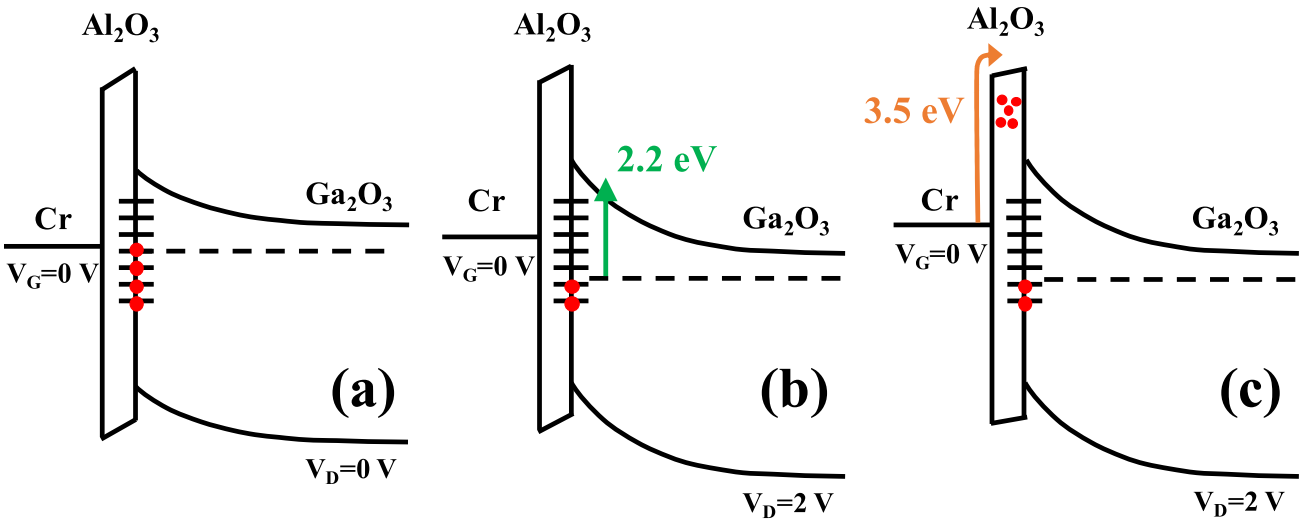

Fig. 10. Schematic of the trapping mechanisms at the Al_2O_3/β-Ga_2O_3 and Cr/Al_2O_3 heterointerfaces. The band diagram represents the device region near the bottom of the fin channel. (a) Band diagram at the equilibrium corresponds to region 1 and shows the pre-existing electrons trapped at the oxide–semiconductor interface. (b) Band diagram with a positive V_{DG} (corresponding to current transient measurement condition) corresponds to region 2 and shows the detrapping of electrons from the oxide–semiconductor interface. (c) Band diagram with a positive V_{DG} (corresponding to current transient measurement condition) corresponds to region 3 and shows the injection of electron from the metal in the insulator. As a consequence of the trapped electrons, the band of the Al_2O_3 bends further upward, resulting in a shift of V_{TH}.

corresponding current is measured [33]. This measurement technique allows to investigate changes in the drain–gate leakage induced by exposure to monochromatic light and can be used to evaluate the threshold energy for detrapping electrons from deep states at the Ga_2O_3/Al_2O_3 interface and for injecting electrons from the metal to the Al_2O_3 (band discontinuity).

The measurement is carried out as follows: the device is biased with a gate voltage $V_G = 0$ V, and $V_D = 2$ V while continuously monitoring the gate leakage. After 10 s in dark, monochromatic light is turned on, and the corresponding leakage transient is recorded for 1800 s. The measurement is repeated at increasing photon energies, from 1.5 to 5 eV. The results obtained through this technique are reported in Fig. 8.

In Fig. 9, we report the relative variation of drain–gate leakage (I_{DG}) induced by light with increasing photon energies. Once again, we can identify three regions, with 2.2 and 3.5 eV as boundaries. I_{DG} does not change with photon energies lower than 2.2 eV (region 1); such energy is not sufficient to transfer electrons across the Al_2O_3 insulator or to extract carriers from deep traps at the Ga_2O_3/Al_2O_3 interface. For higher photon energies (>2.2 eV, region 2), drain–gate leakage significantly increases with light exposure, indicating that photons have enough energy to favor detrapping from the oxide–semiconductor interface. After being detrapped, these electrons are swept toward the drain ($V_D = 2$ V), thus increasing the current. Finally, (region 3) for E_{ph} higher than 3.5 eV, a slight decrease in the drain current is observed.

An explanation of the trapping and detrapping mechanisms observed during the measurements and for this light-dependent leakage variation is given in the following and is schematically shown in Fig. 10.

The devices under test are characterized by a not negligible density of dielectric/semiconductor interface states, as already discussed in [19] [see Fig. 10(a)]. The density of electrons at this interface can vary during the repeated I_D–V_{GS} sweeps in dark (up to 3 V), which may induce a small trapping, due to the change of the position of the Fermi level during the measurement itself. This is consistent with the results in Fig. 2, showing that a voltage higher than 2 V can induce a threshold shift. As a consequence, the threshold shifts in Fig. 7 (region 1) can be ascribed to the measurement-induced trapping of electrons at the Al_2O_3/Ga_2O_3 interface (see Fig. 3). Since light with photon energy $E_{ph} < 2.2$ eV does not have enough energy to induce a significant leakage or a significant detrapping from interface states [see Fig. 9 (region 1)], in this photon energy range trapping prevails, and electrons are accumulated at the Al_2O_3/Ga_2O_3 interface causing a positive shift in V_{TH}. These electrons begin to be detrapped from the oxide–semiconductor interface for $E_{ph} > 2.2$ eV, as suggested by the negative shift of V_{TH} (region 2 in Fig. 7). In the IPS measurement, after being detrapped, these electrons are swept toward the (positively biased) drain, thus generating an increase in the photogenerated current (see Figs. 8 and 9) and schematically shown in Fig. 10(b).

Finally (region 3), for $E_{ph} > 3.5$ eV, the electrons from the metal can be injected in the insulator, toward the positively biased drain [see Fig. 10(c)]. Electrons injected toward the insulator may be partly trapped at oxide traps, thus resulting in a slight positive V_{TH} shift [see Fig. 7 (region 3)]. Trapped electrons have a repulsive action, which slows the injection from the Cr metal to the insulator. As a consequence, for higher energies, photo-induced current shows a slight decrease (see Fig. 9). Changes and singularities in the absorption characteristics of Al_2O_3 and Ga_2O_3 may also contribute to the drop in current observed above 3.5 eV [34]. According to this interpretation, the onset of this last process corresponds to the 3.5 eV conduction band discontinuity between Cr and Al_2O_3.

This value is consistent with theoretical predictions based on the properties of metals [20] and high-k oxides [21].

V. Conclusion

In this article, we reported an extensive analysis of the trapping mechanisms that affect the gate stability of Ga_2O_3 vertical FinFETs. The results discussed in this article indicate that the devices under test show a significant positive shift in the threshold voltage when submitted to a $V_G > 3$ V. The threshold voltage does not recover to the value before stress within a long recovery phase with zero bias applied in dark condition, but it recovers when the transistor is illuminated with UV light. To quantitatively evaluate the properties of the traps involved in this phenomenon, the variation of the threshold voltage, as well as the variation of the light-stimulated drain-to-gate leakage, were studied as a function of the photon energy, in a wide range of E_{ph}. By analyzing the dependence of V_{TH} and I_{DG} on E_{ph}, a clear relation between the trapping and detrapping phenomena occurring in the oxide was described. In addition, we estimated the threshold energy for detrapping from deep interface traps ($E_C-2.2$ eV), as well as the conduction band discontinuity between Cr and Al_2O_3 (3.5 eV).

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