Guiding Principles for Trench Schottky Barrier Diodes Based on Ultrawide Bandgap Semiconductors: A Case Study in Ga_2O_3

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***Abstract*— Ultrawide bandgap (UWBG) semiconductors such as β-Ga_2O_3 can support a much higher electric field than traditional wide bandgap semiconductors, thus promising an unprecedentedly low conduction loss. However, the maximum electric field in regular Schottky barrier diodes (SBDs) is limited due to the constraint set by the reverse leakage current. On the other hand, a trench SBD structure allows for a much higher electric field to be sustained thanks to the reduced surface field (RESURF) effect. In this article, the guiding principles for trench SBDs are investigated through a case study in Ga_2O_3. The advantages of trench SBDs are discussed both by quantitative analysis of the ON-state voltage drop (V_{ON}), as well as by a review of the state-of-the-art Ga_2O_3 device performance. It is found that for kilovolt-class operation, the trench SBD structure is not only preferred but arguably necessary for high-efficiency Ga_2O_3 rectifiers. In addition, the effects of fin/trench geometry on the specific ON-resistance and the electric-field profile are investigated. A design flow oriented toward device performance targets is presented, together with an example design of a 1375-V Ga_2O_3 trench SBD, showing that a V_{ON} (defined at 100 A/cm^2) of below 1 V can be obtained. These results highlight the importance in harnessing the high breakdown field of UWBG semiconductors through trench SBDs for efficient power rectifiers, and provide valuable insights into the device design and optimization.**

***Index Terms*— Ga_2O_3, power semiconductor devices, Schottky diodes, trench-MOS.**

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I. Introduction

ULTRAWIDE bandgap (UWBG) semiconductor materials inherently possess very high breakdown electric fields, resulting in very high projected Baliga's figure-of-merits (BFOMs) even beyond the values of traditional wide bandgap semiconductors such as 4H-SiC and GaN [1]. A high BFOM is equivalent to a low conduction loss at the same voltage rating, thus is highly preferable for efficient power devices. A prime example is β-Ga_2O_3, which has a breakdown or critical electric field (E_c) of ~8 MV/cm due to its bandgap of 4.5–4.7 eV [2]. In addition, β-Ga_2O_3 has other highly desirable attributes, including the existence of shallow donors as well as the availability of melt-grown substrates [3]. The former enables efficient and controllable n-type doping from mid-10^{15} cm^{-3} to beyond 10^{18} cm^{-3} [4], while the later allows for a potentially low-cost device platform [5].

To extract the full potential of UWBG semiconductors in power devices, it is important to reach a high electric field close to E_c. BFOM captures the tradeoff between the breakdown voltage (BV) and the specific ON-resistance ($R_{ON,sp}$)

$$\text{BFOM} = \frac{\text{BV}^2}{R_{\text{ON,sp}}} = \frac{\varepsilon_s \mu_n E_c^3}{4} \quad \text{or} \quad \frac{\varepsilon_s \mu_n E_{\max}^3}{4} \tag{1}$$

where ε_s is the dielectric constant and μ_n the electron mobility. Without reaching E_c at the BV of the device, E_c in the original definition of BFOM needs to be replaced by the maximum parallel-plane electric field (E_{max}) achievable in the device at breakdown, thus the effective BFOM will be lowered and the conduction loss increased.

Schottky barrier diodes (SBDs) are high-efficiency rectifiers due to a typically lower ON-state voltage drop (V_{ON}) than p-n diodes and no storage of minority carriers. But, it is also generally associated with a higher reverse leakage current density (J_R) through the Schottky barrier. As a result, the rated BV is determined by the maximum allowable reverse leakage current ($J_{R,max}$), rather than avalanche breakdown. The leakage current can be reduced by increasing the Schottky barrier height ($q\phi_B$), but this will result in an unfavorable increase of V_{ON} due to the increase in the built-in potential (V_{bi}), which roughly is equal to ϕ_B.

Without increasing the Schottky barrier height, J_R can only be controlled by limiting the electric field near the Schottky

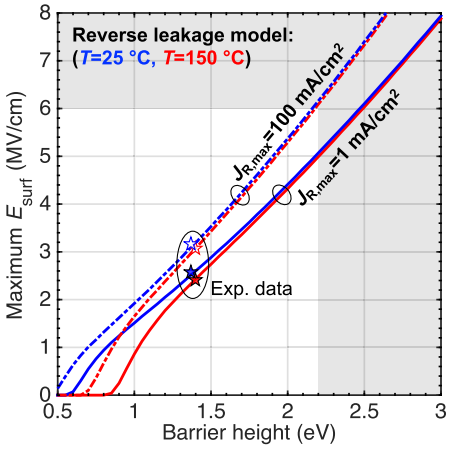

Fig. 1. Calculated maximum surface electric field (E_{surf}) as a function of the barrier height in regular β-Ga_2O_3 SBDs, under maximum reverse leakage current density ($J_{R,max}$) of 1 mA/cm^2 and 100 mA/cm^2. Adapted with permission from Li *et al.* [6] © 2020 AIP Publishing LLC.

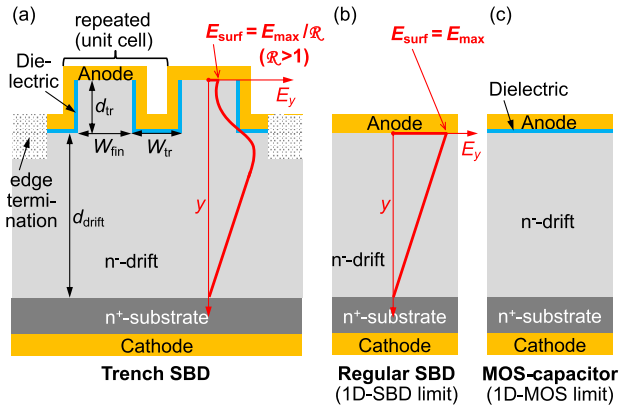

Fig. 2. Schematic cross section of (a) trench-MOS SBD, (b) regular SBD, and (c) MOS-capacitor. The regular SBD and the MOS-capacitor are the 1-D limits of the trench SBD with $d_{tr} \to 0$ and $W_{fin} \to 0$, respectively. To illustrate RESURF, the electric-field profile along a vertical cutline (E_y) at the center of the fin channel in the trench SBD is schematically plotted and compared with that in the regular SBD.

contact surface, or the surface electric field (E_{surf}). We have previously calculated the maximum E_{surf} allowable in regular Ga_2O_3 SBDs at fixed $J_{R,max}$ values [6], as shown in Fig. 1. It can be seen that under $q\phi_B = 1.1$ eV, E_{surf} is only $\sim$1.8 MV/cm at room temperature under $J_{R,max} = 1$ mA/cm^2, which is a common current density for specifying the BV in power SBDs. Unfortunately, due to the 1-D nature of the electric-field profile in a regular SBD, the maximum electric field in the drift region happens to be at the surface, as shown in Fig. 2(b). Consequently, E_{surf} should be used in (1) in place of E_{max} for regular SBDs. Clearly, due to the constraint of the leakage current as well as the 1-D nature, the effective BFOM in regular SBDs will be much lower than the projected limit of UWBG semiconductors.

To alleviate the constraint due to the leakage current, it is important to decouple J_R from E_{max}. This means that the maximum electric field should not be located at the Schottky contact surface, but deeper within the device body. This is only possible with a 2-D or 3-D electric-field profile, as in the case of a junction-barrier-Schottky diode (JBSD). JBSDs are also often referred to as merged p-n Schottky (MPS) diodes. As this name suggests, a JBSD can be viewed as a regular SBD with additional p-type regions inserted under the Schottky contact surface, forming p-n junctions not only vertically, but also laterally. It is the charge-coupling effect due to the lateral p-n junctions that reduced the E_{surf} near the Schottky contact interface, such that E_{max} is located away from the surface. In this way, J_R can be successfully decoupled from E_{max}, allowing for a higher E_{max} and thus a higher BFOM, without sacrificing V_{ON}. Although the original concept of reduced surface effect (RESURF) is not identical to the scenario in JBSDs [7], the underlying charge-coupling mechanism is identical, thus we are also using this terminology for JBSDs and the like.

Due to the difficulty in native p-type doping [8], it is challenging to realize JBSDs in Ga_2O_3. Another challenge associated with traditional JBSDs is the realization of high-quality lateral p-n junctions. For example, this is still an unsolved problem today for GaN, thus trench JBSDs have been proposed and demonstrated [9]. On the other hand, the p-n junctions in JBSDs can be replaced with MOS-structures while preserving the RESURF effect. Such a structure is called a trench-MOS barrier Schottky (TMBS) rectifier or a trench SBD in short, as schematically shown in Fig. 2(a). Trench SBDs have been successfully realized in Si [10], 4H-SiC [11], and GaN [12]. For UWBG semiconductors like Ga_2O_3, due to the large difference between the maximum E_{surf} and E_c, it is even more important to utilize the RESURF effect for efficient rectifiers, thus trench SBDs are highly preferable to regular SBDs, especially for medium-to-high voltage applications, as will be discussed in detail in later sections. Furthermore, trench SBDs have an additional advantage over JBSDs due to a smaller sidewall-depletion width in the fin channels at ON-state. This is because the built-in potential in a MOS structure can be made much smaller than that of p-n junctions, especially in UWBG semiconductors. As will be discussed later, a small sidewall-depletion width will benefit the $R_{ON,sp}$.

In this article, we first present a model in Section II to analyze the ON-state voltage drop in trench SBDs and illustrate its advantage over regular SBDs, by using Ga_2O_3 as an example. Then, we review in Section III the advancements of state-of-the-art Ga_2O_3 trench SBDs. In Sections IV and V, we discuss the impact of fin/trench geometry on $R_{ON,sp}$ and the electric-field profile, serving as guidelines for design optimization. Lastly, we show in Section VI a design flow oriented toward device performance targets, as well as a design example of a kilovolt-class high-efficiency Ga_2O_3 trench SBD with its performance compared against a regular SBD counterpart.

II. Advantage in V_{ON}

To quantitatively reveal the benefits of the RESURF effect in trench SBDs, we analyze its ON-state voltage drop (V_{ON}). In general, under a certain ON-current density (J_{ON}), V_{ON} in

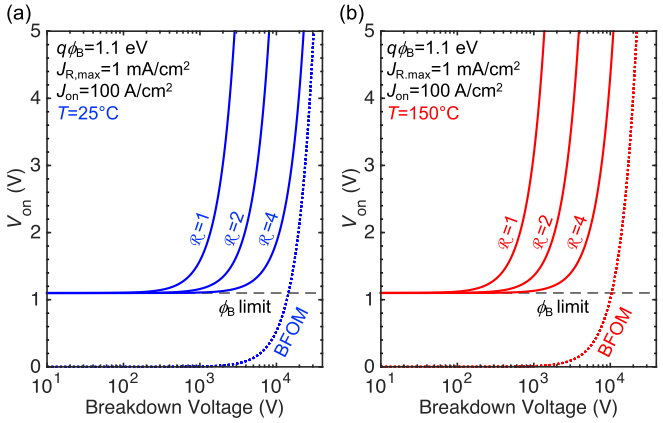

Fig. 3. Calculated V_{ON} at an ON-current density of 100 A/cm^2 in Ga_2O_3 trench SBDs at (a) 25 °C and (b) 150 °C, using (3). The barrier height is fixed at 1.1 eV and the RESURF factor ($\mathcal{R}$) is varied from 1 to 4. The BV is defined at $J_{R,max}$ = 1 mA/cm^2. The calculated BFOM limits considering E_c = 8 MV/cm are 18.8 GW/cm^2 at 25 °C and 9.9 GW/cm^2 at 150 °C, representing the V_{ON} limits due to differential $R_{ON,sp}$ only.

a SBD can be expressed by

$$V_{ON} = V_{bi} + J_{ON} \cdot R_{ON,sp} \tag{2}$$

where $R_{ON,sp}$ here is the *differential* specific ON-resistance at ON-state. For simplicity, we approximate V_{bi} with ϕ_B. In a single-sided abrupt junction as in the case of a regular SBD, $R_{ON,sp}$ is near-optimized under a non-punch-through condition at the BV, the same condition under which BFOM was derived. In a trench SBD, the surface electric field (E_{surf}) is reduced by a factor of $\mathcal{R}$ with respect to the maximum electric field (E_{max}) in the drift region due to RESURF, i.e., $E_{surf} = E_{max}/\mathcal{R}$. Here, $\mathcal{R}$ is referred to as the RESURF factor. It follows that $\mathcal{R} > 1$ in a trench SBD, as illustrated in Fig. 2(a), whereas $\mathcal{R} = 1$ in a regular SBD [Fig. 2(b)] or a MOS capacitor [Fig. 2(c)]. Assuming that the additional ON-resistance due to the fin/trench RESURF structures can be neglected, i.e., the $R_{ON,sp}$ of the trench SBD is dominated by the drift region resistance, we have using (2)

$$V_{ON} \approx \phi_B + J_{ON} \cdot \frac{4BV^2}{\varepsilon_s \mu_n \mathcal{R}^3 E_{surf}^3}. \tag{3}$$

With $\mathcal{R} > 1$, V_{ON} is reduced through the reduction of $R_{ON,sp}$.

In a given material, the maximum allowable E_{surf} under a given $J_{R,max}$ is primarily a function of the barrier height and temperature (T) [6]. In the case of β-Ga_2O_3, under $q\phi_B$ = 1.1 eV and $J_{R,max}$ = 1 mA/cm^2, E_{surf} is calculated to be 1.78 MV/cm at 25 °C and 1.36 MV/cm at 150 °C by a numerical reverse leakage model, which considered both barrier tunneling and thermionic emission under the influence of image-force lowering [6], as shown in Fig. 1. For the electron mobility in β-Ga_2O_3, we adopt a drift mobility value of 166 cm^2/V·s at 25 °C and 87 cm^2/V·s at 150 °C according to the temperature-dependent Hall mobility model and the calculated Hall factor of ~1.5 in [13]. The dependence on doping concentration is neglected for simplicity. ε_s in Ga_2O_3 is taken to be 10 ε_0 [14], where ε_0 is the vacuum permittivity.

Using the aforementioned values and assumptions, V_{ON} in Ga_2O_3 trench SBDs is calculated as a function of BV at J_{ON} = 100 A/cm^2, as shown in Fig. 3. It can be seen that at a relatively low BV below 100 V, V_{ON} is dominated by the built-in potential (~ϕ_B). As BV increases, V_{ON} begins to increase due to the contribution from the differential $R_{ON,sp}$. The RESURF effect in trench SBDs "delays" the increase of V_{ON} due to the reduction of $R_{ON,sp}$ as a result of $\mathcal{R}$ [see (3)]. It can be seen that a RESURF factor of ~4 is necessary to maintain a low V_{ON} for a BV of 1 kV and above. Of course, with a higher barrier height, the requirement on the RESURF factor can be relaxed, but that comes at a cost of an increase in V_{bi}. Thus, it can be concluded that for kilovolt-class Ga_2O_3 rectifiers that focus on high efficiency, i.e., low V_{ON}, it is extremely beneficial to use the trench-SBD structure.

The necessity of RESURF effect in Ga_2O_3 SBDs can be understood from another aspect. In 4H-SiC SBDs, the drift mobility is roughly five times higher than that of Ga_2O_3. With the same barrier height, the maximum E_{surf} is similar due to the similar effective mass in these two materials. This means that the differential $R_{ON,sp}$ in regular Ga_2O_3 SBDs will be 5× higher than 4H-SiC SBDs. As a result, Ga_2O_3 SBDs need to be operated at ~5 times lower J_{ON} to get the same V_{ON} as 4H-SiC SBDs, which translates to a 5× larger chip size for the same current rating. On the other hand, as will be shown in Section VI, trench SBDs could allow for a 30× reduction in the differential $R_{ON,sp}$, which more than offsets the 5× difference in mobility. Clearly, to compete favorably with high-voltage 4H-SiC SBDs in performance, trench SBDs are therefore, the preferred choice over regular SBDs in the case of Ga_2O_3.

III. Advancements of β-Ga_2O_3 Trench SBDs

The first demonstration of Ga_2O_3 trench SBDs is by Sasaki *et al.* [15]. The devices were fabricated on a (001) epitaxial wafer grown by halide vapor phase epitaxy (HVPE) on a single-crystal Ga_2O_3 substrate. As shown in Fig. 4(a), the thickness and the net doping concentration of the epitaxial layer is 7 μm and 6×10^{16} cm^{-3}, respectively. Fig. 4(b) shows the optical top-view image of the fabricated trench SBDs. The trench SBD shows similar forward current–voltage (I–V) characteristics with the regular SBD, as shown in Fig. 4(c). The slightly higher turn-on voltage of the trench SBD is attributed to the potential barrier due to the MOS structure at the fin sidewalls. The slightly higher differential $R_{ON,sp}$ is due to the restriction of the current path due to the fin/trench structures. The reverse I–V characteristics of the tench SBDs is shown in Fig. 4(d). In comparison with the regular SBDs, J_R is significantly reduced, leading to a higher BV (~240 V). This serves as a clear proof of concept for the presence of RESURF effect in trench SBDs. The same group reported the first characterization of the switching performance of their Ga_2O_3 trench SBDs [16]. As expected, due to the unipolar nature, Ga_2O_3 trench SBDs show much superior reverse recovery characteristics than Si fast recovery diodes, and are comparable with SiC SBDs.

By adopting an epitaxial layer with lower doping concentration and increased thickness (10 μm), we demonstrated

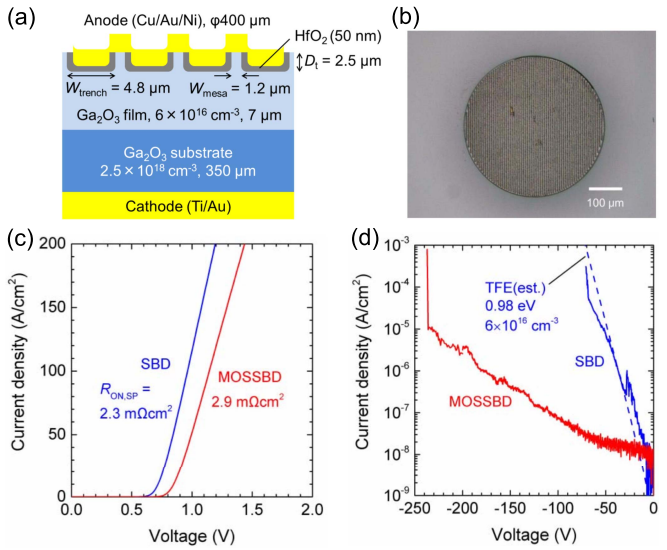

Fig. 4. (a) Schematic cross section of the Ga_2O_3 trench SBDs. (b) Optical image of the Ga_2O_3 trench SBDs. (c) Forward *I*–*V* and (d) reverse *I*–*V* characteristics of the Ga_2O_3 trench SBDs in comparison with the regular SBDs. Reprinted from Sasaki *et al.* [15] © 2017 IEEE.

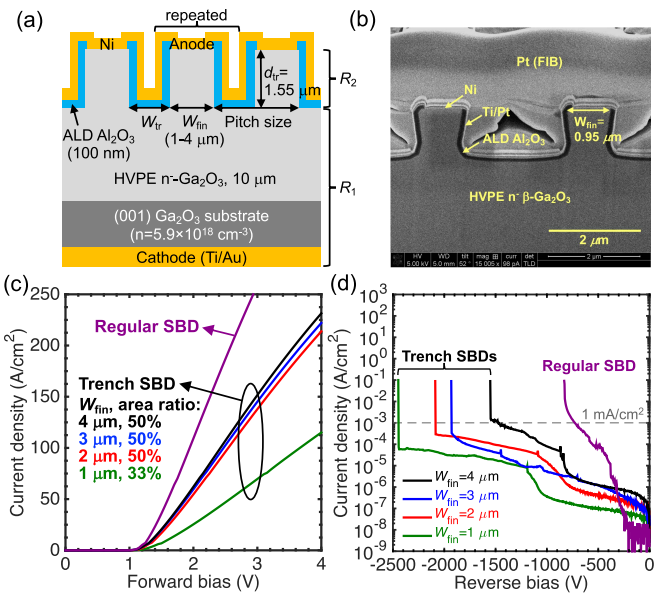

Fig. 5. (a) Schematic cross section of our third-generation Ga_2O_3 trench SBDs. (b) SEM cross-sectional image of the Ga_2O_3 trench SBDs with $W_{fin} = 1$ μm. (c) Forward *I*–*V* and (d) reverse *I*–*V* characteristics of the third-generation Ga_2O_3 trench SBDs in comparison with the regular SBDs. Adapted from Li *et al.* [19] © 2018 IEEE.

the first trench Ga_2O_3 SBD with a BV of 1.5 kV [17]. However, the ON-current was low as a result of a very low doping concentration of $1-2 \times 10^{15}$ cm^{-3}. With a higher doping concentration of 2×10^{16} cm^{-3}, we obtained a much improved ON-current in our second-generation devices, while still achieving a BV of 1230 V [18]. Although the turn-on voltage is similar, the differential $R_{ON,sp}$ of the trench SBDs is $\sim$15 m$\Omega \cdot$ cm^2, much higher than the value of 6.6 m$\Omega \cdot$ cm^2 in regular SBDs fabricated on the same wafer. We found that the higher $R_{ON,sp}$ is partially due to the charge trapping effects at the fin sidewall interface. The trench SBDs exhibit an ultralow J_R of <1 μA/cm^2 before breakdown due to the RESURF effect, which also results in a much higher BV than the cofabricated regular SBDs, which show a BV of 730 V [18].

With improved device designs and fabrication process, the BV was further improved to over 2 kV in our third-generation Ga_2O_3 trench SBDs [19]. To reduce the resistance of the fin channels, we reduced the trench depth (d_{tr}) from our previous design of 2 μm to 1.55 μm, as shown in Fig. 5(a). To mitigate the previously observed sidewall trapping effects, wet acid treatments in HCl and HF was performed to reduce the dry etch induced damage and improve the smoothness of the fin sidewall. Fig. 5(b) shows the cross-sectional image of the fin/trench structure taken by scanning electron microscope (SEM). As a result of the acid treatments, the sidewall appears to be smoother than our second-generation devices [18].

Fig. 5(c) shows the forward *I*–*V* characteristics of the third-generation trench SBDs with different fin-channel widths (W_{fin}) and fin area ratios (ARs). AR is defined as the ratio of the fin-channel width (W_{fin}) to the pitch size, which is a sum of the trench width (W_{tr}) and W_{fin} [see Fig. 5(a)]. While the trench SBDs have a higher differential $R_{ON,sp}$ than the regular SBDs, the $R_{ON,sp}$ is similar for devices with an identical AR. This is an indication that the sidewall depletion due to the charge trapping effects is insignificant, as will be discussed further in Section IV. In comparison with the second-generation devices, the third-generation trench SBDs have a smaller $R_{ON,sp}$ of 11.3 m$\Omega \cdot$ cm^2, as a result of the reduced d_{tr} and improved sidewall interface quality.

Fig. 5(d) shows the reverse *I*–*V* characteristics of the third-generation trench SBDs with different W_{fin}. The impact of the fin width on the RESURF effect was revealed: with a smaller W_{fin}, J_R is smaller, indicating a more pronounced RESURF effect. In addition, the hard BV increases with decreasing W_{fin}. Through TCAD simulations, we identified that the breakdown in devices with $W_{fin} \geq 2$ μm is due to the electric-field crowding near the trench bottom corners, which is more pronounced with increasing W_{fin}. In devices with $W_{fin} = 1$ μm, the BV is limited by the edge termination [20]. Combining the BV and $R_{ON,sp}$ results, the third-generation trench SBDs with $W_{fin} = 2$ μm showed a highest BFOM of 0.39 (0.45) GW/cm^2 from dc (pulsed) measurements.

With the breakdown mechanisms identified, we sought to further improve the BV in our fourth-generation trench SBDs [21], [22]. W_{fin} was chosen to be 1 μm due to a less severe electric-field crowding near the trench bottom corners than in larger W_{fin} designs. In addition, as will be discussed in Section V, the peak electric field near the trench bottom corner can be reduced by decreasing d_{tr}. Thus, we adopted a reduced d_{tr} value of 1.1 μm. To mitigate the edge field crowding, we designed a field plate (FP) structure at the device periphery, as shown in the schematic cross section in Fig. 6(a). The optical top-view image of the fabricated field-plated trench SBD is shown in Fig. 6(b).

Fig. 6(c) shows the reverse *I*–*V* characteristics of the field-plated (FP) trench SBDs in comparison with regular

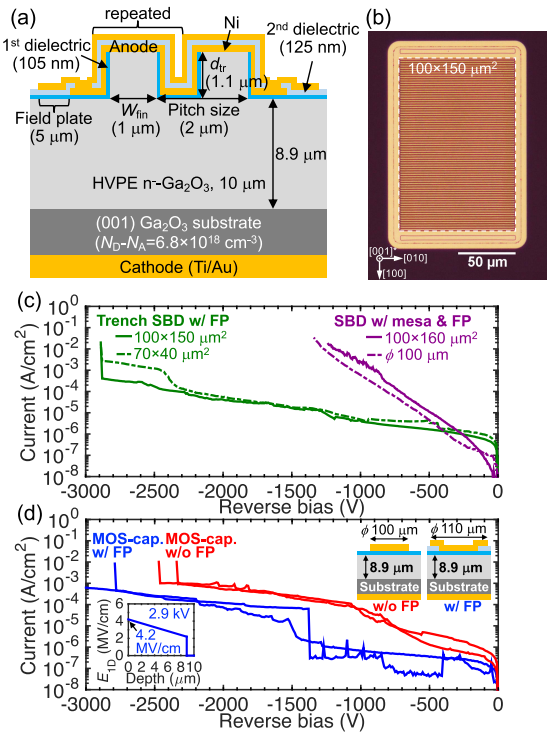

Fig. 6. (a) Schematic cross section of our fourth-generation field-plated (FP) Ga_2O_3 trench SBDs. (b) Optical image of the FP trench SBDs. (c) Reverse *I*–*V* characteristics of the FP trench SBDs in comparison with the regular SBDs. (d) Reverse *I*–*V* characteristics of the cofabricated MOS-capacitor test structures with or without the FP. Inset in (d) shows the calculated 1-D vertical electric-field profile at 2.9 kV in the field-plated MOS-capacitors. Reprinted from Li *et al.* [22] © 2020 IEEE.

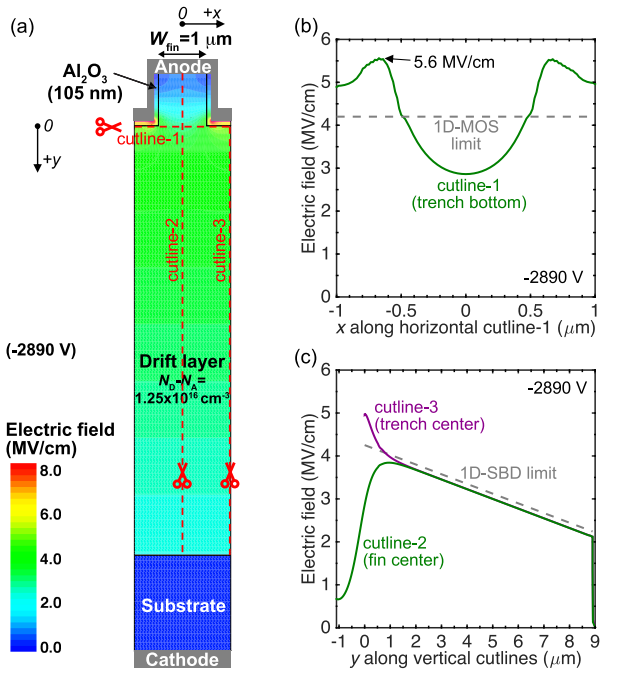

Fig. 7. (a) Simulated electric-field profile in an unit cell of the fourth-generation FP-Ga_2O_3 trench SBDs at the BV of 2.89 kV. (b) Electric-field profile along the horizontal cutline 1 nm under the trench bottom surface (cutline-1). (c) Electric-field profile along the vertical cutlines at the center of the fin channel (cutline-2) and the trench (cutline-3).

SBDs [22]. The reduced trench depth still allows for a sufficient RESURF effect as shown in the much-reduced reverse leakage current in the trench SBDs. The BV of the FP-trench SBDs is 2.89 kV. Together with a $R_{ON,sp}$ of 10.5 (8.8) m$\Omega \cdot$ cm^2 under dc (pulsed) measurements, the FP-trench SBDs achieved a record-high BFOM of 0.80 (0.95) GW/cm^2 among all Ga_2O_3 power devices reported so far.

The breakdown of the FP-trench SBDs is destructive, as indicated by the breakdown craters at the device edge. This suggests that breakdown is likely due to edge field crowding. As shown in Fig. 6(d), a similar BV is measured on cofabricated field-plated MOS-capacitors, which have an identical field-plate structure as the FP-trench SBDs, suggesting that the breakdown is indeed due to edge field crowding. This is not surprising: while the field-plate structure can reduce the edge-field crowding, it cannot fully eliminate it, and the remaining electric-field peak is still quite substantial according to our simulation results [21]. Here, the FP is indeed effective, since the MOS-capacitors without FP have a lower BV of ~2.4 kV. Clearly, more effective edge termination techniques other than FPs is highly desirable not only for trench SBDs, but also for vertical Ga_2O_3 power devices in general. In the article, we will focus only on the electric-field management in the active regions of trench SBDs without further discussing the subject of edge termination, which is a rich subject itself.

Inset in Fig. 6(d) shows the calculated electric-field profile in field-plated MOS capacitors at the BV of 2.9 kV. A parallel-plane E_{max} of 4.2 MV/cm is revealed, which is already higher than the E_c of 4H-SiC and GaN, but still lower than that of Ga_2O_3 due to the limitation of the edge termination. The electric-field profile within the unit cell of the FP-trench SBDs at the BV is simulated by TCAD Sentaurus, as shown in Fig. 7(a). As expected, the RESURF effect is observed near the Schottky contact.

Here, it is worth pointing out the "cost" of the RESURF effect, which is present in the increased electric field near the bottom of the trench. Fig. 7(b) shows the electric-field profile along the horizontal cutline 1-nm under the trench bottom surface (cutline-1). The parallel-plane surface electric-field limit of 4.2 MV/cm in a MOS-capacitor is also illustrated, representing the limiting case where $W_{fin} \rightarrow 0$ [1-D-MOS limit, see Fig. 2(c)]. Not only is there electric-field crowding near the trench bottom corner, the electric field at the center of the trench is also higher than the 1-D limit, i.e., the "cost."

Fig. 7(c) shows the electric-field profile along the vertical cutlines at the center of the fin channel (cutline-2) and the trench (cutline-3). In comparison, the parallel-plane electric-field profile in a regular SBD is also shown as a comparison, representing the limiting case where $d_{tr} \rightarrow 0$ [1-D-SBD limit, see Fig. 2(b)]. Cutline-2 reveals a E_{surf} of 0.7 MV/cm, corresponding to $\mathcal{R} \sim 6$ relative to the E_{max} of 4.3 MV/cm in the 1-D-SBD limit. We chose the E_{max} from the 1-D-SBD limit, since it is roughly an average of the profile along the two vertical cutlines, as can be seen from Fig. 7(c). In addition,

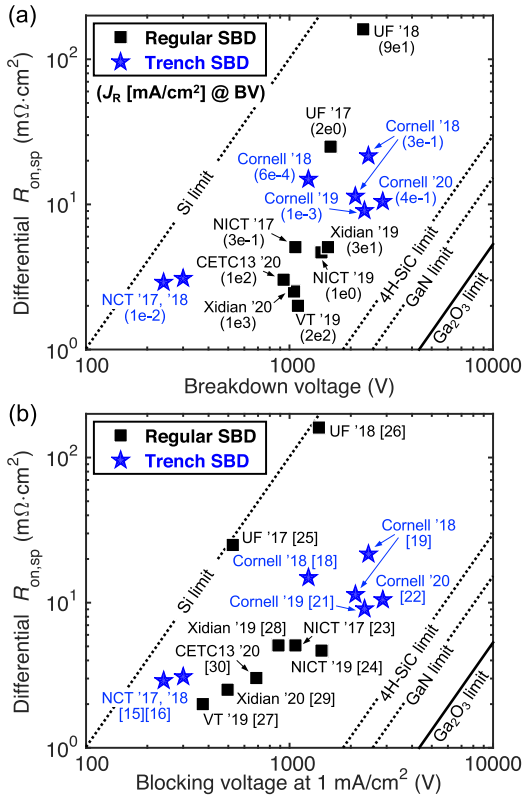

Fig. 8. Benchmark plots of the state-of-the-art Ga_2O_3 trench SBDs [15]–[19], [21], [22] and regular SBDs [23]–[30]. (a) Differential $R_{ON,sp}$ versus reported BV. The reverse leakage current density (J_R) in mA/cm^2 near the reported BVs are showed in parenthesis. (b) Differential $R_{ON,sp}$ versus BV defined at $J_R = 1$ mA/cm^2.

the 1-D-SBD limit is also the case where no RESURF effect is present. The close resemblance between the electric-field profile along the vertical cutlines and the 1-D-SBD limit below the trench bottom illustrates that the drift region can be designed based on the 1-D-SBD limit. On the other hand, the RESURF effect is mostly controlled by the design of the fin/trench region. As a result, the design of the RESURF structure and the drift region can be decoupled.

The dc performance of reported Ga_2O_3 trench SBDs to date [15]–[19], [21], [22] is benchmarked in Fig. 8(a) against the state-of-the-art Ga_2O_3 vertical SBDs [23]–[30]. In terms of the as-reported BFOM values to date, trench SBDs are only slightly superior than regular SBDs: the highest value of 0.8 GW/cm^2 in trench SBDs [22] versus that of 0.6 GW/cm^2 in regular SBDs [27]. However, the reverse leakage current in trench SBDs is generally much lower than regular SBDs at the BV, all having values below 1 mA/cm^2. If $J_R = 1$ mA/cm^2 is used as the breakdown criterion, as shown in Fig. 8(b), the effective BV of majority of the regular SBDs will be lower, while the BV of the trench SBDs will stay the same. The regular SBD reported in [24] shows notably higher BFOM than other regular SBDs in Fig. 8(b), largely due to its high barrier height (~1.77 eV).

In general, nearly all reported Ga_2O_3 SBDs to date are limited by the edge termination. With the limitation of edge termination removed, it is possible for Ga_2O_3 trench SBDs to approach the ultimate unipolar limit of Ga_2O_3 with $E_{surf} < E_{max} = E_c$, while regular SBDs will be limited by the surface electric field ($E_{surf} = E_{max} < E_c$).

IV. Modeling of $R_{ON,SP}$

Under a forward bias, the series resistance or the differential $R_{ON,sp}$ in trench SBDs can be separated into two main parts: R_1 that sums all the resistive components combined *below* the fin channels, including the drift region resistance, substrate resistance, and cathode contact resistance, R_2 from the fin channels, as illustrated in Fig. 5(a). Within the fin channels, if there is no contribution to the conductance from accumulation of electrons at the sidewall interface, R_2 will be determined solely by the conducting area within the fin channel. From capacitance–voltage analysis on planar MOS-capacitors, we found that the accumulation condition requires a very large forward bias due to acceptor-like interface states on the etch Ga_2O_3 surfaces [18]. Thus, the absence of accumulation is a reasonable assumption for the current devices. Furthermore, there may be a certain sidewall depletion width (W_d) due to the presence of negative interface charge on the sidewall [20], [31]. This will reduce the effective conduction width of the fin channel from W_{fin} to $W_{fin} - 2W_d$. Considering the impact of the sidewall depletion, the differential $R_{ON,sp}$ in trench SBDs is given by [22]

$$R_{ON,sp} = R_1 + \frac{R_2}{(1 - \frac{2W_d}{W_{fin}}) \cdot AR} \tag{4}$$

where R_2 here is the specific ON-resistance in the fin channel. The AR and W_d capture the effective conducting area in the fin channels relative to the total device active area.

Fig. 9(a) shows the measured differential $R_{ON,sp}$ as a function of AR in our third-generation devices, as well as the $R_{ON,sp}$ model without considering the sidewall depletion [19]. While decent agreements are observed between the model and the measured data for $W_{fin} \geq 2$ μm, the measured $R_{ON,sp}$ with $W_{fin} = 1$ μm can only be fit with a effectively smaller W_{fin}, indicating the presence of sidewall depletion.

Fig. 9(b) shows the measured $R_{ON,sp}$ as a function of W_{fin} in our fourth-generation devices. Here, under an identical AR, an increase of the $R_{ON,sp}$ with decreasing W_{fin} is observed, a clear indication of the presence of sidewall depletion. This behavior can be well-fit with the $R_{ON,sp}$ model using (4), from which a sidewall depletion width of 120 nm ± 30 nm at a forward bias of 3 V is extracted. The $R_{ON,sp}$ model is also applicable to similar devices such as vertical fin transistors [32], as long as the contribution from sidewall accumulation can be neglected. If not, a more elaborated $R_{ON,sp}$ model will need to be developed. In fact, the sidewall accumulation could reduce the fin-channel resistance significantly, and even provide a surge current capability in trench SBDs, thus a good MOS-interface quality is highly desirable. Without sidewall accumulation, it is important to maintain a reasonably high AR, such that the contribution from the fin-channel resistance is insignificant, leaving the drift region resistance as the dominant contribution – an assumption we made earlier for the V_{ON} model.

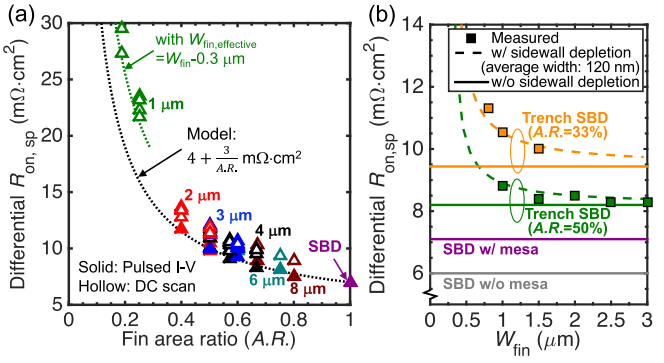

Fig. 9. (a) Differential $R_{ON,sp}$ of the third-generation Ga_2O_3 trench SBDs as a function of the fin AR, as well as the fitting using the $R_{ON,sp}$ model without considering sidewall depletion. Adapted from Li *et al.* [19] © 2018 IEEE. (b) Differential $R_{ON,sp}$ of the fourth-generation FP Ga_2O_3 trench SBDs as a function of the fin width (W_{fin}), as well as the fitting using the $R_{ON,sp}$ model considering sidewall depletion (4). Reprinted from Li *et al.* [22] ©2020 IEEE.

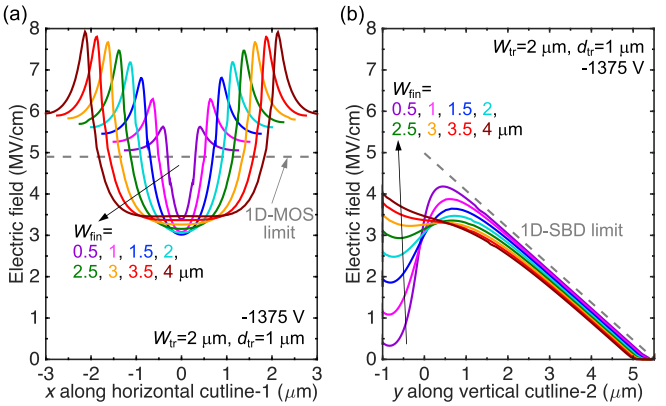

Fig. 10. Simulated electric-field profile along (a) horizontal cutline-1 under the trench bottom surface and (b) vertical cutline-2 at the center of the fin channel, under different values of W_{fin} and a reverse bias of −1375 V.

V. Design of the Electric-Field Profile

A central part in the design of trench SBDs is the design of the electric-field profile under reverse bias. In general, the electric-field profile at a certain reverse bias is mainly controlled by the doping profile, the fin/trench geometry, and to a lesser extent the dielectric properties. In the simplified case as shown in Fig. 2(a), the doping concentration is assumed to be constant in the entire n^--layer including the fin region, and the fin/trench geometry is determined by only three parameters: W_{fin}, W_{tr}, and d_{tr}. In this section, we will investigate the impact on the electric-field profile by these three parameters. We should note that the trench bottom corner should ideally be rounded to reduced the associated electric-field crowding. But for simplicity, we only consider an abrupt 90° trench corner in this article, i.e., the worst scenario.

As mentioned previously in Section III, a good starting point of the drift region design is the 1-D-SBD limit [Fig. 2(b)]. Here, we aim at a BV of 1.2–1.4 kV and a target average E_{max} of 5 MV/cm for a sufficient design margin in the case of Ga_2O_3. Under a non-punch-through condition at BV, the BV and E_{max} will determine the net doping concentration (N_d) and thickness (d_{drift}) of the drift region, according to the familiar expressions: $BV = eN_d d_{drift}^2/(2\varepsilon_s)$ and $E_{max} = eN_d d_{drift}/\varepsilon_s$. For simplicity, we have designed the drift region with $N_d = 5 \times 10^{16}$ cm^{-3} and $d_{drift} = 5.5$ μm, corresponding to a BV of 1375 V under a E_{max} of 5 MV/cm. The dielectric layer has a minor influence on the overall field profile. We have chosen a thickness (d_{ox}) of 100 nm, similar to what was used in our trench SBDs [18], [19], [22]. The dielectric constant (ε_{ox}) is taken to be 8.2 ε_0, corresponding to the measured value of Al_2O_3 [18]. Due to the 2-D nature of the electric-field profile, it is difficult to obtain analytical solutions, thus we simulate the profile using TCAD Sentaurus.

Fig. 10(a) and (b) shows the influence of W_{fin} on the electric-field profile along the horizontal cutline-1 below a trench bottom surface and the vertical cutline-2 at the center of the fin channel, respectively. The definition of the cutlines are the same as in Fig. 7(a). Similar to what we have reported in [19], a smaller W_{fin} is beneficial for both a smaller electric-field peak at the trench bottom corners as well as a more pronounced RESURF effect. In practice, there is a lower limit of W_{fin} due to both manufacturability and the likely existence of a certain sidewall depletion width due to the built-in potential. A W_{fin} around 1 μm may be a sweet spot with all the factors considered, and also with the feasibility verified experimentally [15], [21], [22].

Fig. 11 shows the influence of d_{tr} on the electric-field profile. Here, a tradeoff is observed between the surface electric field and the electric field near the trench bottom: a larger d_{tr} will reduce E_{surf} but at a cost of an increase in the electric field near the trench bottom with respect to the 1-D limit. Therefore, d_{tr} should be made as small as possible, as long as a sufficient RESURF effect is maintained, i.e., the RESURF effect should not be over-designed. A smaller d_{tr} also benefits the $R_{ON,sp}$.

Fig. 12 shows the influence of W_{tr} on the electric-field profile. As can be seen in Fig. 12(b), under the same fin geometry, the RESURF effect is nearly independent of W_{tr}. To minimize $R_{ON,sp}$, W_{tr} should be made as small as possible for the largest AR. However, as shown in Fig. 12(a), the electric field near the trench bottom increases rapidly with reducing W_{tr}. Therefore, a reasonably large W_{tr} should be maintained.

Finally, it is worth noting that the aforementioned influences of the trench-geometry parameters are not specific to one drift-layer design and Ga_2O_3 only. Rather, the qualitative trends are universal, as governed inherently by the Poisson equation in 2-D.

VI. Design Flowchart and Example

Based on the effect of the fin/trench geometry on the electric-field profile, we discuss a design example of a 1375-V Ga_2O_3 trench SBD with a Schottky barrier height of 1.1 eV. A universal design flow is summarized in Fig. 13. We target at a $J_{R,max}$ of ∼1 mA/cm^2 at 150 °C, ensuring an even lower $J_{R,max}$ at lower temperature. Regarding the constraints on the electric field, we adopt the same average E_{max} of 5 MV/cm as

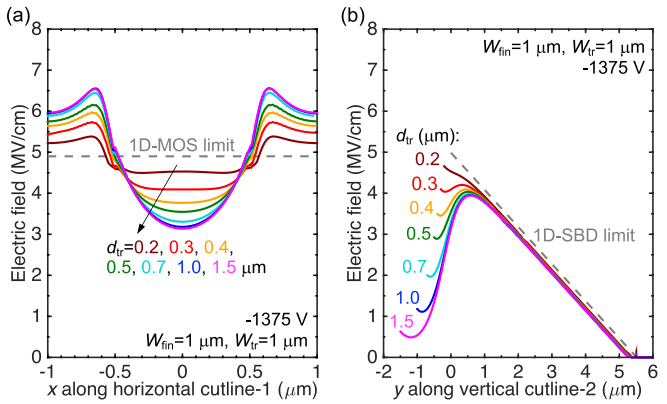

Fig. 11. Simulated electric-field profile along (a) horizontal cutline-1 under the trench bottom surface and (b) vertical cutline-2 at the center of the fin channel, under different values of d_{tr} and a reverse bias of −1375 V.

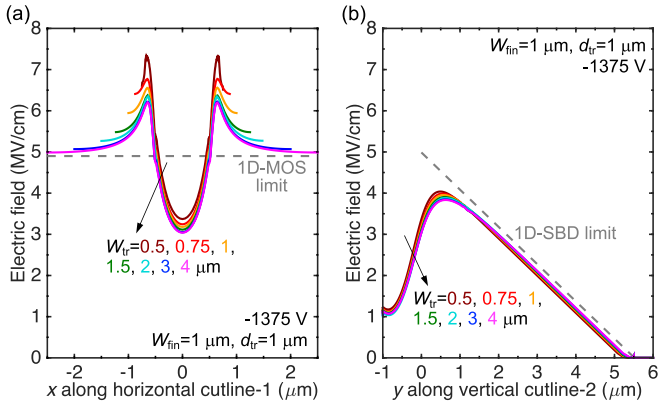

Fig. 12. Simulated electric-field profile along (a) horizontal cutline-1 under the trench bottom surface and (b) vertical cutline-2 at the center of the fin channel, under different values of W_{tr} and a reverse bias of −1375 V.

TABLE I

SUMMARY OF THE CALCULATED DC CHARACTERISTICS OF THE DESIGNED 1375-V b-Ga_2O_3 TRENCH AND REGULAR SBDs. (THE FIN/TRENCH GEOMETRY IN THE TRENCH SBD IS DESIGNED WITH $W_{fin} = 1\ \mu m$, $W_{tr} = 1\ \mu m$ AND $d_{tr} = 0.85\ \mu m$. FOR THE DIELECTRIC LAYER, $d_{ox} = 100$ nm AND $\varepsilon_{ox} = 8.2\ \varepsilon_0$)

	ϕ_B (V)	N_d (cm^{-3})	d_{drift} (μm)	T (°C)	J_R @ 1375 V (mA/cm^2)	V_{on} @ 100 A/cm^2 (V)	differential $R_{on,sp}$ ($m\Omega \cdot cm^2$)
Trench SBD	1.1	5×10^{16}	5.5	25	1.3×10^{-2}	0.90	0.54
				150	1.3	0.82	1.0
Regular SBD	1.1	4×10^{15}	19.5	25	5.9×10^{-3}	2.7	18
				150	1.3	4.2	35

used in Section V, and limit the peak E_{max} to below 7 MV/cm, which is around the E_c of β-Ga_2O_3. Consequently, the drift layer design remains the same as discussed in Section V.

The design of the fin/trench geometry needs to satisfy the requirements on the leakage current and the peak E_{max}. From the calculation of the reverse leakage current [6], we found that with $\phi_B = 1.1$ eV, a J_R of 2.5 mA/cm^2 can be maintained

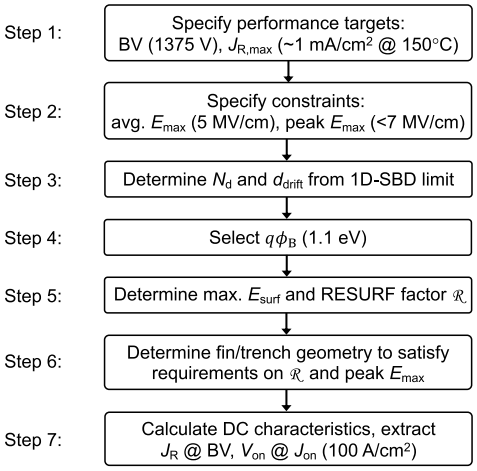

Fig. 13. Device performance target-oriented design flowchart for trench SBDs. Note that steps 4–7 can be performed iteratively to determine the optimum barrier height for the lowest possible V_{ON}.

at 150 °C with an E_{surf} of 1.51 MV/cm, corresponding to a RESURF factor of 3.3 with respect to the average E_{max}. With a fin AR of ~50%, this will lead to a $J_{R,max}$ of ~1.3 mA/cm^2, close to our design target.

We first chose W_{fin} to be 1 μm. W_{tr} is designed to be 1 μm for an AR of 50%, with a moderate increase in the electric field near the trench bottom, as shown in Fig. 12(a). The design of d_{tr} depends on the requirement on the E_{surf} or the RESURF factor. From simulation, a d_{tr} of 0.85 μm is found to be sufficient. Note that along the top Schottky contact surface in trench SBDs, the surface electric field is nonuniform. However, it has a highest value at the center of the fin channels. Thus, as long as the E_{surf} at the center for the fin channel satisfies the requirement on J_R, the overall leakage current will certainly do. With this design, the peak electric field in Ga_2O_3 at 1375 V is extracted to be 6.5 MV/cm from simulation [also can be seen from Fig. 11(a)]. This value complies with our requirement on the peak E_{max}. Note that the peak electric field can be reduced with a rounded trench bottom corner, which has been recently explored in a TCAD simulation study [33].

The calculated reverse and forward I–V characteristics of the designed 1375-V Ga_2O_3 trench SBD is shown in Fig. 14(a) and (b), respectively. At the designed BV of 1375 V and 150 °C, J_R is calculated to be 1.3 mA/cm^2. The differential $R_{ON,sp}$ of the trench SBD is calculated from the $R_{ON,sp}$ model discussed in Section IV. To obtain the same J_R in a regular SBD with the same barrier height, the required drift layer thickness and doping under a non-punch-through condition is 19.5 μm and 4×10^{15} cm^{-3}, respectively. The reverse and forward I–V characteristics of such a regular SBD is also shown in Fig. 14 as a comparison. It can be seen from Fig. 14(b) that the regular SBD has a much higher $R_{ON,sp}$ than the trench SBD due to the much higher resistance in the drift layer.

The design parameters and detailed dc performance metrics of these two SBDs are summarized in Table I. Notably, the differential $R_{ON,sp}$ of the trench SBD is >30× smaller than the regular SBD. The drastic reduction V_{ON} in the trench SBD is

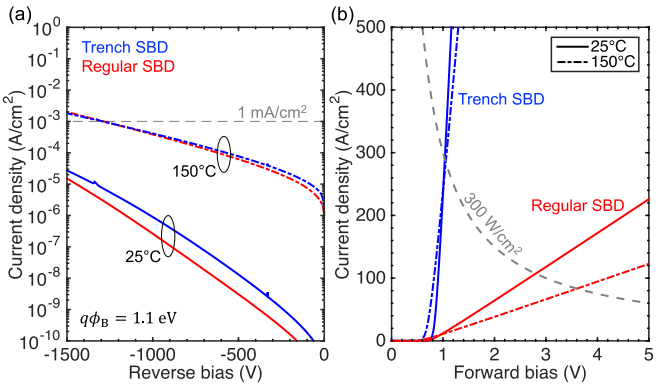

Fig. 14. Calculated (a) reverse *I–V* and (b) forward *I–V* characteristics of the design example of a 1375-V Ga_2O_3 trench SBD, in comparison with a regular SBD counterpart. The designs target at the same leakage current at 150 °C [6] at the same BV of 1375 V for both the trench and regular SBDs, followed by the determination of the drift layer parameters and SBD forward characteristics in the two types of SBDs (see Fig. 13). Detailed design parameters and dc performance metrics are summarized in Table I.

consistent with the calculated V_{ON} results shown in Fig. 3(b), barring the exact values of V_{ON} due to the approximations we made in (3) ($V_{bi} \approx \phi_B$ and $R_2 \ll R_1 \approx R_{ON,sp}$). This example highlights the importance of RESURF effect in the design of kilovolt-class high-efficiency power rectifiers based on UWBG semiconductors.

VII. Conclusion

In this article, we showed that for kilovolt-class operation, the trench SBD structure is not only preferred, but arguably necessary for high-efficiency rectifiers based on β-Ga_2O_3. In fact, this is true for all UWBG semiconductors. The RESURF effect in trench SBDs decouples the reverse leakage current J_R from the maximum electric field E_{max} in the device structure, allowing for a higher average E_{max} to be reached away from the Schottky contact interface, which leads to a lower $R_{ON,sp}$ and V_{ON}. An analytical model for V_{ON} is derived for trench SBDs, revealing the importance of the RESURF effect quantitatively. Experimental demonstrations of Ga_2O_3 trench SBDs to date have already confirmed the presence of the RESURF effect, which leads to a generally higher BV and lower J_R than regular SBDs. A simple model for $R_{ON,sp}$ is provided and experimentally verified. Through a simulation study, the effect of fin/trench geometry on the electric-field profile is identified, which is important for the design optimization. A design example of a kilovolt-class Ga_2O_3 trench SBD is presented, which show a V_{ON} lower than 1 V at an ON-current of 100 A/cm^2.

Finally, it is worth pointing out that the dielectric layer in trench SBDs plays an important role in supporting the high electric field in UWBG semiconductors. Due to the continuity of the electric displacement field across the MOS interface, the electric field in the dielectric layer can also be very high, leading to reliability concerns. This is a universal challenge among all UWBG power devices using MOS structures and is out of the scope of this article. However, without going into details, we mention three potential solutions to this issue for UWBG trench SBDs: 1) development of breakthrough high-κ dielectric materials with high breakdown field and reliability; 2) development of p-type shield regions under the trench bottom surface through p-n heterojunctions; and 3) design of a safe operating margin at a cost of a reduced performance but with the reliability preserved. Clearly, these solutions require innovations from both fundamental material science as well as device design. With further advancements on the edge termination and the robustness of the dielectric layer, trench SBDs could effectively harness the high electric-field capability of UWBG semiconductors for efficient power rectification.

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