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Degradation Mechanisms of GaN-Based Vertical Devices: A Review

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This article reviews most recent results on the reliability of vertical GaN-based devices, by presenting a few case studies focused on the stability and degradation of high-voltage GaN-on-GaN diodes and of GaN-based field-effect transistors (FETs). With regard to diodes, two relevant stress conditions are investigated. The first is operation at high forward current that can induce a degradation of the electrical properties of the devices, mostly consisting in an increase in the operating voltage, well correlated to a decrease in the electroluminescence signal emitted by the diodes. This degradation process is ascribed to the diffusion of hydrogen from the highly p-type doped regions toward the junction, with consequent compensation of the acceptor (Mg) dopant. The second stress regime investigated on diodes is avalanche: specifically, it is shown that polarization-doped GaN devices may show avalanche capability, and the stability of diodes in avalanche regime is investigated in detail. With regard to transistors, the analysis is focused on GaN-on-GaN vertical Fin-FETs. First, the stability of the threshold voltage under positive gate stress is analyzed, and the role of interface/oxide traps is discussed by experimental characterization. Then, the degradation under positive gate or high-drain stress is investigated, to provide information on the dominant degradation processes.

1. Introduction

Over the last decade, the research in the field of GaN-based power devices has shown impressive advancements. Due to the heteroepitaxial growth on silicon substrates, GaN-based high-electron mobility transistors (HEMTs) can reach a high performance while having a relatively low cost. Currently, industrial efforts are mainly focused toward GaN lateral field-effect transistors (FETs) because they can be easily fabricated using a complementary metal oxide semiconductor compatible process. In addition, the use of an AlGaN/GaN heterostructure—in the presence of large polarization fields—allows to maximize channel conductivity and electron density. GaN lateral devices are now commercially available and target voltages up to 900 V,[1] thus competing with Si- and SiC-based components for consumer and industrial electronics, and for the automotive field. The high breakdown field (11 times higher than silicon) and the wide energy gap (3.4 eV) allow high-voltage and high-temperature operation, thus ensuring a high reliability to this technology.

Despite the great potential of GaN lateral devices, they have some limitations that may slow their applicability in the >1 kV range. First, the breakdown voltage of a lateral transistor scales with the gate–drain spacing, i.e., with device area. Reaching high breakdown voltages is technically feasible, but results in an increase in device area and cost. Increasing device size can also impact parasitic resistance. A second factor that needs to be considered is that lateral devices are very sensitive to surface effects. The 2-dimensional electron gas (2DEG) is very close to the surface, and trapping processes at the AlGaN/passivation interface may significantly impact the dynamic performance of the devices.[2] In addition, in most cases the electric field in lateral devices is not uniform, across the gate–drain spacing, and has peaks at the edge of the gate and of each field plate. Field can be minimized through the use of field plates; however, the addition of field plates may impact device capacitance, and an accurate design must be conducted to ensure simultaneously low-field and high

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device performance.[3,4] Finally, lateral GaN HEMTs are typically based on an AlGaN/GaN heterostructure, which is intrinsically normally-on. To reach normally-off operation, a p-type gate can be used,[5] and threshold voltages above 1 V can be obtained.[6] If higher threshold voltages are required (e.g., 3–5 V; see ref. [7] and references therein), different approaches can be considered, such as the use of an metal insulator semiconductor/metal oxide semiconductor (MOS) structure or the adoption of a cascoded configuration.

Several Si and SiC power transistors are based on a vertical configuration: the flow of current is controlled by a gate placed on the top of the transistor, and electrons flow through a thick drift-region, over which most the potential drops in off-state. The vertical approach allows to increase the breakdown strength of the transistors, without impacting device area, provided that sufficiently thick drift regions are fabricated. Also, vertical devices are almost insensitive to surface trapping effects because current flow takes place in the bulk semiconductor. As was the case for Si and SiC, also GaN is now ready for the transition to vertical configuration. GaN vertical diodes and transistors have already been demonstrated, grown on free-standing GaN substrates with dislocation densities up to 10^6 cm^{-2}.[7–60] In several cases, the breakdown voltage of these devices is higher than 1 kV, thus clearing the way to the application in the power semiconductor field. Recent reports also demonstrated the possibility of growing GaN vertical devices on foreign substrates (see, e.g., refs. [41, 52, 60–66]). Both the quasivertical and the fully vertical approaches have been implemented, to ensure an effective extraction of current from the drain. The research on vertical GaN-on-Si is mainly driven by the need of reducing the cost of GaN vertical devices: a recent study[63] evaluated the cost of wafer and epitaxy for different vertical GaN technologies, and indicated that vertical GaN-on-Si devices can allow a 10–100 times cost reduction. Another advantage of vertical GaN-on-Si is that it is compatible with 8 in. production lines, thus being suitable for effective industrial production. Obviously, the development of vertical GaN-on-Si technology is slowed by the higher dislocation density and by the difficulty of growing thick drift regions on a silicon substrate: these aspects are currently under investigation, and quasivertical vertical and fully vertical GaN power diodes on foreign substrate (Si) with breakdown voltages near 1 kV have already been demonstrated.[35,67]

With regard to GaN vertical diodes, both Schottky-barrier diodes and p–n diodes have been investigated and fabricated. In both cases, improvements in breakdown voltage were obtained through the optimization of the growth conditions (see, e.g., ref. [10]), a careful design of the drift region,[41] or the use of guard rings.[39] With regard to vertical transistors, several approaches have been proposed: the current aperture vertical electron transistor (CAVET) uses a combination of 2DEG channel and vertical drift region. Current blocking layers are used to create a barrier for electrons that can only flow through a current aperture at the center of the device.[43] Another approach is the vertical trench metal oxide semiconductor field effect transistor (MOSFET) (see refs. [39, 60] for recent examples), where an MOS structure is used in combination with a trench to control the flow of current through the device. A third approach is the vertical power Fin-FET:[68] here current flow is controlled through the use of nanometer size fins, typically composed only of n-type material. Finally, vertical 3D GaN nanowire MOSFETs and PolarMOS have also been proposed.[68–70]

All the structures described earlier are of high interest for the development of GaN-based vertical devices. Each of them has intrinsic advantages and potential drawbacks that represent interesting research challenges, rather than fundamental limits. Previous reports preliminarily investigated the stability of vertical GaN-based components (see, e.g., ref. [71]), suggesting that these devices can have a good ruggedness and a good potential for high-voltage applications.

Over the last few years, we have analyzed several GaN vertical devices, both diodes and transistors,[49,50,69,70,72–76] identifying

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and describing the most relevant degradation mechanisms and related processes. The aim of this article is to present a summary of our most recent results in this field, by describing a number of case studies conducted in our laboratories on GaN-based vertical devices.

More specifically, the first case study that we present here deals with the stability of p–n diodes under high current stress, and is relevant for the development of reliable diodes. In fact, GaN-based vertical diodes are expected to be operated at high current and current density (>kA cm^{-2}). Under such stressful conditions, the stability of the resistivity and turn-on voltage must be carefully evaluated. To this aim, we conducted a set of stress experiments at high current density on p–n diodes, and investigated the electrical degradation of the devices during stress time. The results collected within this study suggest that during operation at high current densities, a diffusion process leads to an increase in the operating voltage and to a decrease in the electroluminescence (EL) signal emitted by the devices. The results are interpreted by considering the diffusion of hydrogen from the top p-doped layer toward the junction.

The second case study described later deals with the operation of GaN p–n diodes in avalanche regime. We analyzed polarization-induced p–n diodes that are the basic units of PolarMOS. First, we show that polarization-doped p–n diodes have avalanche capability; second, we investigate the stability of the avalanche voltage with stress time, and discuss the origin of the "breakdown-walkout" and its relation with traps within the drift region.

The third case study deals with GaN-based vertical Fin-FETs. On these devices, we investigated the threshold voltage instabilities induced by operation at positive gate stress, demonstrating the existence of two different trapping processes: the detrapping of electrons from the gate insulator that takes place at low stress voltages (<2 V) and results in a negative threshold voltage shift, and the injection of electrons from the channel into the gate insulator that occurs at higher stress bias (up to 5–6 V) and results in a positive threshold shift.

Finally, we analyzed the robustness of GaN-based vertical FETs under high electric field, suggesting that the quality of the gate oxide and the minimization of the field are necessary steps for the optimization of the reliability of the devices.

2. Degradation of GaN-on-GaN Vertical Diodes Submitted to High Current Stress

The degradation of impurity-doped vertical GaN p–n diodes stressed at high current density was investigated by means of electro-optical measurements.[72]

The structure of the analyzed devices consists of a Si-doped n-GaN layer (10 μm) with a doping $N_D \approx 2 \times 10^{16}$ cm^{-3}, a Mg-doped p-GaN layer (0.4 μm) with a doping higher than 10^{19} cm^{-3}, and a Mg-doped p$^+$-GaN layer (0.02 μm) with a doping higher than 10^{20} cm^{-3} grown by metal-organic chemical vapour deposition (MOCVD) on a GaN substrate.[77–79] The devices have a diameter of 110 μm and were optimized for high voltage operation through the use of a field plate.[78]

To study the physical mechanism responsible for the degradation of the impurity-doped p–n diodes under forward bias condition, a high current density of 0.7 kA cm^{-2} was applied for 36 000 s and the electrical and optical parameters were monitored during the stress.

Figure 1 shows the behaviour of the *I–V* and *L–I* characteristics at different stress times. We found that the stress at high current density resulted in an increase in turn-on voltage (and on-resistance) (Figure 1a) and in a decrease in the EL signal (Figure 1b). In particular, the changes in the *I–V* curves for increasing stress time were characterized by three main phenomena, as shown in Figure 1a: the first phenomenon was the increase in the turn-on voltage and it was visible after 300 s of stress; the second one was the increase in the generation–recombination current in the low forward region and it was visible after 6300 s; and the third one was the increase in the leakage current in the reverse bias region and it was visible after 31 500 s.

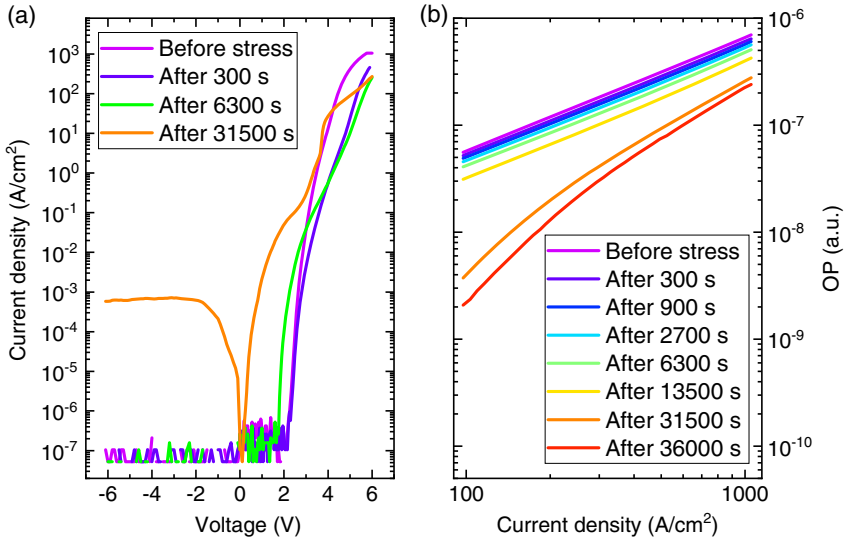

Figure 1. a) *I–V* and b) *L–I* curves measured before stress and after each step of the stress of an impurity-doped p–n diodes at $J_{stress} = 0.7$ kA cm^{-2}. Experimental data from ref. [72].

On the contrary, by analysing the EL versus current characteristics in Figure 1b, a gradual degradation in the optical performance of the device was visible up to 13 500 s, and then, for longer stress times, a further degradation process took place. This latter could be related to the generation of nonradiative defects within the depletion region, as suggested by the fact that the slope of the log–log *L–I* curves increased from nearly 1 toward 1.7 for stress times longer than 13 500 s.[78,80]

It is worth noting that the decrease in the optical power was linearly correlated with the increase in on-resistance for increasing stress times, as shown in **Figure 2**a, suggesting a common origin of the degradation of the electrical and optical performance. This common origin could be related to the presence of hydrogen in the device.

Hydrogen is introduced within the p-GaN layers during the growth and typically it has concentration similar to Mg.[81] The H atoms tend to create Mg—H bonds, which may be broken by temperature and current flow, leaving H interstitial in the lattice that can diffuse from the highly doped p-GaN layer toward the p–n junction, following the concentration gradient. The H atoms can therefore passivate Mg atoms near the junction, resulting in a lower hole injection due to the acceptor compensation; a lower hole concentration can explain both the decrease in the EL signal and the increase in turn-on voltage.

The hypothesis that the physical mechanism responsible for the degradation of impurity-doped p–n diodes was caused by a diffusion mechanism, possibly involving H atoms, is supported by the dependence of the variation of both the optical power and the on-resistance on the square root of time (Figure 2b). In fact, the square-root dependence on stress time of the electrical and optical parameters obeyed the Fick's second law in one dimension (Equation 1)

$$N_{\text{diff}}(x,t) = N_0 \,\text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \quad (1)$$

where N_{diff} is the number of impurities that can be found at position x at time t, N_0 is the concentration of the impurities at the junction (that is assumed to be constant), erfc is the error function, x is the distance from the junction, D is the diffusion coefficient, and t is the stress time.[82,83]

For longer stress times, the degradation mechanism causes a further increase in the slope of the log–log *L–I* curves. This increase could be explained by the generation of shockley read hall-recombination centers.[84]

3. Demonstration of Avalanche Capability in Polarization-Doped Vertical GaN p–n Diodes: Study of Walkout due to Residual Carbon Concentration

Next, we investigated the avalanche capability and the stability of polarization-doped vertical GaN p–n diodes in avalanche mode.[49,50] The devices are grown by MOCVD and have a GaN substrate, a Si-doped n^--GaN layer (200 nm) with doping $N_D \approx 10^{18}\,\text{cm}^{-3}$, a Si-doped n-GaN layer (7 μm) with doping $N_D \approx 2\times10^{16}\,\text{cm}^{-3}$, a n-type linearly graded AlGaN layer with the Al composition graded up from 0% to 5.6% (1 μm), a p-type linearly graded AlGaN layer with the opposite Al composition gradient (from 5.6% to 0%) (0.4 μm), and a Mg-doped p-GaN layer (20 nm) with a doping higher than $10^{20}\,\text{cm}^{-3}$.[85] A p–n junction obtained by grading the Al composition results 1) in an enhancement of p-type conductivity compared with the impurity-doped case, 2) in a doping level that does not strongly depend on temperature or frequency, 3) in the absence of carrier freeze-out, in contrast to what the impurity-doped carriers do when the temperature decreases, and 4) in a higher breakdown field due to the larger bandgap of AlGaN.[70] The breakdown voltage of the analyzed diodes is significantly improved through the use of a field plate.[77–79]

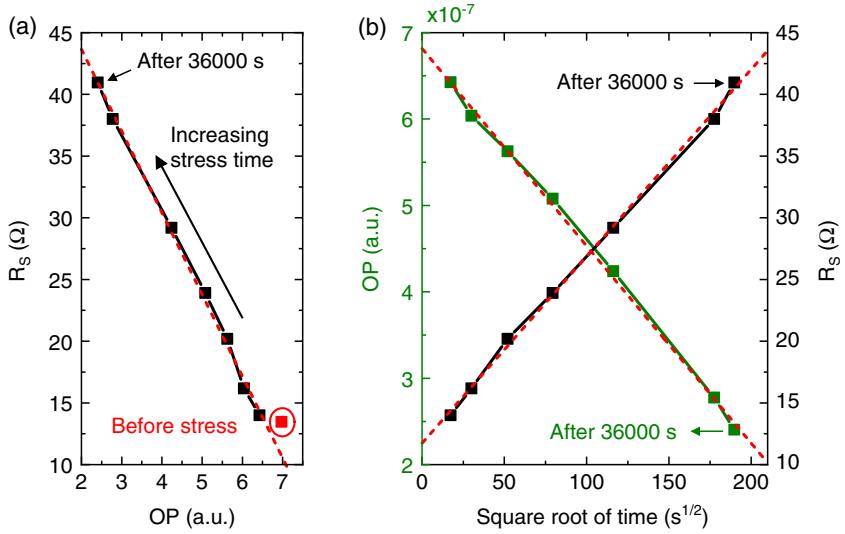

Figure 2. a) Relation between the increase in the series resistance and the decrease in the optical power during the stress. b) Relation between the variation of the optical power (green curve) and of the series resistance (black curve) and the square root of stress time. Experimental data from ref. [72].

Two generations of these polarization-doped p–n diodes were characterized and compared: the Gen1 diodes have a high carbon level throughout the device structure, on the order of $2–3 \times 10^{16}\,cm^{-3}$, and the Gen2 diodes have a carbon level below the detection limit of secondary ion mass spectrometry (SIMS) $<1 \times 10^{16}\,cm^{-3}$. It was found that both generations are avalanche capable, and the Gen1 diodes exhibit recoverable breakdown walkout while the Gen2 diodes do not. The summarized study on the Gen1 diodes is presented later, while the study on the Gen2 diodes will be reported elsewhere. The avalanche capability of the Gen1 diodes was tested by means of *I–V* characterizations at different temperatures (inset of **Figure 3**). As can be noted, the diodes have a low leakage current up to high breakdown voltage (−1370 V at 30 °C), where a sudden increase in the current occurs. By analyzing the reverse voltage for a current density of $-10\,mA\,cm^{-2}$, a positive temperature coefficient with a slope of $0.5\,V\,°C^{-1}$ was found, indicating an avalanche process.

It was therefore necessary to understand if the breakdown voltage was stable, because the stability of p–n diodes under avalanche regime is important for high reverse voltage operation. To investigate the behavior of the devices when a strong reverse bias was applied, a constant current stress in avalanche mode ($J_{stress} = -1\,mA\,cm^{-2}$) was conducted. Figure 3 shows that the avalanche voltage increases with increasing stress time. This time-dependent shift of the reverse voltage to higher (negative) values is referred to as breakdown walkout,[86–88] and it was found to be fully recoverable in the analyzed devices after some rest time. Then, we analyzed the transients of the breakdown voltage during the recovery phase conducted after the constant current stress in avalanche mode at different temperatures; the Arrhenius plot shown in **Figure 4** (black symbols) was obtained. By comparing the Arrhenius plot with previous reports a deep level possibly related to carbon on nitrogen site CN was found.[89–92] To confirm the presence of C_N, capacitance-deep-level transient spectroscopy (C-DLTS) measurements were carried out at different temperatures. These measurements consist in two phases: in the first phase the defects in the space charge region are filled by applying a filling voltage, and in the second one the detrapping process from the deep levels are studied by analyzing the capacitance variation at a certain measure voltage.[93] By repeating the measurements at different voltages, it is possible to investigate different active volumes of the device, and by repeating the measurements at different temperatures it is possible to extract an Arrhenius plot. The results of the temperature-dependent measurements are shown in Figure 4 (red symbols); a deep level possibly ascribed to C_N was found again.

The experimental data therefore suggest that the breakdown walkout process could be related to the presence of residual carbon in the polarization-doped p–n diodes. A model able to explain these experimental results was proposed, by considering that, when a strong reverse bias is applied, C_N behaves as a deep acceptor and is ionized. This leads to an increase in the Coulomb and phonon scattering in the lattice (due to the higher number of ionized impurities), and consequently to a decrease in the mean free path of carriers. To trigger impact ionization, the electrons need to gain enough energy to create an additional electron–hole pair, and the density of electrons that have sufficient energy depends on the mean free path, as can be seen in Equation (2)

$$n^* = n \cdot \exp\left(-\frac{d}{\lambda}\right) \tag{2}$$

where n^* is the density of electrons that have the energy required to start the avalanche process, n is the total electron density, d is the distance necessary to gain sufficient energy for the impact ionization, and λ is the mean free path. Therefore, a decrease in the mean free path corresponds to a decrease in the density of electrons that have sufficient energy to create additional electron–hole pairs. Therefore, once more and more C_N is ionized, a higher negative voltage will be necessary to start the avalanche multiplication.

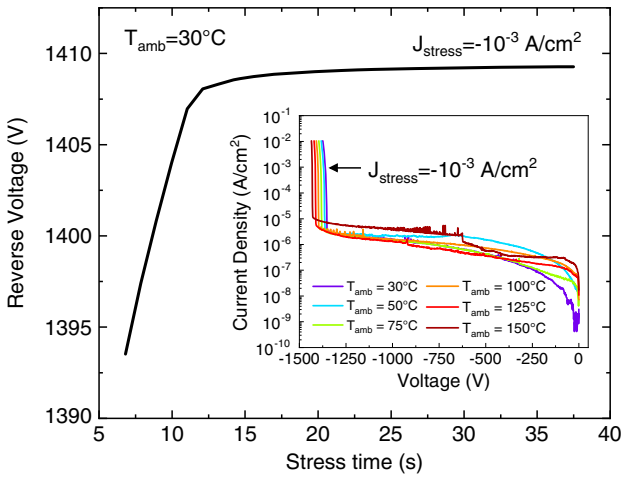

Figure 3. Time dependence of breakdown walkout. The breakdown voltage increases during the stress time in avalanche mode. Inset: *I–V* curves at different temperatures of the diode under reverse bias condition. Experimental data from ref. [49, 50].

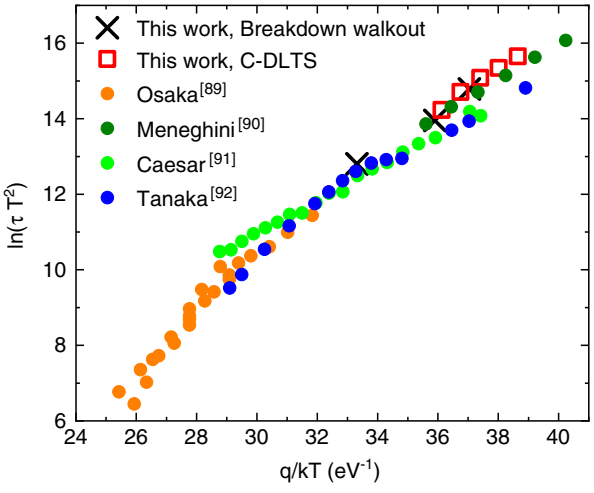

Figure 4. Comparison between defects identified in the literature and the Arrhenius plot obtained by analyzing the breakdown walkout process (black symbols) and the C-DLTS measurements (red symbols). Experimental data from ref. [49, 50].

4. Analysis of the Trapping Mechanisms and Degradation on GaN-on-GaN Vertical FETs

Among vertical GaN devices, the vertical fin field-effect transistors (VFETs) have recently demonstrated to be an excellent candidate for next-generation power converters.[23,94] The VFET epitaxial layers are grown on a 2 in. GaN substrate. The epitaxial layers consist of 8 μm-thick n-GaN channel and n^--GaN drift layer doped 2×10^{16} cm^{-3} and 0.3 μm-thick n^+-GaN. To obtain MOS gate stacks on sidewalls, a combined dry–wet etching technique is used and a 15 nm Al_2O_3 layer was deposited by atomic layer deposition (ALD) using H_2O and TMA at 250 °C as gate dielectric. Gate metal (molybdenum) was sputtered immediately after ALD. In VFETs, the current flows vertically through submicrometer channels formed by carrier accumulation at the oxide/GaN interface; the cross section of one-channel device is shown in **Figure 5**a. The channel electron density simulations at different gate voltage are shown in Figure 5b.[73] Below the threshold voltage ($V_{GS} = 0\,V < 1\,V$), the device is in the off-state and the channel is depleted. For gate voltages higher than the threshold, the channel is fully formed, and the electron density peaks at the Al_2O_3/GaN interface, and in the center of the GaN layer it becomes equal to the dopant concentration. The VFET structure consists in the repetition of gate–GaN channel–gate modules in which multiple channels operate in parallel to obtain sufficient current.

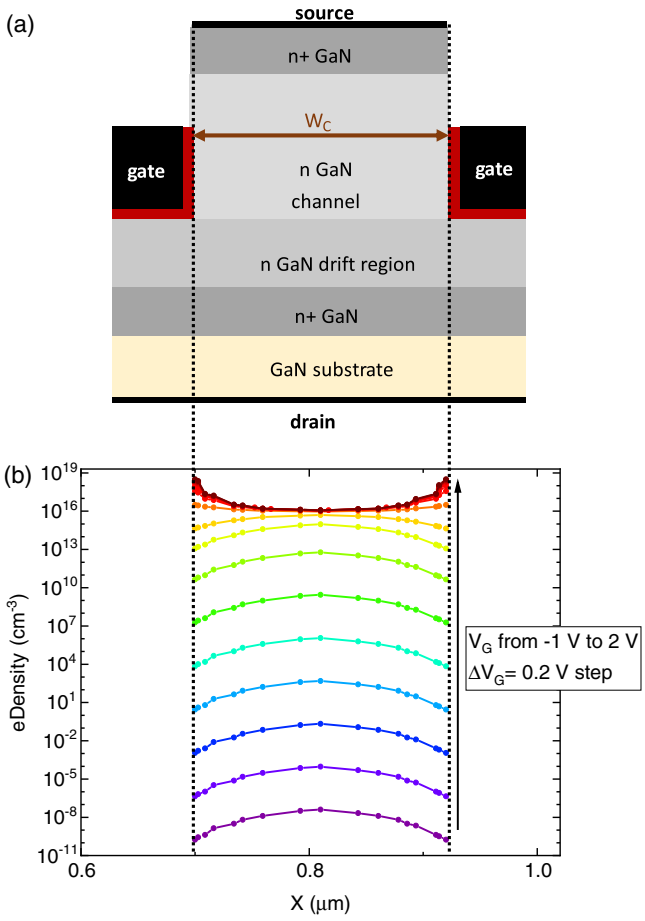

Figure 5. Simulation of electron density in a VFET for different gate voltages.

4.1. Instability of Threshold Voltage in GaN-on-GaN Vertical FETs Submitted to Positive Gate Bias

In ref. [73], the first analysis on the dynamic performance and on the gate stability of these devices has been reported. To study trapping effects on the dynamic parameters of the devices, double pulses have been applied to the drain and gate terminals starting from a trapping condition (positive gate voltage and zero drain bias) to a measurement condition to monitor the variation in the on-resistance and threshold voltage. The results are shown in **Figure 6**. When VFETs are subjected to pulsed positive gate bias, the on-resistance slightly decreases due to a change in the interface scattering (not reported here): R_{on} is determined by both carrier concentration and carrier mobility; when the device is submitted to positive V_G, the trapped charge may change the total interface scattering, thus increasing the mobility near the interface.[95] In addition, the devices show a negative threshold voltage shift for low positive gate bias ($0\,V < V_{GS} \leq 2\,V$), while for high trapping bias ($V_{GS} \geq 3\,V$) a positive shift of the threshold voltage is observed. At low gate bias, the negative threshold voltage shift is ascribed to the detrapping of electrons from the Al_2O_3 insulator (see mechanism 1 in **Figure 7**a); on the contrary, high gate voltages induce the injection of electrons from the accumulation region (channel) toward the dielectric, leading to a positive shift of the threshold voltage (see mechanism 2 in Figure 7a,b).

The stability of VFETs was investigated by $I_D V_D$ and fast $I_D V_G$ measurements performed during a constant voltage stress test of 100 s at different $V_{Gstress}$, followed by 100 s of recovery with gate, source, and drain terminals at 0 V. With positive gate bias, the on-resistance decreases in time and the threshold voltage shows a fully recoverable negative shift for low gate voltages, and a positive shift (nonrecoverable in thousands of seconds) for higher gate voltages (>3 V). The gate leakage at low and high gate bias for 100 s has been monitored to confirm the hypotheses: the gate leakage becomes relevant only at high gate voltages. The positive threshold voltage shift is correlated with the gate leakage (injection of electrons from the channel toward the insulator) and the mechanism has a slow recovery time.

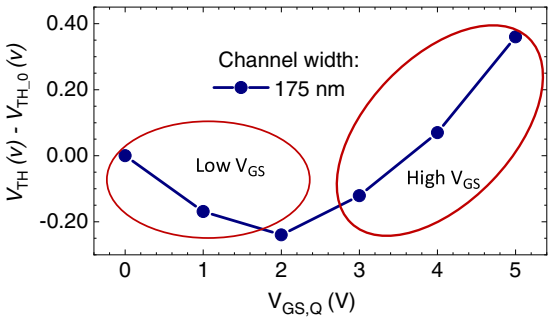

Figure 6. Variation of the threshold voltage as obtained from pulsed $I_D V_G$ performed for different trapping conditions at $V_{GS,Q} = 0$ V, 1 V, 2 V, 3 V, 4 V, 5 V; $V_{DS,Q} = 0$ V. The threshold voltage has an initial negative shift for low gate voltage ($V_{GS} < 2$ V), then a positive shift for higher gate voltages.

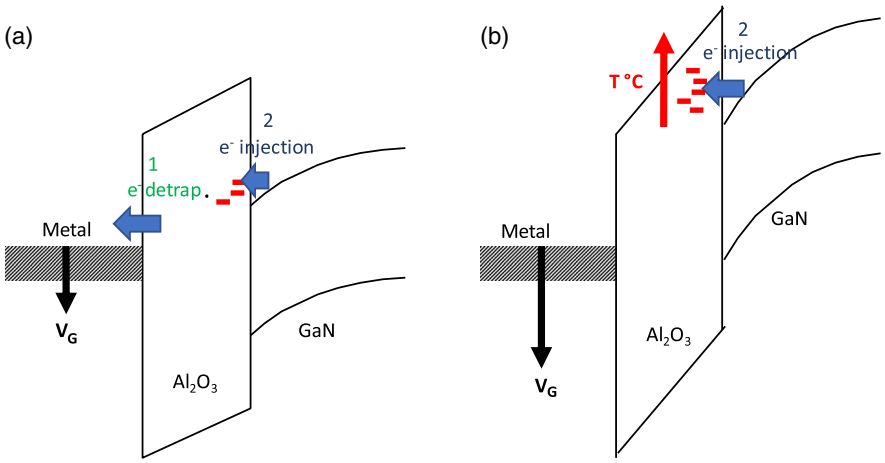

Figure 7. Pictorial representation of the trapping mechanisms under positive gate bias: a) mechanism 1: at low gate bias, electrons already trapped inside the insulator are detrapped leading to a negative shift of the threshold voltage; mechanism 2: electrons in the channel are injected towards the insulator. b) At high gate bias, mechanism 2 is dominant. Two factors contribute to the second mechanism: the high gate bias, i.e., the strong band bending, and the high temperature (high electron energy).

Constant voltage stress tests were conducted at different temperatures (25, 50, and 75 °C) to study the effect of the temperature on the trapping–detrapping kinetics. At low stress voltages ($V_{GS} \leq 2$ V), temperature does not significantly affect the trapping kinetics, confirming that the negative threshold shift is ascribed to an electrostatic process (emission of electrons from insulator to metal). On the contrary, at high gate bias ($V_{GS} \geq 3$ V), the total gate current increases with temperature. In conclusion, both the gate voltage (stronger band bending) and the high temperature (increase in the average energy of electrons in the channel) favor the injection of carriers toward the insulator (see Figure 7b).

An extensive analysis of the mechanism 2 (see Figure 7) occurring at high positive gate voltage is reported in the previous study.[76] This mechanism is observable for longer stress times, and it is predominant for higher voltages (see **Figure 8**). Moreover, mechanism 2 is found to be recoverable only when the device is exposed to UV light (see **Figure 9**). A possible explanation is that electrons trapped in a specific level in the oxide acquire the energy necessary to be detrapped and reach the n-type GaN,[76,96] through hopping. Another possibility is that under UV light the recovery is assisted by the holes accumulated at the Al_2O_3/GaN interface. The UV exposure induces a negative shift of the threshold voltage by increasing the conductive electrons either by electron detrapping from oxide or by generation of carriers, in good agreement to previous reports on different MOS structures.[97,98] The instability of the threshold voltage in VFETs is correlated with the presence of interface states. To quantify the interface states, the changes in the gate–source capacitance as a function of voltage in trapping and detrapping conditions have been evaluated.

Gate–source capacitance curves have been performed as a function of the gate voltage, after biasing the device in depletion under UV light (at −3 V) and accumulation (at 5 V). The *C–V* curve (**Figure 10**) performed after UV exposure in off-state (red line) shows a negative shift of the threshold voltage and a change in the slope at the turn-on in respect of the *C–V*

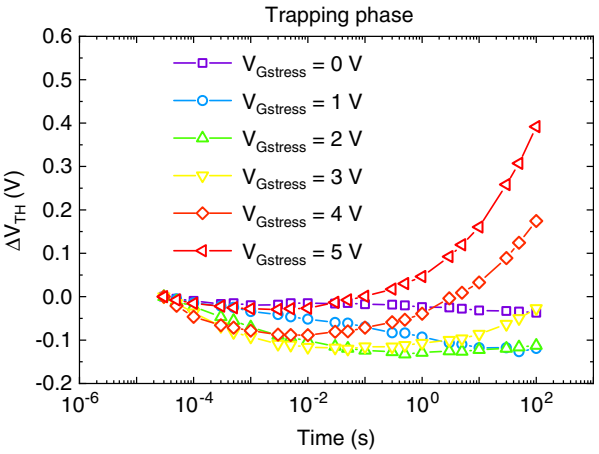

Figure 8. Threshold voltage transients during a constant bias experiment at different gate voltages and $V_{DS} = 0$ V. For short stress times, the negative shift is dominant, and then the second mechanism, i.e., trapping of electrons in the oxide, occurs (earlier for higher gate bias) leading to a positive shift of the threshold voltage.

performed after accumulation (black line). The rigid shift in *C–V* is ascribed to charges (oxide traps) that are not influenced by the electron quasi-Fermi level; the change in slope is ascribed to interface states, and can be used to calculate the amount of interface states that changed occupancy with V_G.[99] With this method, a peak interface state density of 4×10^{13} cm^{-3} eV^{-1} at $V_{GS} = 2$ V has been calculated.

4.2. Degradation of Vertical GaN-on-GaN Fin Transistors under Positive Gate or High-Drain Stress

To evaluate the robustness of GaN-on-GaN fin transistors, we conducted step stress experiments; the devices were submitted to a forward gate voltage for 120 s with drain and source biased

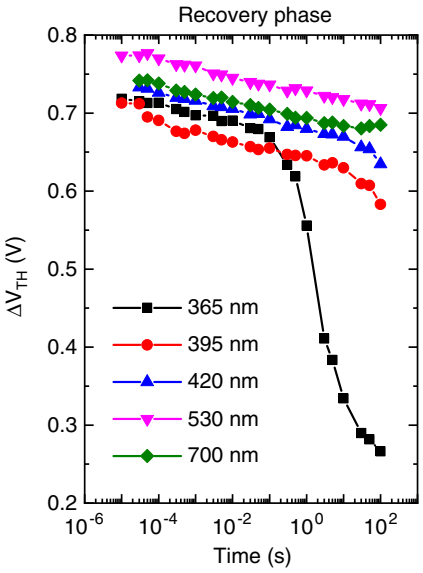

Figure 9. Threshold voltage transients performed during a recovery phase under LED light at different wavelengths, after stress at $V_{GS} = 4$ V: a strong recovery is observed only when the device is illuminated with UV light at 365 nm (corresponding to energy gap of GaN).

to 0 V, then the gate voltage was sequentially increased by 0.25 V/step, and the device transfer characteristics were monitored at each step. With this technique it is possible to investigate the mechanisms that lead the device to failure. The results of the step stress are shown in **Figure 11**: the gate current monitored during the stress increases at each step of stress, and for $V_{GS} = 7.25$ V an abrupt increase of more than 4 decades is observed due to the dielectric breakdown. From the plot of the $I_D V_G$ in semilogarithmic scale (**Figure 12**), a positive shift of the threshold voltage is observed for low stress voltages (in good agreement with the previous work[73]). Moreover, the positive gate bias induces a significant increase of subthreshold slope

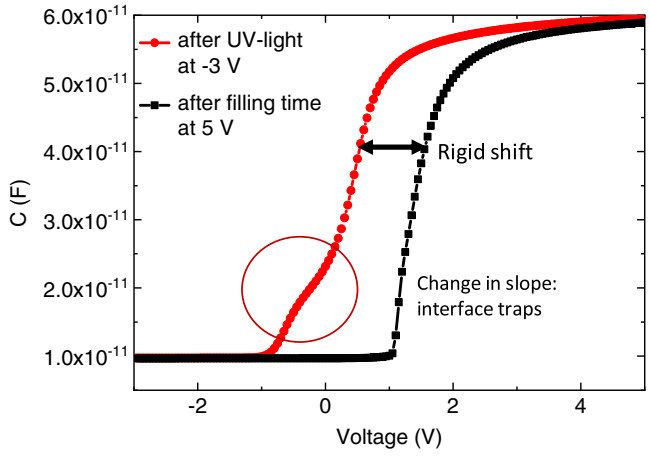

Figure 10. Gate–source capacitance plots measured on a VFET with a channel width of 125 nm by sweeping the gate voltage from −3 to 5 V after illuminating the device with UV light and from 5 to −3 V after biasing the device at 5 V in dark condition for 1000 s.

at $I_{DS} = 10^{-3}$ A cm^{-2}. This can be explained by considering another mechanism (mechanism 3 in Figure 12): at very high gate stress voltages (up to 7.75 V), the electrons injected from the channel to the insulator may promote the generation of traps. Electron traps are depleted during stress, thus giving higher current at turn-on and an increase in subthreshold slope.

We also investigated the prolonged stress under positive gate bias on VFETs with different gate width.[74] To analyze the degradation mechanism responsible of the catastrophic failure when the VFETs are submitted to positive gate bias, step stress tests have been performed. It is demonstrated that the trend of gate current during stress depends on the gate voltage (**Figure 13**). For low gate voltages (up to $V_{Gstress} = 0.5$ V), the gate current slightly decreases during stress. In this range of voltages, the mechanisms 1 (detrapping of electrons) and 2 (injection of electron from the accumulation channel to the oxide) occur simultaneously and the fact that one of the two dominates (increasing or decreasing of the gate current) is device-dependent.

For higher gate voltages, mechanism 2 (see Figure 13) occurs, leading to a decrease in the gate current during each stage of the stress experiment: the newly trapped electrons have a repulsive action, preventing further electrons from being trapped in the oxide, thus inducing a decrease/stabilization in gate leakage. At $V_{Gstress} > 5.5$ V, the creation of percolation/shunt paths leads to the consequent breakdown of the dielectric.

Nine devices with 70 nm of channel width and eight devices with 280 nm were stressed at constant voltage ($V_{GS} = 5$ V) until failure. The degradation trend of the gate current shows an abrupt increase in the gate current due to a time-dependent defect generation/percolation through the oxide. The corresponding Weibull plots are shown in **Figure 14**: the failure rate decreases with time ($\beta < 1$) and this is in good agreement with the hypothesis of dielectric breakdown. 2D simulations (see **Figure 15**) indicate that the failure point is located at the corner of the insulator, where the electric field is maximum.

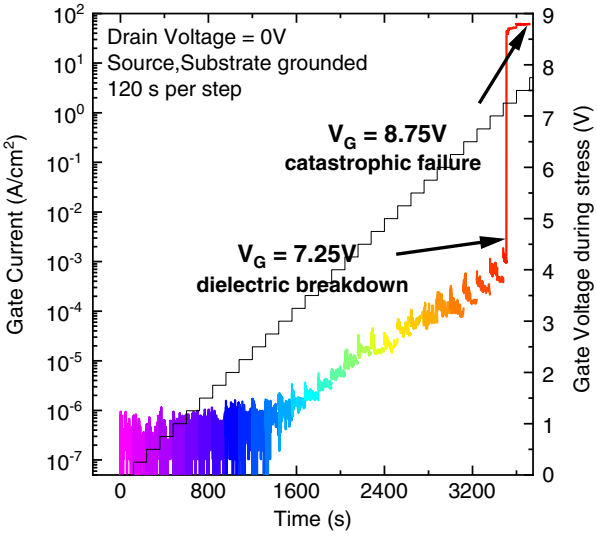

Figure 11. Step stress performed with $V_{Dstress} = 0$ V and by increasing the $V_{Gstress}$ by 0.25 V each 120 s of stress. The breakdown of the dielectric occurs at 7.25 V.

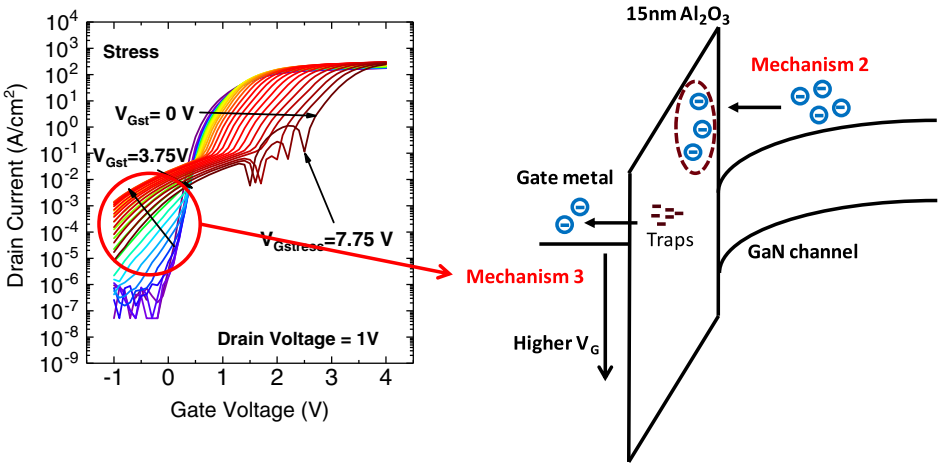

Figure 12. Stressing at increasing gate voltages induces an increase in the subthreshold slope due to trap generation in the oxide (left): traps are depleted during stress, thus giving higher current near turn-on (right).

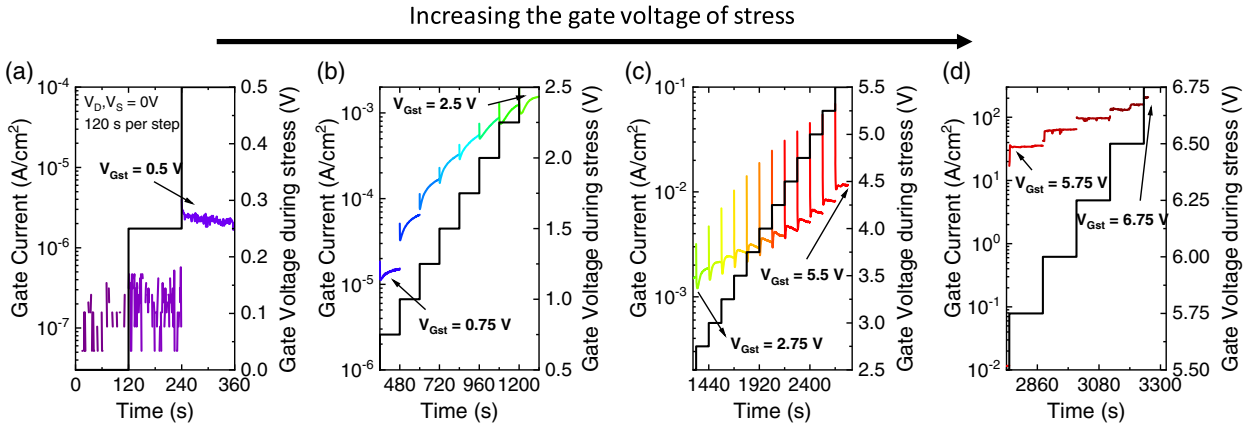

Figure 13. Trend of the gate current for each step of the gate stress on one of the analyzed VFETs. a) At $V_{Gstress} = 0.5$ V, the gate current slight decreases during 120 s of stress due to slight trapping of electrons inside the insulator. b) For 0.75 V $< V_{Gstress} <$ 2.5 V, a fast initial decrease followed by a slow increase of the gate current is observed. c) For 2.75 V $< V_{Gstress} <$ 4.5 V, the gate current starts to decrease at long stress times. d) For $V_{Gstress} >$ 5.5 V, percolation/shunt paths have been created leading to the breakdown of the dielectric.

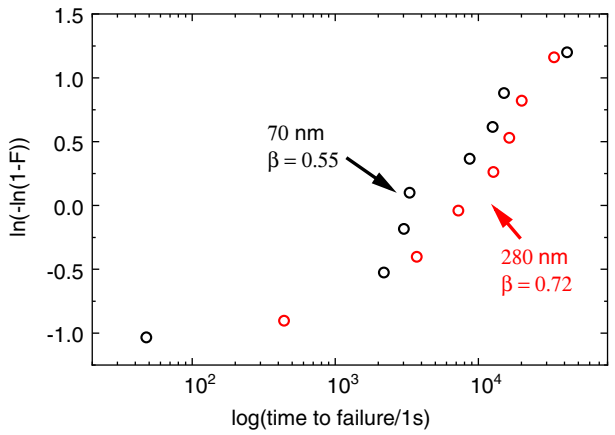

Figure 14. Comparison of the Weibull plots at 99% of confidence level for VFETs with 70 nm channel (black curve) and 280 nm channel (red curve).

The degradation of VFETs under high drain voltage has also been investigated.[75] The device was submitted to a step stress test in which the drain voltage has been increased by 20 V every 120 s, with $V_{GS} = 0$ V. At the end of each step, a DC characterization was performed. The results are shown in **Figure 16**: a small positive V_{TH} shift and negligible variations in on-resistance are induced by high drain bias. The VFET shows a good stability up to 280 V (the device under test is optimized for 200 V operation).

Ruzzarin et al.[74] reported the analysis of the degradation process that occurs when the VFETs are submitted to high drain voltage in off-state ($V_{GS} = 0$ V). The gate current has been monitored during a constant voltage stress experiments at 300 V: a catastrophic failure was reached after 2 h of stress, and consists in a rapid increase in the gate leakage current. By means of 2D simulations of the electric field within the device submitted to high drain voltage, the peak of the electric field was found again to be located at the edge of the gate.

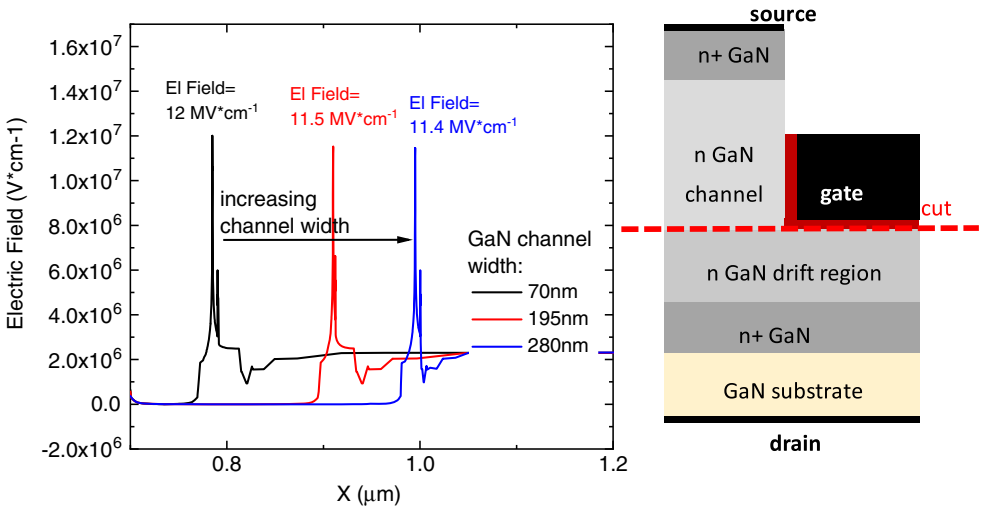

Figure 15. Simulation of the electric field when the device is at 5 V. The peak of the electric field is located at the corner of the dielectric independently of the channel width. Devices with shorter channel width have higher peak of the electric field. Values of the field may be overestimated due to the fact that square corners were used in the simulations.

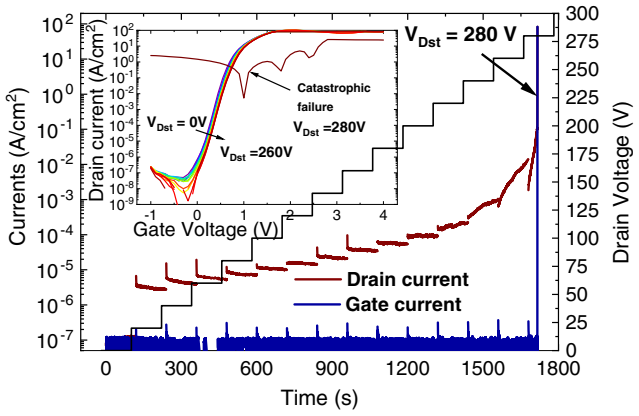

Figure 16. Gate and drain currents measured during the step stress at high drain voltage. Inset: $I_D V_G$ performed at each step of the drain step stress.

5. Conclusions

In conclusions, we have summarized recent case studies in the field of GaN vertical power devices. The results indicate the existence of a set of degradation processes that do not constitute fundamental limits, and can be solved through a careful optimization of device structure. The study of GaN vertical devices is still at the early phase: a significant progress in this field will be possible through extensive research, and will open the way to this revolutionary technology.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

defects, degradation, GaN, reliability, vertical

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