GaN/AlN p-channel HFETs with I_{max} >420 mA/mm and ~20 GHz f_T / f_{MAX}

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***Abstract*—**A strong need exists for a wide-bandgap p-type transistor counterpart of the n-channel GaN HEMTs for power electronics and novel RF circuits. In this work, the first p-channel nitride transistors that break the GHz speed barrier are demonstrated. By leveraging the unique single-channel high-density polarization-induced 2D hole gas of the GaN/AlN heterostructure, best-in-class contact resistances, and scaled T-gate design, p-channel transistor on-currents of 428 mA/mm are observed, with cutoff frequencies in the 20 GHz regime. These observations demonstrate the unique enabling role of the polarization discontinuity at the GaN/AlN semiconductor heterojunction and offer significant hope for a new high-speed and high-voltage wide-bandgap CMOS device platform for applications in RF and power electronics domains.

I. Introduction

The polarization-induced high-density 2D electron gas (2DEG) at Al(Ga,In)N/GaN heterojunctions exhibits excellent electron mobility in a wide-bandgap semiconductor channel. The combination of high mobility, high 2DEG density, and capability to handle high voltages makes GaN HEMTs very attractive for generating high powers at RF and mm-wave frequencies [1], in addition to high-speed switching of large voltages for efficient energy conversion. A p-channel transistor counterpart has proven far more difficult but holds much promise for several novel applications ranging from active loads for wide-bandwidth amplifiers, to power digital to analog convertors (DACs) and digital power amplifiers (PAs) to ease impedance matching and power combining.

The recent discovery of a very high-density polarization-induced 2D hole gas (2DHG) at the GaN/AlN interface [2] led to the demonstration of p-channel heterostructure field-effect transistors (HFETs) that hit the 100 mA/mm mark [3]. In this work, it is shown that, on the same material platform, when the source/drain distance and the gate length are scaled, low resistance ohmic contacts enable Schottky-gate p-channel GaN HFETs reach on currents >420 mA/mm and f_T/f_{MAX} ~20 GHz.

II. Materials Growth

The realization of the nitride p-channel HFETs starts with the growth of the GaN/AlN epitaxial layers using plasma-assisted molecular beam epitaxy (MBE) on Al-polar AlN/Sapphire templates [**Fig. 1(a)**]. The epitaxial stack consists of a ~500 nm AlN buffer, a ~15 nm undoped GaN layer, and a ~15 nm heavily Mg-doped ([Mg] $>5\times10^{19}$ cm^{-3}) ~5% InGaN layer. A high-density 2DHG is induced by the polarization-discontinuity at the GaN/AlN interface, and is quantum-confined in the GaN layer by the GaN/AlN valence band offset and high polarization fields. The InGaN layer primarily enables low-resistance ohmic contacts, with the secondary benefit of enhancing the polarization-induced 2DHG by absorbing the surface depletion. The energy band diagram in **Figure 1(b)** shows the expected location of the polarization-induced 2DHG, with sheet density of ~5-6$\times10^{13}$ cm^{-2} and hole mobilities ranging from 10-20 $cm^2/V\cdot s$ at room temperature [2]. **Figure 1(c)** shows the crystal structure of the semiconductor heterostructure, highlighting the discontinuity in the combined (spontaneous + piezoelectric) polarization across the heterointerface, and the creation of a negative polarization fixed sheet charge, which generates the positive mobile hole gas. The mechanism of formation of the 2DHG is the valence-band analogue of what enables the 2DEG in n-channel III-nitride HFETs. The 2DHG is observed to be present across the entire 2-inch wafer, with sheet resistances ranging in ~9-25 kΩ/sq as shown in **Fig. 1 (d)**, and roughly 80% of the wafer in the ~10-15 kΩ/sq range.

III. Device Fabrication

Diced 8 mm × 8 mm pieces from the epitaxial wafer were used for the fabrication of the transistors. **Figure 2** shows the process flow for the fabrication of the GaN/AlN p-channel HFETs. First, Pd/Au/Ni ohmic contacts are formed, followed by mesa isolation into the AlN substrate, followed by a global recess etch where the InGaN layer is removed from all regions except under the ohmic pads, with a slight overetch into the UID GaN layer. A further gate-specific recess, defined by electron beam lithography (EBL), tunes the local GaN thickness to roughly 8 nm. Standard Mo/Au gates are defined by optical lithography down to 0.6 µm, while shorter T-gates are defined by EBL. The completed device dimensions achieved are shown in the table in **Fig. 2**, which also shows the completed SEM images of the completed HFETs and a close-up of the EBL gate of ~120 nm length.

IV. Device Results And Discussion

Figure 3 shows the electrical properties of the ohmic contacts of the processed device. The current flow and resistance is compared for the cases before and after the removal of the InGaN contact layer from areas not under the metal pad, the structure of which is indicated in **Fig 3(a)**.

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The low-bias current is only barely lower after the removal of the InGaN layer as seen in **Fig 3(b)**, and the contact resistance is nearly identical for both cases at very low currents as seen in **Figs 3(c)** and **3(d)**. But with increasing current injection, the contact resistance falls, especially for the structure with the InGaN layer removed. The measured R_c drops from ~9 Ω·mm to below 1 Ω·mm when the current exceeds 100 mA/mm. Prior to the recess etch, the specific contact resistance is found to approach ~10^{-6} Ω·cm^2 at ~200 mA/mm. These are among the lowest contact resistances measured in the GaN p-channel platform and are directly responsible for the high performance of the devices.

Figure 4(a) shows the measured output characteristics of the p-channel HFETs of 120 nm gate length, and 680 nm source-drain distance. The saturated on-current reaches 428 mA/mm, and repeatable current saturation, pinch-off, and similar performance is measured for several devices of similar size. **Figure 4(b)** shows the transfer characteristics of the Schottky-gated p-channel HFETs, which exhibit an on/off ratio of ~10^2. Since this is limited by the gate leakage of the Schottky diode, addition of a very thin insulator in the future can significantly enhance this ratio [4]. **Figure 4(c)** shows the threshold voltage of ~4 V and a peak $g_{m,ext}$ of ~66 mS/mm, all at room temperature.

Figure 5 shows how the p-channel HFET performance metrics scale with the gate lengths and the source/drain distance and compare it to several prior embodiments of p-channel GaN transistors. The maximum on currents in this study are found to roughly follow the classic ~$1/L_g$ scaling law. Shorter gate lengths also show lower leakage, and make a strong case for an insulating barrier in the future.

Figure 6(a) shows the measured small signal RF current gain $|h_{21}|^2$, unilateral gain U, and maximum stable gain/maximum available gain (*MSG/MAG*) after de-embedding. The measurement is performed using microwave wafer probes in ambient air. For RF characterization, scattering parameters are measured from 50 MHz to 40 GHz. The measurements are calibrated using short, open, load, and through (SOLT) impedance standards on an alumina substrate. The parasitics are de-embedded using an open structure on the same chip as the p-channel HFETs. After de-embedding, f_T and f_{MAX} are extracted from the frequency where the current gain $|h_{21}|^2$ and unilateral gain U drop to 0 dB, respectively. In both cases, the gain exhibits a -20 dB/dec slope. The f_{MAX} extracted from U and *MSG/MAG* are consistent. The f_T /f_{MAX} of 19.7/23.3 GHz are obtained at V_{gs} = 0 V and V_{ds}= -10 V after de-embedding. In comparison, neglecting the open de-embedding test structure renders f_T/f_{MAX} values of 11.5/22.5 GHz. **Figure 6 (b)** shows the measured and modeled S parameters after de-embedding from 0.05 to 40.05 GHz at V_{gs}= 0 V and V_{ds}= -10 V. The small signal circuit schematic and parameters used in the model are shown in **Fig. 7**. The extracted small signal $g_{m,int}$ is 74 mS/mm, compared to the measured DC value of $g_{m,ext}$= 66 mS/mm. Benefiting from the T-gate, a small gate resistance R_G of 3.4 Ω (68 Ω/mm) is achieved which helps boost f_{MAX}. Compared with conventional 2DEG HEMTs, the source and drain resistances R_S and R_D of the p-channel HFETs are an order of magnitude higher (~ 1.0 vs. 0.1 Ω·mm) for similar geometry [18]. Larger cutoff frequencies are thus expected by reducing these resistances. **Figure 6 (c, d)** show the bias-dependence heat maps of the f_T/f_{MAX} values extracted in the same manner as **Fig 6 (a)** at various V_{gs} and V_{ds}. The symbols in these maps are the biasing conditions during the RF measurements. The heat maps vividly indicate that the highest RF performance of the p-channel HFETs is achieved at an on-current of ~-100 mA/mm and V_{ds} ~ -10 V.

Figure 8 shows how the wide-bandgap p-channel HFETs discussed in this work compare to earlier reports [3-17] of p-channel transistors in the nitride family. Though still short of the n-channel counterparts, applications in both the analog RF domain as well as power electronics stand to benefit significantly with the performance levels GaN p-channel HFETs are capable of.

V. Conclusion

The scaling of the p-channel GaN HFET with optimal contacts has helped achieve a 4× higher performance than the last generation and marks the first Nitride p-channel transistor that breaks the GHz speed barrier. The increased drive current and speed of the p-HFETs seen here in the AlN/GaN platform, combined with the excellent performance of the n-HFETs on the same platform [19] is expected to take this wide-bandgap CMOS platform into new application domains in the RF and power electronics arenas [20].

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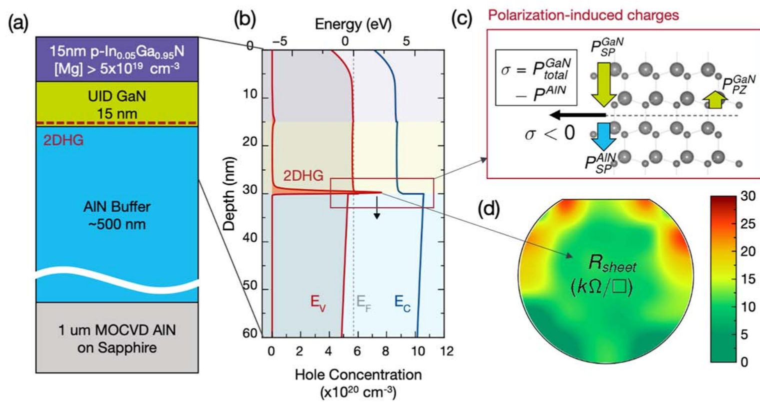
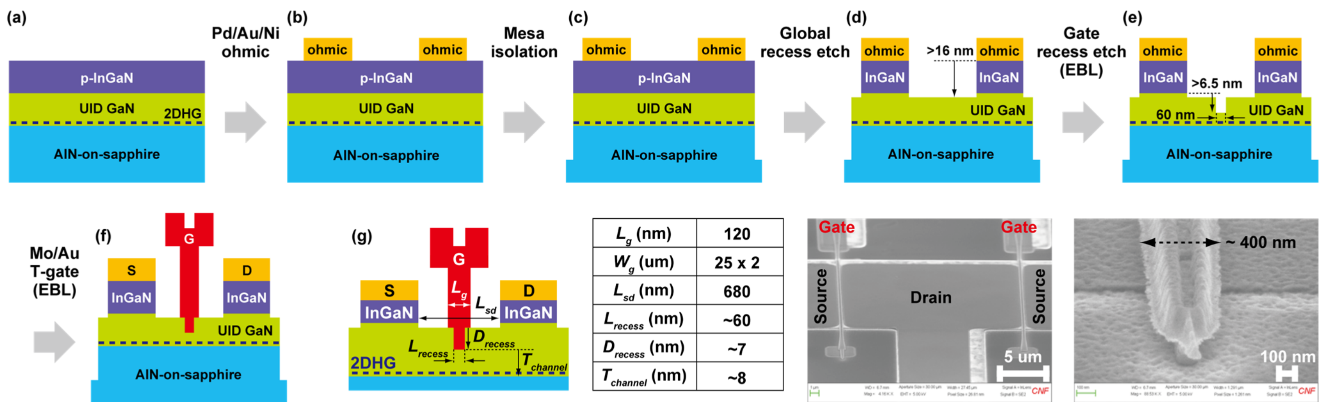


Fig. 1. (a) Layer structure of the epitaxial film grown by MBE, dashed line indicating where a high-density 2D hole gas (2DHG) is present. (b) Energy band-diagram showing the band alignment at the interface and the 2DHG. (c) Polarization difference at the undoped GaN/AlN interface gives rise to fixed negative sheet charges, which together with a valence band offset between the GaN and AlN, leads to a tightly-confined mobile 2DHG channel. (d) The sheet resistance map shows the uniformity of the 2DHG across the MBE-grown 2 inch wafer, pieces of which were used for fabricating the devices in this work.



L_g (nm)	120
W_g (um)	25 x 2
L_{sd} (nm)	680
L_{recess} (nm)	~60
D_{recess} (nm)	~7
$T_{channel}$ (nm)	~8

Fig. 2. Scaled-device process overview include (a) MBE grown GaN/AlN heterostructure with the Mg-doped $In_{0.05}Ga_{0.95}N$ layer, (b) non-alloyed Pd/Au/Ni ohmics, (c) Cl_2-based ICP etching for mesa isolation , (d) first recess etch step for removing p-InGaN, (e) 2nd recess etch with electron-beam lithography (EBL) to thin the gate-channel distance, and (f) Mo/Au Schottky T-gate. (g) Enlarged cross-sectional schematic of the device structure with the T-gate of L_g= 120 nm , W_g= 25 µm × 2. Finally, 70° angled-view SEM images of the fabricated p-HFETs and T-gate.

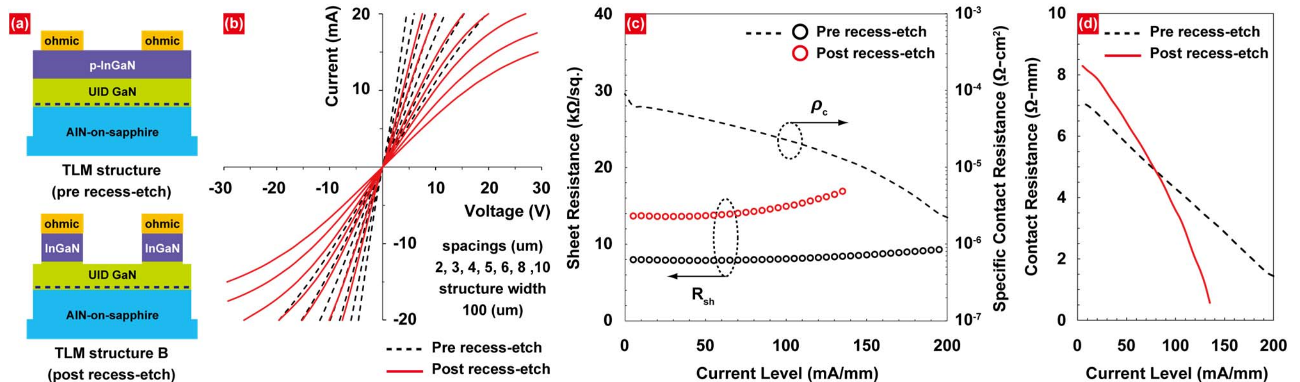


Fig. 3. (a) TLM test structures of pre recess-etch and post recess-etch for removing the top p-InGaN contact layer. (b) Linear TLM *I-V* of representative non-alloyed Pd/Au/Ni ohmic contacts to the Mg-doped $In_{0.05}Ga_{0.95}N$, and (c) sheet resistances and (c) specific contact resistances and (d) contact resistances versus current level showing highly conductive but imperfectly ohmic behavior. Note that the specific contact resistance ρ_c on the post recess-etch TLM structure is not plotted since it can't be reliably extracted in TLM structures with unequal sheet resistances under the metal contacts and between the metal contacts.

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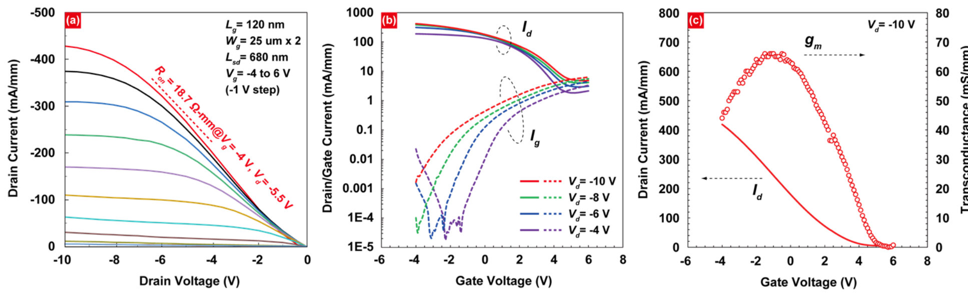

Fig. 4. Transistor characteristics of the p-channel HFETs with L_g= 120 nm, W_g= 25 μm × 2, and L_{sd}= 680 nm. (a) Output *I-V* curves show current saturation and an on-resistance of 18.6 Ω·mm at V_g= -4 V. (b) Log-scale transfer curves show two orders of I_{on}/I_{off} modulation, limited by Schottky gate leakage. (c) The linear-scale transfer curve shows normally-on operation and a peak $g_{m,ext}$ of 66 mS/mm.

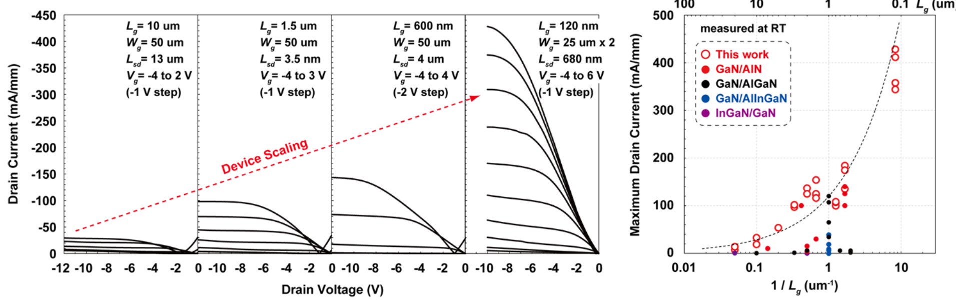

Fig. 5 Device scaling characteristics, and maximum drain current I_{dMAX} versus gate length L_g for scaled GaN/AlN p-channel HFETs.

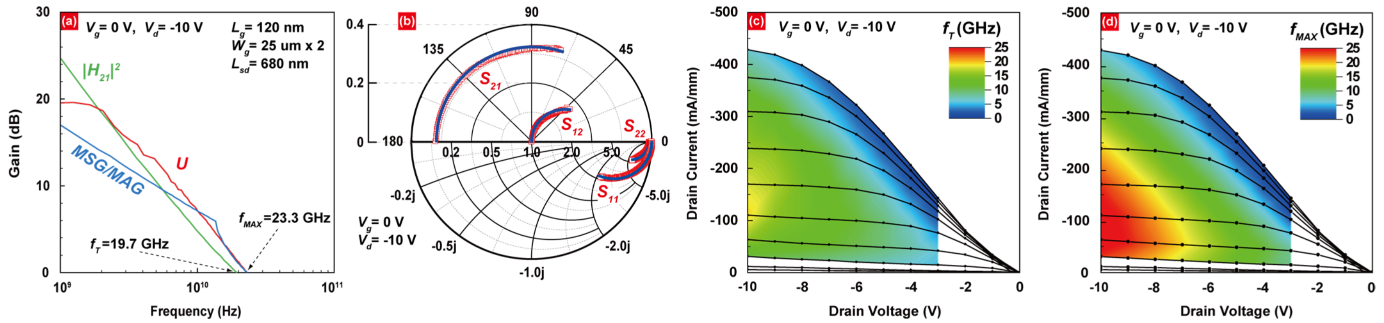

Fig. 6. Small-signal measurements on the p-channel HFETs with L_g= 120 nm, W_g= 25 μm × 2, and L_{sd}= 680 nm. (a) Cutoff frequencies measured on the GaN/AlN p-channel HFETs with f_T/f_{MAX}= 19.7/23.3 GHz. (b) Measured (symbols) and modelled (lines) S-parameters of the p-HFET at V_{gs} = 0 V and V_{ds} = -10 V. V_{ds} and V_{gs} bias dependence of (c) f_T and (d) f_{MAX} extracted from *U*. The colors indicate frequencies on the contour maps.

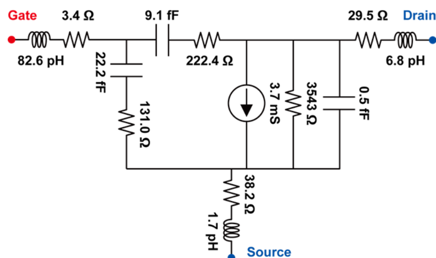

Fig. 7. Small-signal equivalent-circuit model of p-channel HFETs shown in Fig. 6 under V_{gs} = 0 V and V_{ds} = -10 V.

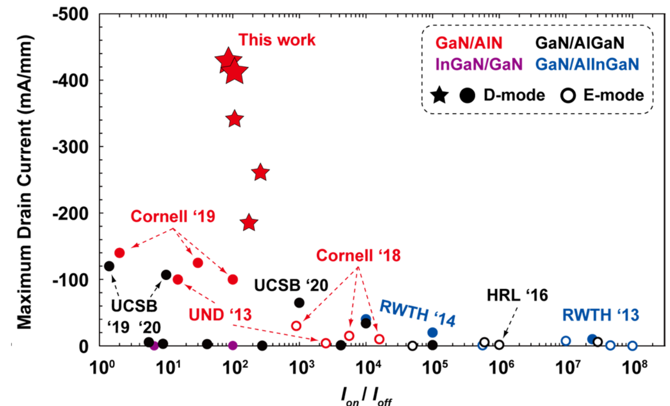

Fig. 8. Benchmark of III-Nitride p-channel FETs from [3-17], and this work (★). Filled-circles are depletion-mode FETs and hollow circles are enhancement-mode FETs. Filled (●) and hollow (○) red circles represent our previous results with GaN/AlN p-channel HFETs.

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