SiC Substrate-Integrated Waveguides for High-Power Monolithic Integrated Circuits Above 110 GHz

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***Abstract*—Substrate-integrated waveguides (SIWs) of different geometry are designed, fabricated, and measured on a SiC wafer, along with SIW-based resonators, SIW-based filters, grounded coplanar waveguides (GCPWs), GCPW-SIW transitions, and calibration structures. Two-tier calibration is used to extract the intrinsic SIW characteristics from GCPW-probed scattering parameters. The resulted D-band (110–170 GHz) SIWs exhibit a record low insertion loss of 0.22 ± 0.04 dB/mm, which is four times better than that of the GCPWs. A 3-pole filter exhibits a 1.0-dB insertion loss and a 25-dB return loss at 135 GHz, which represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. These results show the promise of SIWs for integrating HEMTs, filters, antennas, and other circuit elements on the same SiC chip.**

***Keywords*—cavity resonators, microwave filters, millimeter wave integrated circuits, semiconductor waveguides**

I. Introduction

Conventional microwave monolithic integrated circuits (MMICs) are based on coplanar or microstrip transmission lines, which suffer from high loss, significant crosstalk, and limited power capacity at frequencies above 110 GHz. By contrast, substrate-integrated waveguides (SIWs) [1], [2] have low loss, minimum crosstalk, and high power capacity. However, because the size of SIWs is on the order of the propagation wavelength λ, SIWs are usually implemented at the board level for hybrid integration. Monolithic integration becomes feasible only when the operation frequency exceeds 110 GHz, so that λ < 1 mm in a typical semiconductor such as Si. In the case of high-power GaN-on-SiC MMICs, SIWs are especially attractive because SiC is high in dielectric constant, electrical resistivity, breakdown strength, mechanical toughness, and thermal conductivity, but low in loss tangent and thermal expansion coefficient [3]–[6].

Despite the attractiveness of SIWs, to date there are few reports of SIWs above 110 GHz on Si [7]–[11] or SiC [12], [13]. In this paper, we demonstrate D-band (110–170 GHz) SiC SIWs with an insertion loss of 0.22 ± 0.04 dB/mm. Also fabricated on the same wafer is a 3-pole SIW filter with a 1.0-dB insertion loss and a 25-dB return loss at 135 GHz. These record performances (Table I and Table II) make SIW promising for monolithic integration of high-quality SIW filters, edge-firing SIW antennas [14], and GaN HEMTs [15] (Fig. 1).

Table 1. Substrate-integrated waveguides above 110 GHz

Year	Sub-strate	Bandwidth (GHz)	Insertion Loss (dB/mm) [a]	Return Loss (dB) [b]	Reference
2010	Si	95–200	4–6	>14	[7]
2012	Si	150–210	2–3	>16	[8]
2018	Si	110–170	0.4–0.6	>14	[9]
2020	Si	243–325	0.4–1.0	>17	[10]
2017	SiC	160–220	0.4–0.7		[12]
2019	SiC	150–220	0.5–1.2		[13]
2021	SiC	110–170	0.32±0.06 [c]	>17	This Work

[a] Normalized by the SIW length plus the length of two GCPW-SIW transitions
[b] For the SIW plus two GCPW-SIW transitions
[c] 0.22±0.04 dB/mm after transitions are de-embedded by two-tier calibration

Table 2. > 110 GHz filers based on substrate-integrated waveguides

Year	Sub-strate	Freq. (GHz)	Insertion Loss (dB) [a]	Return Loss (dB) [a]	Band-width	Reference
2020	Si	279	9	20	1%	[10]
2020	Si	140, 280	3.9, 2.5	17, 11	10%	[11]
2017	SiC	183	~1	18	5%	[12]
2021	SiC	135	1.0	25	11%	This Work

[a] For the SIW plus two GCPW-SIW transitions

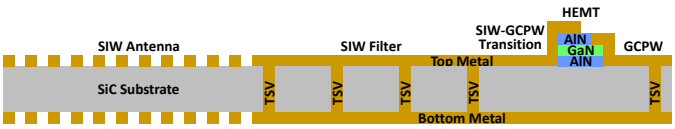
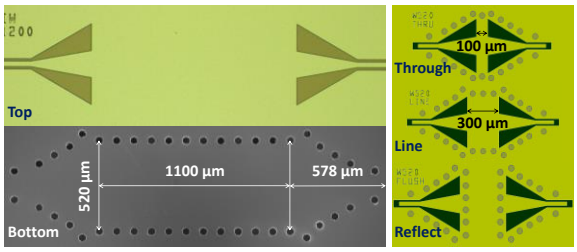


Fig. 1. Schematics of an MMIC with an edge-firing SIW antenna, an SIW filter, and a GaN HEMT on the same SiC chip.

II. Design, Fabrication, and Measurement

Guided by analytical equations [16] and numerical simulations (HFSS), D-band SIWs are designed, fabricated and measured on 100-µm-thick 6H-SiC wafers with > 10^6 Ω·cm resistivity. Each SIW has two parallel rows of through-substrate vias (TSVs) that are 40 µm in diameter and 100 µm apart center-to-center [Fig. 2(a)]. The rows are 520 µm apart center-to-center to cut off the fundamental TE_{10} mode below 110 GHz. Additionally, SIW resonators and filters of different geometry are designed (Fig. 3).



(a) (b)

Fig. 2. (a) Frontside and backside micrographs of an 1100-µm-long D-band SiC SIW between two 578-µm-long GCPW-SIW transitions. (b) Composite layout of SIW calibration structures "through," "line," and "reflect."

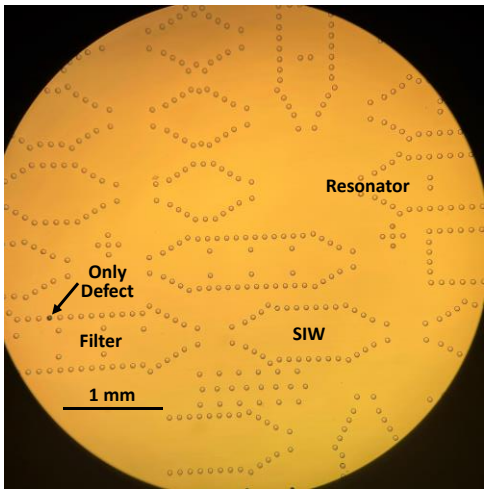


Fig. 3. Micrograph of the backside of a SiC wafer patterned with SIWs, filters, resonators, and calibration structures of different geometry.

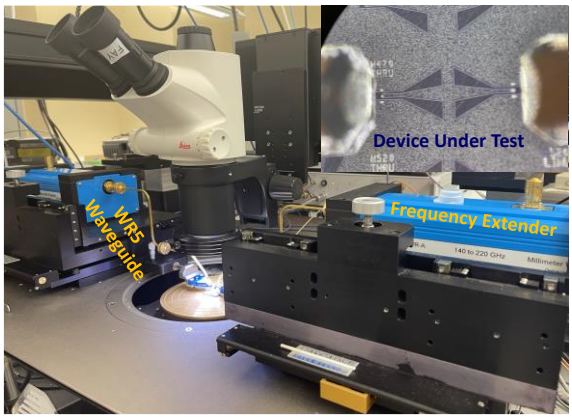


Fig. 4. Measurement setup based on a 67-GHz VNA, G-band frequency extenders, and wafer probes. Inset shows an SIW "through" under test.

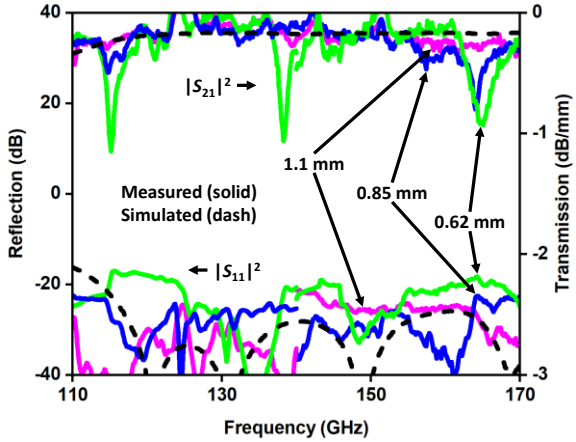


Fig. 5. Measured vs. simulated magnitudes of S_{11} and S_{21} for an SIW with a length of 620 µm, 860 µm, or 1100 µm. S_{21} is normalized by the SIW length.

To facilitate wafer probing, each SIW is transitioned [17], [18] to a grounded coplanar waveguide (GCPW) [19] at both the input and output. Each transition is 578-µm long, including a 175-µm GCPW section, a 353-µm tapered section, and a 50-µm SIW section [Fig. 2(a)]. In the GCPW section, the center electrode is 30-µm wide with a 16-µm gap from the ground electrodes. In the tapered section, the center electrode is linearly widened to 155 µm while the gap is linearly widened to 158 µm. To extract the intrinsic SIW characteristics, through-reflect-line (TRL) calibration structures [20], [21] are laid out [Fig. 2(b)] and fabricated on the same SiC wafer as the SIWs. Composite layouts are shown in Fig. 2(b) because they are more informative than chip micrographs as shown in Fig. 2(a).

Fabrication starts with frontside (Si face of SiC) metallization by 100-nm-thick Ni and 700-nm-thick Al, before the SiC wafer is flip-mounted on a sapphire carrier for TSV etching. Similar to [22], TSVs are etched in an Oxford PlasmaPro 100-380 COBRA inductively-coupled plasma etcher with 50-sccm SF_6 and 10-sccm O_2 under 10-mTorr pressure and cryogenic cooling. RF powers of 2000 W and 50 W at 2 MHz are applied to the plasma and substrate, respectively. The etch rate of SiC through a 5-µm-thick Ni mask is 15 µm/h with a 50:1 selectivity over Ni. Backside metallization consists of 100-nm-thick Ni and 2-µm-thick Al.

Lacking D-band frequency extenders, the fabricated SIWs are characterized by a Keysight E8361C VNA equipped with VDI F-band frequency extenders for 110–140 GHz and OML G-band frequency extenders for 140–170 GHz (Fig. 4). For each band, Formfactor Infinity probes with ground, signal, and ground tips at 50-µm pitch are used. Two-tier calibration is applied sequentially. Tier-1 calibration shifts reference planes from the VNA to the probe tips, using the load-reflect-reflect-match (LRRM) method [23] and a Formfactor 138-356 impedance-standard substrate. Tier-2 calibration shifts reference planes past the GCPW-SIW transitions to the intrinsic SIW section, using the TRL method and the calibration structures of Fig. 2(b). Despite stitching errors at 140 GHz, the general trend of the measured data is consistent with the simulated results across the D band.

III. Results and Discussion

Fig. 5 shows the measured and simulated magnitudes of the reflection and transmission coefficients, S_{11} and S_{21}, for an SIW length of 620 µm, 860 µm, or 1100 µm, with S_{21} normalized by the SIW length. (S_{22} and S_{12} are comparable to S_{11} and S_{21} and

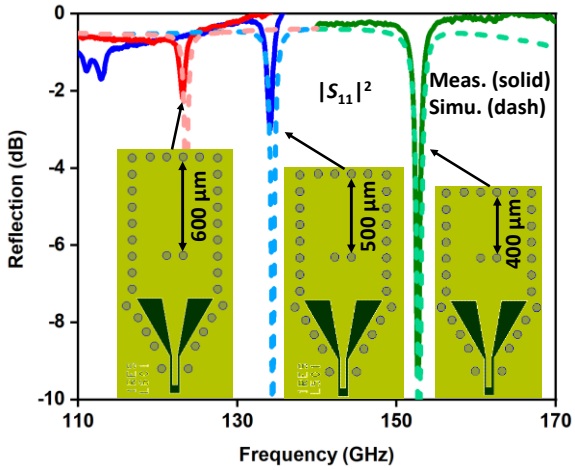


Fig. 6. Measured vs. simulated magnitude of S_{11} for one-port resonators comprising a GCPW-SIW transition and an SIW cavity 400-µm, 500-µm, or 600-µm long.

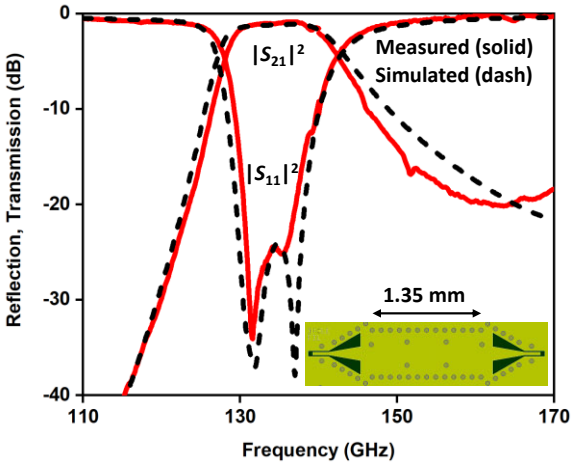


Fig. 7. Measured vs. simulated magnitudes of S_{11} and S_{21} for a three-pole SIW resonator.

hence, not shown.) Agreements are evident between measurement and simulation, and between different lengths. From 110 GHz to 170 GHz, the insertion loss is 0.22 ± 0.04 dB/mm and the return loss is greater than 17 dB. The insertion loss is four times lower than that of GCPWs fabricated on the same SiC wafer. Microstrip transmission lines would have even higher loss than GCPWs above 110 GHz [7]. The SIW loss could be further reduced by better metallization, as simulation indicates the loss is mainly in the conductor rather than the dielectric, in agreement with [8]. Presently, the GCPW section of the transition is too short to fully dissipate higher-order modes generated by the probe contact before they reach the tapered section. This results in ripples in S_{11} and S_{21} after the two-tier calibration. The ripples could be removed with a longer GCPW section at the expense of higher transition loss. In any case, it is challenging to measure an insertion loss as small as 0.2 dB and SIWs much longer than 1 mm should be used to more precisely characterize their insertion loss.

Apparently, others listed in Table I do not use two-tier calibration and include the loss and length of the transitions in their reports. In our case, with tier-1 calibration only to the probe tips and 578-µm-long GCPW-SIW transitions added to the 1100-µm-long SIW, the return loss is comparable but the insertion loss increases to 0.32 ± 0.06 dB/mm, indicating that the transitions are broadband and low loss (< 0.2 dB per transition). This insertion loss is listed in Table I to be consistent with others.

Fig. 6 shows the measured and simulated magnitude of S_{11} for one-port resonators each comprising a GCPW-SIW transition and an SIW cavity 400-µm, 500-µm, or 600-µm long. They resonate at 153 GHz, 134 GHz, and 123 GHz with an unloaded quality factor Q [24] of 210, 160, and 110, respectively. The 400-µm-long SIW cavity is equivalent to a parallel circuit of 27-Ω resistance, 0.14-pH inductance, and 8-pF capacitance. The high Q reflects the low loss of the SIW.

Fig. 7 shows the measured and simulated magnitudes of S_{11} and S_{21} for a three-pole filter comprising a 1.35-mm-long SIW and two GCPW-SIW transitions. The measured insertion and return losses are 1.0 dB and 25 dB, respectively, at the band center of 135 GHz. The 3-dB bandwidth is 15 GHz or 11%. The out-of-band rejection is greater than 40 dB and 20 dB below and above, respectively. These characteristics are consistent with the high-Q resonators and represent the state of the art of SiC SIW filters. They are order-of-magnitude better than that of Si on-chip filters. The rejection below band takes advantage of the SIW cutoff characteristics. The rejection above band can be improved by suppressing higher-order modes.

IV. Conclusion

D-band SiC SIWs, resonators, and filters are designed, fabricated, and measured. The SIWs, with a record low insertion loss of 0.22 ± 0.04 dB/mm, have four times lower loss than GCPWs fabricated on the same SiC wafer. The three-pole filter, with an insertion loss of 1.0 dB, represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. With further improvements, SIWs could be used to efficiently interconnect HEMTs, filters, antennas, and other circuit elements on the same SiC chip for high-power monolithic integrated circuits above 110 GHz.

The adaptation of SiC SIWs could be rapid, taking advantage of available technology. SiC substrates are commonly thinned down to 100 µm in high-power GaN MMICs to facilitate heat dissipation. TSVs similar to those in SIWs are commonly used to reduce the source inductance and are available in commercial GaN foundries [25]. Although TSVs in an SIW are of much higher density, wafer breakage is usually not an issue because SiC is mechanically tough. It can be seen in Fig. 3 that the TSVs are uniform, the yield is high, and the design is robust.

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