






Next generation electronics on the ultrawide-bandgap aluminum nitride platform

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Abstract

Gallium nitride high-electron-mobility transistors (GaN HEMTs) are at a point of rapid growth in defense (radar, SATCOM) and commercial (5G and beyond) industries. This growth also comes at a point at which the standard GaN heterostructures remain unoptimized for maximum performance. For this reason, we propose the shift to the aluminum nitride (AlN) platform. AlN allows for smarter, highly-scaled heterostructure design that will improve the output power and thermal management of III-nitride amplifiers. Beyond improvements over the incumbent amplifier technology, AlN will allow for a level of integration previously unachievable with GaN electronics. State-of-the-art high-current p-channel FETs, mature filter technology, and advanced waveguides, all monolithically integrated with an AlN/GaN/AlN HEMT, is made possible with AlN. It is on this new AlN platform that nitride electronics may maximize their full high-power, high-speed potential for mm-wave communication and high-power logic applications.

Keywords: aluminum nitride, gallium nitride, millimeter-wave, nitride CMOS, GaN HEMT

(Some figures may appear in color only in the online journal)

1. Introduction

As the wireless communication networks that connect our world push to ever-higher frequencies, the performance demand on radio frequency (RF) transistor technology amplifies. The need for higher power, frequency, and efficiency must also comply with the necessity for low cost and small footprint.

This strain of competing interests is perhaps highlighted best in the millimeter-wave (mm-wave) frequency range. The mm-wave spectrum is at a point of rapid growth and expansion in commercial and military application spaces. This is due to mm-wave's capability for high directionality and its short wavelength, which translates to faster data transmission ($>1 \text{ Gbit s}^{-1}$) and higher resolution imaging than lower frequency radio waves.

Many material platforms are vying for market share in this emerging frequency range. Silicon, bolstered by its maturity and cost-effective scale, has produced output powers up to 1 W in the sub-6 GHz regime with silicon lateral-diffusion metal-oxide-semiconductor (LDMOS) technology



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Table 1. Physical properties of relevant materials for high-power RF transistors.

Material	E_{gap} (eV)	E_C (MV cm ⁻¹)	μ (cm ² V · s ⁻¹)	v_{sat} ($\times 10^7$ cm s ⁻¹)	σ_{therm} (W cm · K) ⁻¹
Silicon	1.12	0.3	1440	1.0	1.3
InP	1.34	0.5	5400	3.9	0.68
GaAs	1.42	0.52	9400	0.9	0.55
GaN	3.4	3	1400	2.4	2.5
AlN	6.2	15	450	1.4	3.4
SiC	3.3	3	900	0.8	4.2

[1], but struggles at higher frequencies. Successful operation in the mm-wave frequency range has been achieved by gallium arsenide high-electron-mobility transistors (GaAs HEMTs) [2, 3], silicon germanium heterojunction bipolar transistors (SiGe HBTs) [4], and indium phosphide HBTs [5, 6], albeit at relatively low power levels. To achieve high-power and mm-wave operation simultaneously, focus has turned to gallium nitride (GaN) HEMTs. The relevant material properties of each material platform are shown in table 1. GaN's combination of high saturation velocity and wide bandgap enables its high-power, high-frequency performance, and establishes it as the premier material for future mm-wave electronics.

In the past two decades, GaN HEMTs have routinely demonstrated to record high power density performance across the GHz frequency range. Initial reports of GaN HEMT performance focused on the conventional metal-polar AlGaN/GaN heterostructures with an emphasis on electric field-shaping metal plates, which allow GaN's breakdown performance to further exceed all other competitive platforms. Among the remarkable power densities demonstrated were 40 and 30 W mm⁻¹ at 4 and 8 GHz [7, 8], respectively. AlGaN/GaN HEMTs have also shown 10.5 W mm⁻¹ at 40 GHz (higher frequency) [9]. In an effort to scale for higher frequencies and account for short-channel effects (SCEs), other heterostructures were introduced, such as InAlN-barrier and InAlGaN-barrier GaN HEMTs, which has demonstrated over 1 W mm⁻¹ at 94 GHz [10] and 3 W mm⁻¹ at 96 GHz [11], respectively. Current state-of-the-art performance has been achieved using N-polar GaN HEMTs. By incorporating a thick GaN cap layer, N-polar HEMTs have significantly reduced device dispersion and maintain output powers above 8 W mm⁻¹ at up to 94 GHz [12, 13].

As has historically been the case with developing semiconductor technologies, the laboratory achievements of GaN amplifiers made its first major application appearances in the defense industry. In 2018, Northrup Grumman supplied the first GaN-based ground/air radar system to the U.S. Marine Corps [14]. The Space Fence, a radar network used to track objects in Earth's orbit made possible with GaN amplifiers, was enabled by Lockheed Martin and declared operational by the U.S. Space Force earlier this year [15]. GaN is also emerging in commercial spaces, first in 4G-LTE base stations with more broad adaptation expected in 5G and beyond [16, 17].

With GaN now rapidly growing in both defense and commercial spaces, it is proper to assess the long-term potential of the current RF GaN heterostructures, with the intention of enabling the maximum performance possible. Many of the limitations of conventional GaN amplifiers lie in the

foundational layer of the heterostructure—the buffer. While not directly involved in device transport, the buffer material properties have a profound impact on device characteristics and overall performance. In the conventional AlGaN/GaN heterostructure, where the channel is an extension of the GaN buffer, there is a lack of a back barrier to confine the 2DEG in the vertical direction. The consequence is a spreading of channel region into the buffer, with the end result being a significant increase in output conductance, limiting device gain and efficiency in the mm-wave regime. Additionally, buffer leakage currents are common with GaN buffers. AlGaN back barriers were introduced [18–20] to combat this effect, but at the cost of introducing a higher thermal-resistive alloy layer in the path of the heat flow. Heat dissipation continues to be a significant limitation for GaN technology, and the addition of an alloyed backbarrier limits it further.

It is here, in the juxtaposition of blooming commercial development and an unoptimized GaN amplifier heterostructure, that we propose a new platform for the future of GaN amplifiers: aluminum nitride (AlN). The incorporation of AlN in the form of a buffer layer will enable next generation performance in three critical ways. (1) Enhance thermal management. (2) Provide a maximized back barrier, drastically reducing SCEs and buffer leakage. (3) Enable an unprecedented level of integration in nitride electronics.

The primary integration element enabled by an AlN platform is the addition of the GaN/AlN p-channel FET, allowing for true, high-current nitride CMOS-like RF complementary circuits for the first time in wide bandgap semiconductors [22]. This is made possible with an AlN/GaN/AlN heterostructure, which produces high density, 2D electron and hole gases simultaneously.

In addition to enabling nitride CMOS and RF amplifiers on the same platform, AlN also allows for the full integration of passive components. AlN bulk acoustic wave (BAW) filters, widely adopted in telecommunication front-end modules, can seamlessly integrate via the AlN buffer. Along with signal isolation (BAW filter), computation (CMOS), and amplification (AlN/GaN/AlN HEMT), the AlN platform will also allow for the integration of state-of-the-art SiC substrate-integrated waveguides (SIWs) for RF signal guidance. The fully realized AlN platform (illustrated in figure 1), with superior AlN HEMT performance potential and unprecedented integration capability, will bolster GaN amplifiers as the forefront technology for the future of mm-wave amplification, and will open the door for an array of new applications previously unachievable with nitride electronics, or any other semiconductor platform.

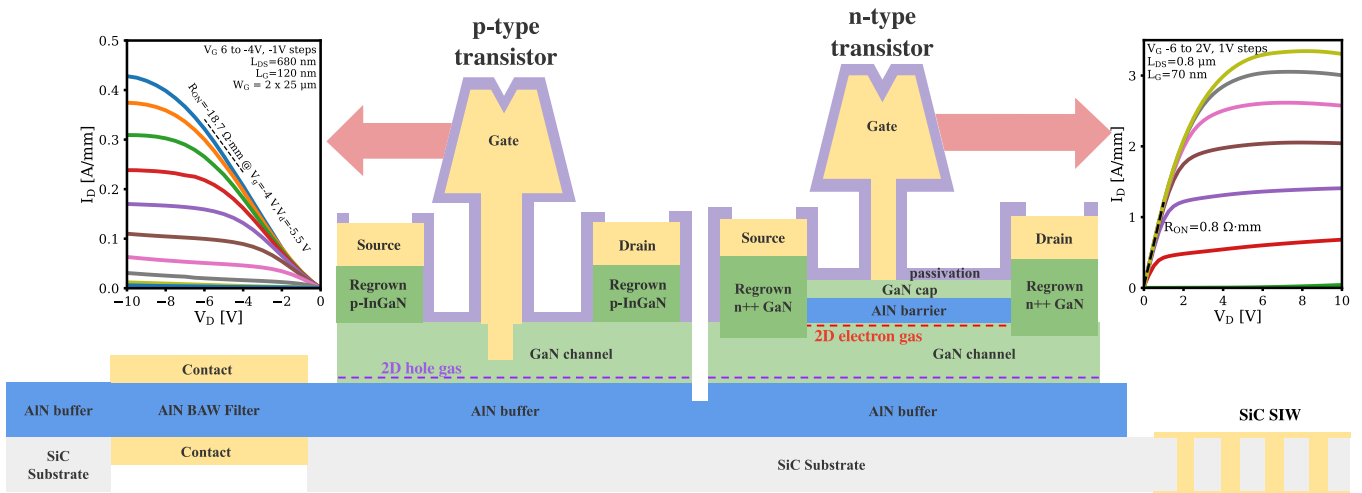


Figure 1. A cross-section of the proposed AlN platform. The incorporation of an AlN buffer will improve upon existing n-type GaN amplifiers, and allow for the inclusion of high-current p-type transistors on the same heterostructure. AlN also enables integration of both BAW filters and SIWs, providing a fully-integrated monolithic RF signal-processing solution. The pFET output characteristics are from Nomoto *et al* [21]. © [2020] IEEE. Reprinted, with permission, from [21].

2. Thermal advantage of AlN

High-frequency performance of GaN HEMTs stems directly from the fundamental material properties such as band-gap and electron transport. A wide bandgap results in a higher breakdown voltage, and a high electron mobility and saturation velocity of the carrier results in higher intrinsic frequency of operation. These properties set an intrinsic limit on the output power a material platform can support. However, a large discrepancy is observed when the experimentally measured output power densities are compared to the intrinsic material output power limit for GaN RF HEMTs, especially at lower cutoff frequencies (f_T) [23]. This difference is explained by considering the effect of heat generation and dissipation during the amplifier operation. In a simple picture, a power amplifier (PA) transforms a low-power input AC signal into an amplified higher-power AC output signal, with the difference coming from the applied DC bias power. In a real world device, only a part of this DC power goes into amplifying the output (depending on the amplifier efficiency)—the remaining power is transferred into the surroundings and the semiconductor material itself in the form of heat. This leads to a highly localized rise in temperature on the drain side of the transistor channel, which deteriorates the electronic properties such as mobility, saturation velocity, limiting the maximum output power that can be extracted from the transistor. The heating is also responsible for a thermal stress gradient in the device semiconductor layers which reduces the reliability and lifetime of the transistor.

Therefore, it is important for any high power RF platform to efficiently conduct the heat away from the active region channel in order to enhance the performance. In an RF HEMT, the drain side of the gate, where the electric field peaks, acts as a heat source. In the absence of a top heat-conducting layer, the heat primarily conducts through the buffer, into the substrate and to the heat sink at the bottom—as illustrated in figure 2(b). The thermal resistances between the channel and

sink therefore play a crucial role in determining the channel temperature and thereby the device performance. The thermal resistances in this setup are in two forms (1) (inverse of) thermal conductivity of the buffer and substrate materials, and (2) thermal boundary resistances between two materials. Both these resistances are manifestations of the fundamental physics of heat transport via phonons and therefore are intrinsic to the semiconductor materials if we consider an ideal crystal material. This allows us compare the AlN platform (AlN buffer on substrate), with the conventional GaN platform (GaN buffer on substrate) and highlight the advantage which the AlN provides us with respect to the expected thermal performance.

Figure 2(a) compares the experimentally measured thermal conductivity values of common materials in III-nitride devices. Silicon (111) and silicon carbide (SiC) are commonly used substrates for these family of devices. SiC, with a high thermal conductivity of $\sim 420 \text{ W mK}^{-1}$ is the substrate of choice for effective thermal management in the current state-of-art RF GaN HEMTs. Single-crystal diamond [24] and cubic-boron nitride (c-BN) [25] have the highest thermal conductivities and there are efforts to integrate these as conduction/heat spreading layers in RF HEMTs [27]. In III-nitrides, AlN has a higher thermal conductivity of 340 W m.K^{-1} compared to 230 W mK^{-1} of single-crystal GaN. It is clear from these values that an AlN buffer holds an advantage over a GaN buffer in terms of heat conduction away from the active region.

An additional factor to consider is the thermal boundary resistance (TBR) between the substrate and the buffer layer. TBR is an intrinsic property of an interface where it acts as a resistance to heat flow and leads to a rise in temperature. In a microscopic picture, according to the diffusive mismatch model (DMM) [26], the TBR at a perfect interface between two ideal materials arises due to the difference in phonon density of available states for a heat carrying phonon to scatter into when moving from one material to the other. The calculated TBR between AlN and GaN buffer layers and commonly used

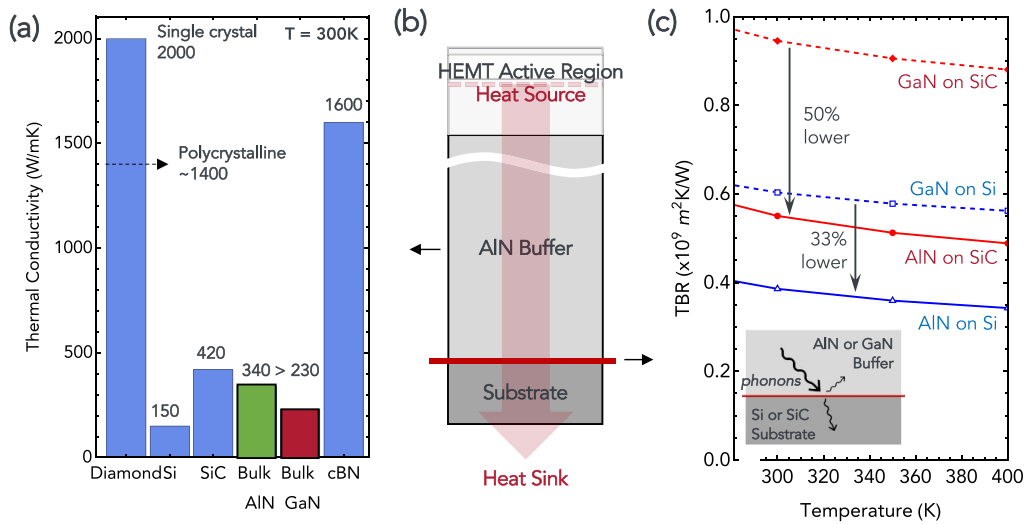


Figure 2. (a) Thermal conductivities of some commonly used materials in III-nitride electronics [24, 25]. Ternary and quaternary alloys are expected to have lower conductivities than their constituent binary counterparts. (b) Theoretical thermal boundary resistances (TBR) calculated using density mismatch model (DMM) [26] under Debye approximation. AlN is expected to have a lower TBR compared to GaN buffers on common substrates such as silicon and silicon carbide. A perfect homoepitaxially grown AlN on single crystal AlN substrates will not have any thermal boundary resistance as a boundary is not defined in that case.

Si(111) and SiC substrates are shown in figure 2(c). The Debye density of states approximation has been used. This model predicts that an AlN buffer should have a lower TBR compared to GaN buffer on both SiC and Si substrates, by ~50% and ~33%, respectively. Experimental measurement of TBRs for these structures have yielded values a couple of orders higher which is attributed to the non-ideal crystal structure near the nucleation interface. This is especially true in case of GaN, where AlN nucleation layers and/or stress-management layers with lower crystal quality result in high TBRs. AlN, with a lower lattice mismatch, can be directly grown on SiC with a better crystal quality and thus lower a TBR. Recent availability of high quality single-crystal substrates have opened up the possibility of homoepitaxial growth of GaN and AlN on bulk GaN and bulk-AlN substrates, respectively, in which TBR will be completely eliminated [28, 29]. Even in this case, comparing to GaN on GaN, AlN on bulk AlN holds a thermal advantage due to higher thermal conductivity.

Thus it is shown how an AlN buffer leads to a better thermal management in RF HEMT when compared to a GaN buffer grown heteroepitaxially on Si, SiC or homoepitaxially on bulk substrates. This should lead to a performance boost in the AlN buffer devices, especially for high power RF transistors. However it must be noted that the values are for near-perfect crystals, and the actual epitaxial crystal quality determines the value of thermal resistances encountered in a real device. Hence the translation of these expected device performance boosts depend heavily on the quality of the material grown.

3. Growth of AlN devices

The first and important step in the design of any high-performance electronic device is the crystal growth. Research into growth of III-nitrides have a rich history of over five

decades. Growth of electronics-grade GaN crystals have been investigated and studied from the early days in RCA back in 1960 [30]. The commonly used epitaxial techniques for growth are metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Traditionally in GaN device growths, AlN has been used either as nucleation layers to counter the lattice mismatch between GaN and the substrate and to improve the quality of subsequent layers. AlN is also used as thin barrier/spacer layers in Al(Ga)N/GaN HEMT structures.

Recent research in electronics-grade AlN growth has been driven by UV LEDs and lasers [31] on sapphire substrates or bulk single-crystal substrates, and by transistors on AlN platform [32]. These require much thicker AlN layers than those used in GaN HEMTs, typically 0.5–1 μm .

Taking a closer look at Al-polar AlN growth for transistor applications, the thick AlN buffer is the essential building-block of the AlN platform. Various groups have demonstrated the growth of AlN buffer layers for HEMTs using MOCVD [33], plasma-assisted (PA) MBE [34], ammonia (NH_3) MBE [35]. The AlN layers have been grown on various substrates such as MOCVD-grown AlN on Sapphire templates [36], 6 H-SiC [37] and Bulk single crystal AlN [34] as starting substrates. 6 H-SiC is typically the substrate of choice for high-power RF transistors due to its low lattice mismatch with respect to AlN, high thermal conductivity and availability of large wafers. Furthermore, it opens up the unique prospect of integration with SIW technologies (SIW) using through substrate vias (TSVs). Typical dislocation densities in devices on MBE-grown 1 μm thick AlN buffers on 6 H-SiC range in $\sim 10^9 \text{ cm}^{-2}$. It must be noted that fully-strained AlN on SiC films up to 700 nm have been demonstrated with threading dislocation densities in the mid 10^8 cm^{-2} [38]. Reducing the dislocation densities should reduce the gate leakage in Schottky gated

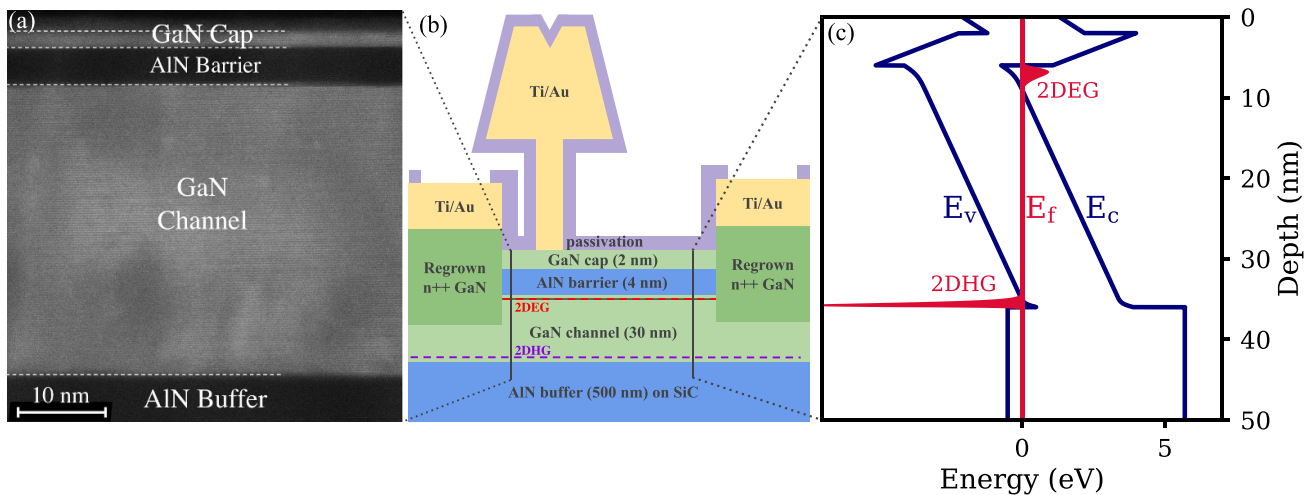


Figure 3. (a) A transmission electron microscope (TEM) image of the MBE-grown AIN/GaN/AIN heterostructure demonstrating atomically-sharp interfaces. (b) A cross-sectional representation of a fully processed, T-gated AIN/GaN/AIN HEMT. (c) The energy band diagram for the heterostructure, showing the predicted formation of both a 2DEG and 2DHG.

transistors, translating to high on-off ratios. Recent efforts in MBE have successfully demonstrate high-quality homoepitaxial AIN on single crystal AIN substrates [28, 29] by optimized crystal surface cleaning.

Because of its wide bandgap and high activation energies of impurity dopants, these AIN layers are electrical insulators and show low buffer leakage in a transistor. On top of this buffer, an active region with a 2D electron gas (2DEG) is grown for n-channel devices, as shown in figure 3. A GaN layer, typically 20–200 nm thick, is used as the channel layer. GaN layers up to 30 nm thick have been shown to be pseudomorphically strained to the AIN buffer. An AIN barrier then grown on top generates a high-density 2DEG at the AIN/GaN interface of densities $\sim 2\text{--}4 \times 10^{13} \text{ cm}^{-2}$. The channel thickness and the barrier thickness are independent knobs to tune the 2DEG density. Typical room temperature Hall mobilities in these 2DEGs have been measured to be around $\sim 700 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ at high densities of $\sim 2\text{--}3 \times 10^{13} \text{ cm}^{-2}$ [34, 35, 37]. Even though this number is lower than mobilities ($\sim 1800 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ reported for lower density 2DEG (mid- 10^{12} cm^{-2}) in GaN HEMTs, the high charge densities and high conductivities enable low R_{ON} and high on-current densities in AIN/GaN/AIN HEMTs [37]. A few groups have also demonstrated a higher mobility 2DEG $\sim 1400\text{--}2000 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ at a 2DEG density of $\sim 1 \times 10^{13} \text{ cm}^{-2}$ using an AlGaN barrier instead of AIN barrier [33, 39]. This gives up the advantage of having a relaxed barrier which is preferred for the reliability of a RF HEMT.

The AIN buffer also offers a unique platform for p-channel transistors due to the ability to generate a high density two-dimensional hole gas (2DHG) at the GaN channel/AIN buffer interface [40]. This is the p-type analog of the Al(GaN)/GaN n-channel HEMT structure. It does not need any acceptor doping to generate holes. An undoped GaN/AIN heterostructure exhibits a hole density of $\sim 5 \times 10^{13} \text{ cm}^{-2}$ and Hall mobility of $25 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ at room temperature.

The presence of both a high-density 2DEG and 2DHG on the same platform makes it very attractive for wide-bandgap

CMOS devices. Record p-channel [21] and n-channel devices [41] have been demonstrated on this platform.

4. AIN/GaN/AIN power amplifier

Thoughtful III-Nitride heterostructure design is the foundation upon which all high-power, mm-wave devices must be built. As previously mentioned, AIN is the premier III-nitride buffer material, as it simultaneously confines the 2DEG and 2DHG, electrically insulates, and thermally conducts better than GaN. Equally as important for mm-wave performance is the material choice for the top barrier. For RF amplifiers, high transconductance and gain are critical, and it is therefore necessary to scale the barrier as thin as possible. This is where material choice is key, as the top barrier material can limit vertical scaling by requiring a certain thickness to generate sufficient charge density.

To quantify this, a self-consistent 1D Schrodinger-Poisson solver [42] was used to simulate the barrier thickness required to generate a 2DEG high density of $2 \times 10^{13} \text{ cm}^{-2}$ for AlGa_{0.3}N, InAlN, and AIN top barriers on Ga-polar GaN channels (figure 4). The Al_{0.3}Ga_{0.7}N barrier, even at 20 nm thick, is unable to achieve the desired high density 2DEG, instead showing $1.4 \times 10^{13} \text{ cm}^{-2}$. Also popular in contemporary GaN HEMT design is the InAlN barrier. In_{0.17}Al_{0.83}N fares better, generating a $2 \times 10^{13} \text{ cm}^{-2}$ 2DEG at a barrier thickness of 6 nm. Notably, an AIN top barrier of just 1.4 nm able to meet the $2 \times 10^{13} \text{ cm}^{-2}$ 2DEG threshold. This reduction is due to the increased polarization difference at the AIN/GaN interface. While the necessary AIN thickness will change slightly when the AIN top barrier and GaN channel are strained to an AIN buffer, this simple comparison is used to demonstrate the general scalability of AIN versus other common top barrier semiconductors. The reduced top barrier thickness provided by AIN is critical for future ultra-scaled mm-wave devices, as it has been empirically shown that transconductance rapidly falls off when the gate length to barrier thickness ratio ($L_G:t_b$)

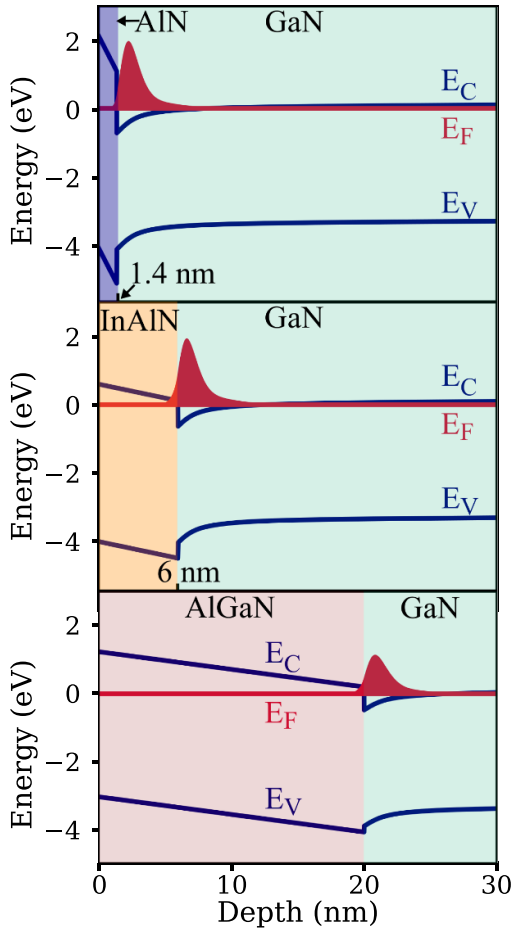


Figure 4. Highlighting the top barrier thickness of AIN, InAlN, and AlGaN required to generate a high density (2×10^{13}) 2DEG. AIN requires a thickness of 1.4 nm, while InAlN requires 6 nm. In the case of the AlGaN barrier, a 2DEG density of 1.4×10^{13} is achieved at a barrier thickness of 20 nm.

is less than five [43]. This is due to SCEs that can be attributed to the lack of gate control, as a result of the increased distance between the gate and the 2DEG. It is important to note that SCEs are also heavily dependent on the presence of a back barrier, and that both a back barrier and thin top barrier are necessary to effectively mitigate SCEs for ultra-scaled HEMTs. While $L_G/t_b < 5$ may shift depending on the full heterostructure design, it can serve as a rule-of-thumb for the gate length limit for commercially-viable device design. Going off this rule, to achieve RF devices with a high density 2DEG and without significant SCEs, an AlGaN barrier will require an L_G of 100 nm, and InAlN requires $L_G = 30$ nm. This is a clear limiting factor, as gate lengths as short as 20 nm have already been demonstrated in industry [44]. With an ideal AIN top barrier of 1.4 nm, and accounting for the fact that the centroid of the 2DEG is ~ 1 nm from the interface, SCEs can be prevented to a gate length of 10 nm. To maximize vertical scaling capabilities, and to take advantage of state-of-the-art, already available gate technology, an AIN top barrier is advantageous.

The incorporation of AIN in both the top barrier and buffer results in an AIN/GaN/AIN heterostructure. Devices on this heterostructure, grown by molecular beam epitaxy (MBE),

were first demonstrated in 2012 [32]. In this report, the GaN channel is scaled to 30 nm in thickness. This improves confinement of the 2DEG and minimizes the distance from the active region to the more thermally conductive AIN buffer. Another effect of having a thin GaN channel is that it can be pseudo-morphologically strained to the AIN buffer [45]. This translates up through the GaN channel to the AIN top barrier, resulting in a relaxed top barrier that increases device reliability and is capable of preventing significant leakage currents at a thickness of just 1 nm [46] due to the high conduction band offset between GaN and AIN.

Perhaps most critically for high-power, mm-wave applications, AIN boasts the largest bandgap, and therefore the largest critical electric field, of the III-nitrides. This is advantageous for increasing device breakdown, which can dramatically increase the maximum output power. Accordingly, the breakdown characteristics of AIN/GaN/AIN HEMTs were investigated for gate-drain lengths (L_{GD}) ranging from 0.27 to 5.1 μm [37]. For RF amplifiers, the breakdown voltage metric is defined as the voltage at which $I_D \geq 1 \text{ mA mm}^{-1}$. The devices were covered in Fluorinert during the measurement process. Figure 5(a) shows the three terminal off-state breakdown of three AIN/GaN/AIN HEMTs with varied gate-drain distances. Among all devices, the highest breakdown voltage observed is $V_{BD} = 591 \text{ V}$ ($L_{GD} = 5.1 \mu\text{m}$), corresponding to an average electric field (E_{BD}) of 1.16 MV cm^{-1} . All measured devices had average electric fields above 1 MV cm^{-1} at breakdown, with 80% of RF devices showing average breakdown fields above 1.5 MV cm^{-1} and up to 2 MV cm^{-1} . Prior to breakdown, the gate current is found to be roughly equal to the drain current. As a result the breakdown is likely due to gate-drain leakage and not avalanche or channel breakdown, and therefore is far from the material limits. While the breakdown mechanics of GaN HEMTs in general are still not fully understood, the consistently high breakdown fields observed in AIN/GaN/AIN HEMTs are promising for the RF amplifier potential of the heterostructure. The high breakdown voltage translates to high operating voltage, as demonstrated by the small-signal performance at a drain bias of 30 V, benchmarked in figure 5(c), yielding a Johnson figure of merit value of $2.2 \text{ THz} \cdot \text{V}$.

More recently, AIN/GaN/AIN HEMTs were fabricated for large-signal amplification measurements. The AIN/GaN/AIN heterostructure was grown by MBE on 6 H-silicon carbide substrates. The fabrication process for the AIN/GaN/AIN HEMTs is highlighted by MBE-regrown ohmic contacts and electron beam lithography (EBL) defined T-gates. The regrowth process begins by patterning the regrown contact regions with a chromium/silicon dioxide hardmask. The sample is then etched via a chlorine-based inductively coupled plasma (ICP) to expose the 2DEG from the sides. The sample is loaded into the MBE where heavily n-type doped ($[\text{Si}] \sim 10^{20} \text{ cm}^{-3}$) GaN is regrown to form an ohmic contact to the 2DEG. The hardmask is removed by a buffer oxide etch. This regrowth process produced a contact resistance of $0.23 \Omega \cdot \text{mm}$. The T-gated devices showed on-currents up to 3.3 A mm^{-1} , as shown in figure 6(a). This high on-current is achieved with an AIN-top barrier thickness of 4 nm and a

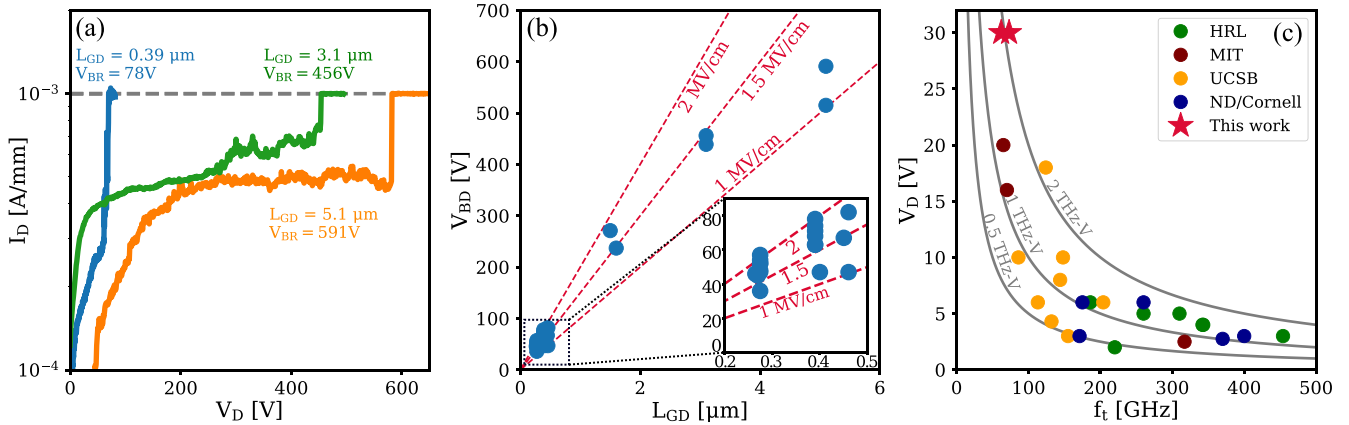


Figure 5. (a) Hard breakdown for three HEMTs with varied gate-drain separations. (b) Breakdown voltage scaling as a function of gate-drain separation ranging from 0.27 to 5.1 μm . (c) Johnson figure of merit benchmark plot comparing the AlN/GaN/AlN HEMT to state-of-the-art GaN HEMTs with submicron L_{GD} and no field plate. Plots are from Hickman *et al* [37]. © [2019] IEEE. Reprinted, with permission, from [37].

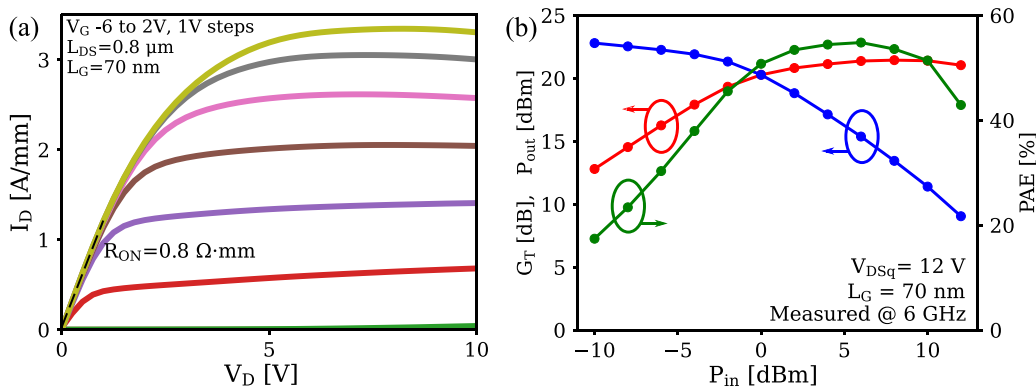


Figure 6. (a) The output characteristics for an AlN/GaN/AlN HEMT, demonstrating $R_{on} = 0.8 \Omega \cdot \text{mm}$ and high on-current of 3.3 A mm^{-1} . (b) Initial load-pull characteristics for these devices, showing 55% power added efficiency (PAE), but with significant gain compression that limits output power to 2.8 W mm^{-1} at 6 GHz.

corresponding charge density of $3 \times 10^{13} \text{ cm}^{-2}$. Small-signal measurements were performed across a range of gate and drain bias points, with the best single bias-point cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of 140 and 239 GHz, respectively. Finally, initial large-signal measurements were performed for these devices, yielding a high power added efficiency (PAE) of 55% and a corresponding output power (P_{out}) of 2.8 W mm^{-1} at 6 GHz. The output current density at this PAE/ P_{out} was 500 mA mm^{-1} . These initial devices were limited by gain compression, a product of immature fabrication processes, including but not limited to unoptimized SiN-last passivation. The long-term solution to the unoptimized SiN is *in-situ* passivation, deposited during the MBE growth of the heterostructure. Efforts are currently underway to significantly increase the thickness of the top AlN barrier ($>20 \text{ nm}$), which will move the surface significantly further away from the channel, mitigating dispersion and subsequent gain compression. In this case, a recessed gate contact will be used to maintain gain at mm-wave frequencies.

While process immaturity currently limits the output power of RF transistors on the AlN platform, the large breakdown, near-record on-currents, promising small-signal

measurements, and high PAE, are indicative of much higher performance. This combined with an optimized heterostructure capable of the most aggressive vertical scaling, suggest that the AlN/GaN/AlN HEMT will soon be capable of much higher output power ($>10 \text{ W mm}^{-1}$) at mm-wave frequencies.

5. AlN-based CMOS

The prospect of wide-bandgap CMOS, particularly in nitrides, has been limited by the physics and development of the p-type conductivity [22]. Difficulties for GaN p-type technology are rooted in the heavy valence band effective masses (low mobility) and deep valence energies (hard to contact). Furthermore, the large acceptor ionization energy (150–200 meV for Magnesium [47]) results in poor dopant activation efficiencies of less than 5%. While numerous structures (GaN/Al-GaN, GaN/AlInGa, InGaN/GaN) have used polarization to induce hole gases, it is only on the AlN platform, using a relatively simple Ga-polar GaN/AlN heterostructure, that a 2DHG has been successfully demonstrated in nitrides without the use of acceptor doping [40]. This is the p-type analog of the

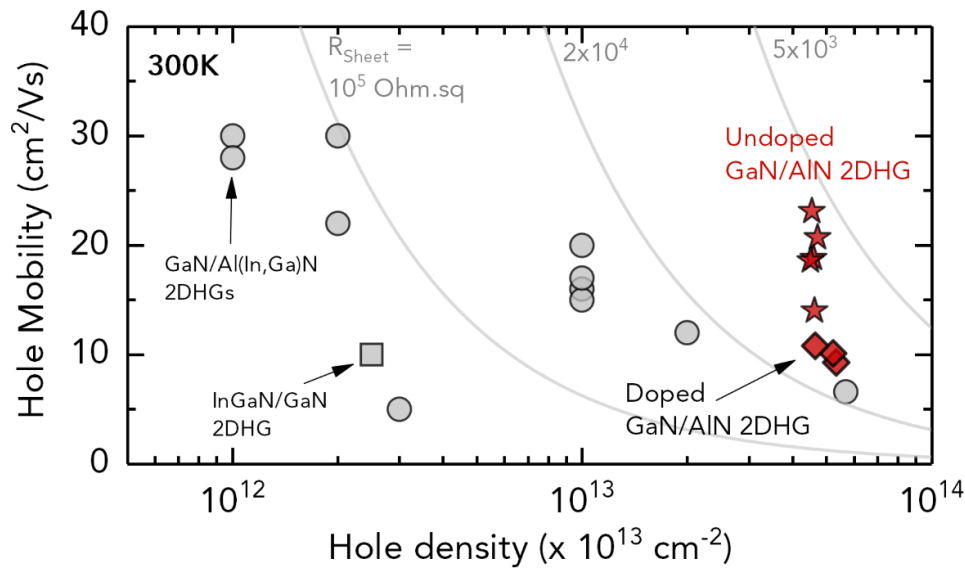


Figure 7. The 2D hole gas in GaN/AlN heterostructures compared to other reported 2DHGs on in III-nitrides. Note that the only 2DHG reported so far in a heterostructure without acceptor doping is the GaN/AlN 2DHG [40]. Comparison to other hole gases on other platforms can be found in Chaudhuri *et al* [40].

ubiquitous Al(GaN)/GaN 2DEG which serve as the channel for RF HEMTs.

Another issue for GaN p-channels is the low hole mobility compared to electrons, with phonon scattering restricting the room-temperature hole mobilities [48, 49] to $\sim 50 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ (compared to $\sim 1000\text{--}1800 \text{ cm}^2 \text{ V} \cdot \text{s}^{-1}$ in GaN 2DEGs). Therefore, in order to minimize sheet resistance, most of the heavy lifting must come from the carrier density. In the same manner as the n-type devices, the GaN/AlN interface provides the maximized polarization difference, and has generated 2DHGs densities of $\sim 5 \times 10^{13} \text{ cm}^{-2}$, among the highest reported among III-nitrides, as shown in figure 7.

A more practical, yet just as significant, hurdle to commercial realization of GaN CMOS is the ease of integration of the n-type and p-type devices. In p-type heterostructures that require doping and/or multi-channel structures, it is difficult to produce quality, high-density, and easily accessible 2DHGs and 2DEGs on the same heterostructure. Fortunately, the same AlN/GaN/AlN heterostructure used to produce the n-channel FET/HEMT results also contains the exact GaN/AlN interface which has yielded the high 2DHG carrier densities shown in figure 7. It has been demonstrated [50] that after a low-power ICP/RIE etch to remove the top AlN barrier layer, the 2DEG is eliminated and only the 2DHG remains, which is reflected in the Hall conductivity changing from n-type to p-type. It is proper to acknowledge that integration challenges remain in this scheme, such as achieving low resistance contacts to an etch-exposed p-channel and recess etch control. Still, it is the combination of simplicity of the heterostructure and quality of the 2DEG and 2DHG that offers a real chance at high-performance nitride CMOS, and it is enabled by the AlN platform.

Since the first demonstration, the GaN/AlN p-channel FET (pFET) has shown continuous improvement with device processing iterations. The first GaN/AlN pFET was demonstrated

in 2012 [52], with on-currents over -100 mA mm^{-1} when the device was pushed to -40 V drain bias, and was limited to 3x on/off ratio. In 2019, pFETs showed high current performance within a reasonable bias range, with the drain current in excess of -100 mA mm^{-1} at -10 V drain bias [51]. More recently, pFET devices on the GaN/AlN platform have demonstrated a record high on-current of 0.42 A mm^{-1} [21], as shown in figure 9(a). The peak transconductance of 66 mS mm^{-1} was observed with two orders of on/off modulation (figure 9(b)). This on/off ratio on this Schottky-gated device is limited by gate leakage. The tuning of the gate placement, surface treatment, and incorporation of a high-K dielectric will dramatically reduce leakage while retaining the overall device performance. The high 2DHG density, in combination with a p-InGaN cap layer below the ohmic contact metal (figures 8(a) and (c)), achieved an extremely low p-type contact resistance of $1 \Omega \cdot \text{mm}$ when the current is in excess of 100 mA mm^{-1} . A cross section of the device, as well as a benchmark of on-current achieved in nitride pFETs, are shown in figure 8. The on-current of 0.42 A mm^{-1} is an order of magnitude higher than the next closest nitride pFET platform. In addition to on-current, the GaN/AlN pFET has also set the record for small-signal gain in p-channel GaN devices, with a cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of 19.7 and 23.3 GHz, respectively, as shown in figure 9(c). The previous record for small-signal gain in p-channel GaN devices was 0.2 and 0.64 GHz [53].

As the GaN/AlN pFET on-current approaches the same order of magnitude as the AlN/GaN/AlN HEMT devices, it should finally become possible to match n and p current drives (at reasonable width ratio) in III-nitrides. The combination of current-matched devices and pFETs with f_t, f_{max} approaching mm-wave frequencies, made possible with the AlN platform, will open up wide-bandgap CMOS design space and enable new applications previously not possible with GaN.

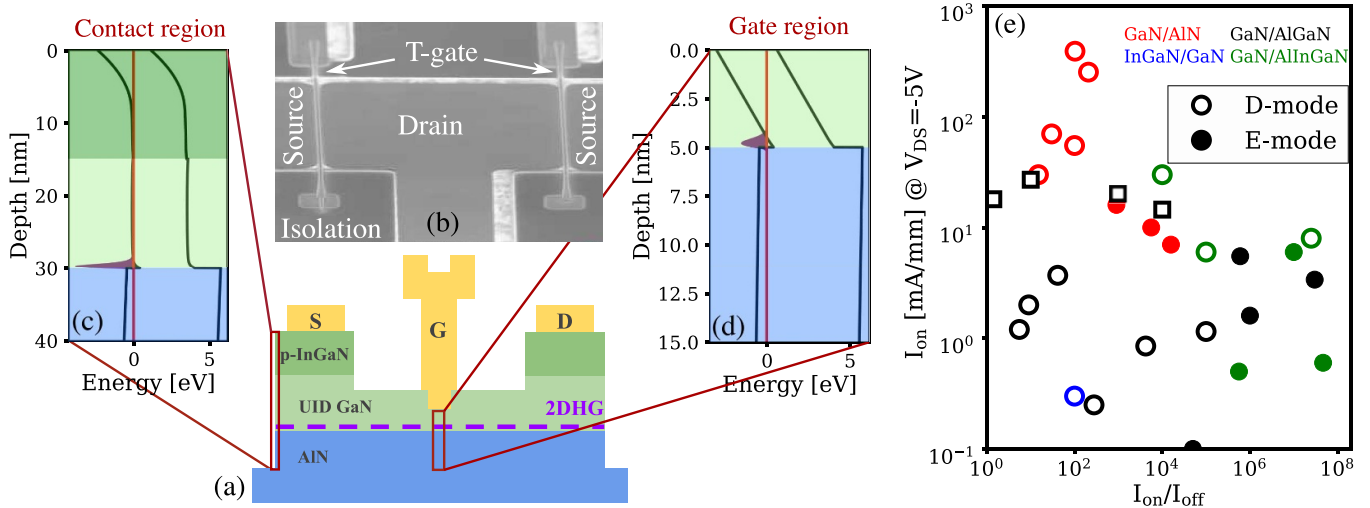


Figure 8. (a) Cross-section representation and (b) SEM image of a fully processed GaN/AlN pFET, with energy band diagrams highlighting the (c) contact and (d) gated regions. Note the channel region is completely undoped. (e) A benchmark plot of reported III-nitride pFETs, with the highest on-currents achieved by the GaN/AlN heterostructure. Figures are modified and updated from Bader *et al* [22, 51]. © [2019] IEEE. Reprinted, with permission, from [51].

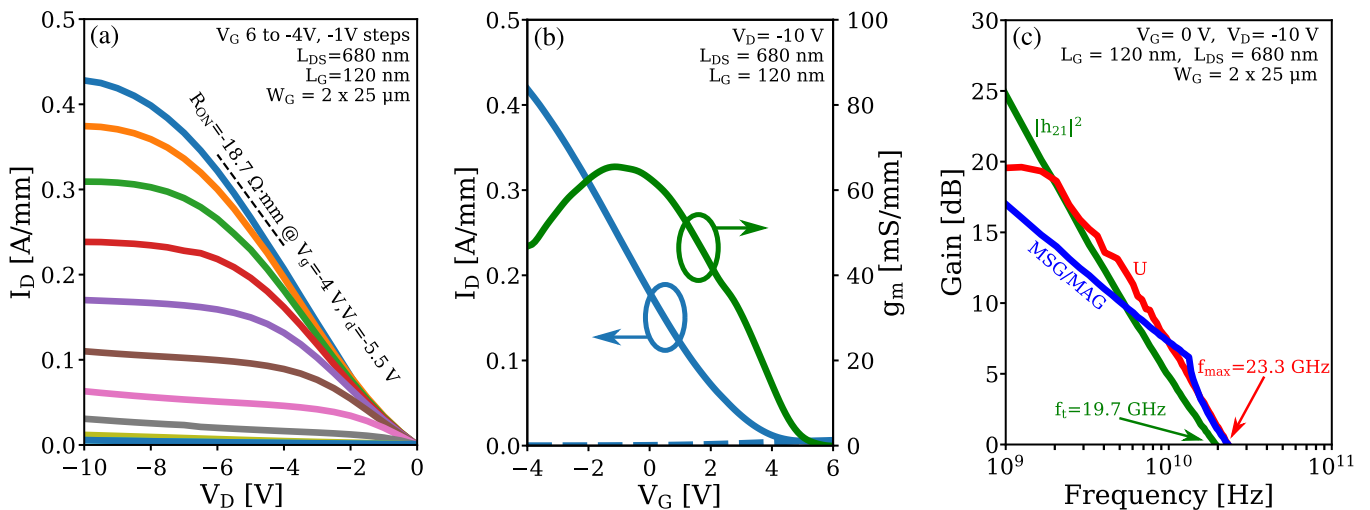


Figure 9. (a) The output characteristics for a GaN/AlN pFET with -100 mA mm^{-1} on-current. (b) The log and (c) linear transfer curves for the same device, highlighted by a transconductance of 15 mS mm^{-1} . Plots are from Nomoto *et al* [21]. © [2020] IEEE. Reprinted, with permission, from [21].

6. BAW filter integration

RF communication systems consist of a transmit (Tx) and receive (Rx) module. The transmit module consists of a high power amplifier (PA) to create and emit high-frequency electromagnetic waves. This need is met by high-power, high-frequency transistors based on a semiconductor platform suited to the frequency and power needs. The kinds discussed earlier in this article using AlN/GaN nitride semiconductors offer a solution for the high-frequency and high-power window, in the mm-wave regime. As essential as to transmit is to be able to receive the signal to which noise has been added during transmission, and whose strength has diminished substantially by the time it is captured by an antenna. To boost the signal back, low-noise amplifiers (LNAs) are needed in the receive module. LNAs are active transistors that may be

designed slightly differently from the high-power PAs to boost this regime of performance. But there is a need to first discern the frequency of the signal from the noise in several other frequencies that enter the receiver antenna. For this purpose, passive filters are used. In the mm-wave exceeding 100 GHz, SIWs are used, which are discussed in the next section. This section describes the filters at lower frequencies, of 10 GHz or lower, that form the front-end of receiver modules in this frequency range. AlN plays a major role in this application because of its mix of attractive piezoelectric and dielectric properties, combined with compatibility with CMOS back-end of the line (BEOL) processing restrictions. In those applications, AlN is deposited by sputtering on the silicon platform to fabricate the filters. Increasingly, the fact that AlN is also grown epitaxially for GaN/AlN transistors is being investigated to approach this problem from the opposite end. Here we

discuss the unique opportunities and challenges in making this form of epitaxial integration of BAW with nitride electronics possible.

The AlN BAW filter operates by forming a metal–insulator–metal acoustic cavity whose thickness determines the desired filter center frequency. Because of the piezoelectric property of AlN, the electromagnetic wave is converted to a sound wave of much smaller wavelength, while conserving the frequency, and thus the cavity resonator only allows those wavelengths that fit to pass through, rejecting the others. The figure of merit of this behavior is the product k^2Q , where k^2 is the electromechanical coupling coefficient, and Q is the quality factor of the resonator. Typical values for AlN BAW filters are $k^2 \sim 0.08$ and $Q \sim 5000$ in the 1–10 GHz window. Since the thickness of AlN required to move to higher frequencies becomes deep sub-micron, the crystalline quality of the conventional sputtering technique poses significant challenges. The crystalline AlN used in nitride FETs and UV LEDs and Lasers have on the other hand managed to produce high quality AlN within 100 nm from the growth interfaces. Therefore, a significant opportunity exists to exploit the epitaxial-AlN for fabricating BAWs. This method has initially been explored [54, 55], and more recently even the metal electrodes have been deposited by epitaxy, realizing an all-epitaxial EpiBAW structure using NbN/AlN/NbN heterostructures [56]. While this is primarily in the demonstration phase, significant challenges lie ahead to harness its true potential. The challenges are not just in the crystalline and piezoelectric control of the epitaxial AlN layers, but in avoiding undesired lateral edge modes, and most importantly, controlling the resistance of the metal electrodes, whose thickness must also be scaled in tandem with the thickness of the AlN layers themselves.

The more interesting opportunity afforded by the EpiBAW structures is the potential to directly integrate them with the AlN/GaN/AlN HEMTs (and also the pFETs and the nitride CMOS) which are described earlier in this article. The on-chip nitride CMOS can then perform low-level of digital logic operations on the nitride chip, before handing off the heavy signal processing to the CMOS back end in the receiver, by taking advantage of the direct integration afforded by the AlN platform. But for moving to the 100 GHz window, the resistive losses of the BAW seem insurmountable at this point since the metal electrodes must be shrunk to a few nm thickness. But luckily the ability to integrate waveguide filters is both feasible and attractive, as discussed next.

7. AlN for SIWs

AlN has been widely used in packaging electronic devices and circuits, including those of RF and microwave electronics. Moving up to mm-wave, the relatively high dielectric constant (k) of AlN compared to that of quartz, glasses or polymers can be turned into an advantage in reducing the interconnect size in microwave monolithically integrated circuits (MMICs), which are necessary for high-density phased arrays.

Table 2. Properties of high-K substrates.

Material	Sapphire	Si	AlN	SiC
Dielectric constant	10	12	8.9	9.7
Loss tangent	10^{-4}	10^{-4}	10^{-4}	10^{-4}
Resistivity ($\Omega \cdot \text{cm}$)	10^{18}	$<10^5$	10^{14}	$>10^5$
Thermal conductivity ($\text{W cm}^{-1} \cdot ^\circ\text{C}$)	0.4	1.3	3.4	4.2
Temperature coefficient of expansion ($\text{ppm}/^\circ\text{C}$)	0.6	2.5	4.5	4.8
Toughness ($\text{MPa} \cdot \text{cm}^{1/2}$)	13	8	45	46

For example, SIWs have been developed mainly on printed circuit boards for RF and microwave electronics [57, 58]. Above 100 GHz, SIW can be realized on chip for mm-wave MMICs, whether the AlN layer is grown on a native substrate or on other high-k substrates such as SiC, Si or sapphire. This is because, the width of an SIW, approximately one half of the signal wavelength, is less than 1 mm above 100 GHz in high-k substrates, making the SIW small enough to be realized on chip. Although these high-k substrates have comparable dielectric constants and loss tangents (table 2), AlN and SiC SIWs are particularly attractive for high-power nitride electronics because of their high thermal conductivities. Additionally, they have closely matched temperature coefficients of expansion for avoiding thermally induced stress in high-power electronics. Their mechanical toughness ensures high yield for SIWs made of hundreds of through-substrate vias (TSVs). Note that the TSV process is well developed for Si, AlN and SiC.

To date, most MMICs use microstrip or coplanar waveguides as interconnects, in which the current is confined along narrow metal lines. By contrast, the current is spread throughout the cross section of an SIW, resulting in higher power-handling capacity. Being well enclosed by metal TSVs and films, the SIW has negligible radiation and crosstalk, which are critical for interconnects above 100 GHz. In fact, the SIW loss is dominated by the metal conductor loss instead of radiation loss or dielectric loss. This is also why SIWs with less than 0.5 dB mm^{-1} total loss around 140 GHz has been demonstrated in high-resistivity Si [59] and SiC [60], although they are not true insulators. It has also been shown that the SiC SIW is three times less lossy than microstrip or coplanar waveguides made of the same material. Lastly, with increasing frequency, the loss of the SIW decreases whereas the loss of the microstrip or coplanar waveguide increases.

Beyond low-loss and high-power interconnects, SIWs can be used as high-quality impedance transformers, filters, and antennas, which are critical components in high-power electronics but traditionally difficult to be integrated on chip. Impedance transformers can be readily realized by adding tuning TSVs in an SIW. By coupling a tuning TSV to a piezoelectrically controlled AlN varactor, tunable filters can be realized similar to that realized in quartz SIWs at the Ka band [61]. SIW

antennas are naturally edge emitters [62], which are more suitable for high-power phased arrays than surface emitters, giving the heat dissipation requirements.

8. Conclusion

The rapid advancements of GaN HEMTs in power and efficiency at mm-wave frequencies have enabled its prominent role in a variety of future wireless communication systems. This article has provided an overview of how AlN may enhance that role via improved HEMT design and new possibilities for nitride integration. The combination of optimized GaN amplifier performance, near current-matched nitride CMOS, and state-of-the-art BAW filters and SIWs, all on the same thermally-conductive AlN platform, will bring digital logic and analog systems together on one, fully-integrated high-power chip. The hope of this AlN-enabled system is to unlock new application spaces previously untouched by GaN electronics, and to get a glimpse of the full potential of the III-nitride material system.

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References

- [1] Gruner D, Sorge R, Bengtsson O, Tanany A A and Boeck G 2010 *IEEE Trans. Microw. Theory Tech.* **58** 4022–30
- [2] Lai R, Wojtowicz M, Chen C H, Biedenbender M, Yen H C, Streit D C, Tan K L and Liu P H 1993 *IEEE Microw. Guid. Wave Lett.* **3** 363–5
- [3] Streit D C et al 1991 *IEEE Electron Device Lett.* **12** 149–50
- [4] Pfeiffer U R, Reynolds S K and Floyd B A 2004 *IEEE Radio Frequency Integrated Symp., RFIC, Digest of Technical Papers* (Piscataway, NJ: IEEE) pp 91–4
- [5] Ingram D L, Chen Y C, Kraus J, Brunner B, Allen B, Yen H C and Lau K F 1999 *1999 IEEE Radio Frequency Integrated Symp.* (Piscataway, NJ: IEEE) pp 95–8
- [6] Grundbacher R, Lai R, Nishimoto M, Chin T P, Chen Y C, Barsky M, Block T and Streit D 1999 *IEEE Electron Device Lett.* **20** 517–19
- [7] Wu Y F, Moore M, Saxler A, Wisleder T and Parikh P 2006 *Device Conf.—Conf. Digest, DRC* pp 151–2
- [8] Wu Y F, Saxler A, Moore M, Smith R P, Sheppard S, Chavarkar P M, Wisleder T, Mishra U K and Parikh P 2004 *IEEE Electron Device Lett.* **25** 117–9
- [9] Palacios T, Chakraborty A, Rajan S, Poblencz C, Keller S, Denbaars S P, Speck J S and Mishra U K 2005 *IEEE Electron Device Lett.* **26** 781–3
- [10] Marti D, Tirelli S, Teppati V, Lugani L, Carlin J F, Malinverni M, Grandjean N and Bolognesi C R 2015 *IEEE Electron Device Lett.* **36** 17–9
- [11] Makiyama K, Ozaki S, Ohki T, Okamoto N, Minoura Y, Niida Y, Kamada Y, Joshin K, Watanabe K and Miyamoto Y 2015 *Technical Digest—Int. Electron Devices Meeting, IEDM* (Piscataway, NJ: IEEE) pp 1–9
- [12] Romanczyk B, Wienecke S, Guidry M, Li H, Ahmadi E, Zheng X, Keller S and Mishra U K 2018 *IEEE Trans. Electron Devices* **65** 45–50
- [13] Romanczyk B et al 2020 *IEEE Electron Device Lett.* **41** 349–52
- [14] Hamilton E 2018 Northrop Grumman delivers first gallium nitride (GaN) G/ATOR system to US Marine Corps (<https://news.northropgrumman.com/news/releases/northrop-grumman-delivers-first-gallium-nitride-gan-gator-system-to-us-marine-corps>)
- [15] Gallagher J, Haimerl J A, Higgins T and Gruber M 2016 *Microw. J.* **59** 4–9
- [16] Ma R and Asbeck P M 2017 *IEEE Microw. Mag.* **18** 77–85
- [17] Yuk K, Branner G R and Cui C 2017 *2017 IEEE 60th Int. Midwest Symp. on Circuits and Systems* (Piscataway, NJ: IEEE) pp 803–6
- [18] Shinohara K et al 2010 *2010 Int. Electron Devices Meeting* (Piscataway, NJ: IEEE) pp 672–5
- [19] Shinohara K et al 2011 *IEEE Electron Device Lett.* **32** 1074–6
- [20] Lee D S, Gao X, Guo S and Palacios T 2011 *IEEE Electron Device Lett.* **32** 617–9
- [21] Nomoto K et al 2020 *Technical Digest—Int. Electron Devices Meeting, IEDM* (Piscataway, NJ: IEEE) pp 163–6
- [22] Bader S J et al 2020 *IEEE Trans. Electron Devices* **67** 4010–20
- [23] Coffie R L 2020 High power high frequency transistors: a material's perspective *High-Frequency GaN Electronic Devices* (Cham: Springer) pp 5–41
- [24] Ho C Y, Powell R W and Liley P E 1972 *J. Phys. Chem. Ref. Data* **1** 279–421
- [25] Chen K et al 2020 *Science* **367** 555–9
- [26] Swartz E T and Pohl R O 1989 *Rev. Mod. Phys.* **61** 605–68
- [27] Mandal S et al 2019 *ACS Appl. Mater. Interfaces* **11** 40826–34
- [28] Lee K, Cho Y, Schowalter L J, Toita M, Xing H G and Jena D 2020 *Appl. Phys. Lett.* **116** 262102
- [29] Cho Y et al 2020 *Appl. Phys. Lett.* **116** 172106
- [30] Maruska H P and Rhines W C 2015 *Solid-State Electron.* **111** 32–41
- [31] Zhang Z, Kushimoto M, Sakai T, Sugiyama N, Schowalter L J, Sasaoka C and Amano H 2019 *Applied Physics Express* **12** 124003
- [32] Li G et al 2012 *IEEE Electron Device Lett.* **33** 661–3
- [33] Chen J T, Bergsten J, Lu J, Janzén E, Thorsell M, Hultman L, Rorsman N and Kordina O 2018 *Appl. Phys. Lett.* **113** 221601
- [34] Qi M et al 2017 *Appl. Phys. Lett.* **110** 063501
- [35] Rennesson S et al 2018 *Physica Status Solidi a* **215** 1700640–1
- [36] Chaudhuri R, Bader S J, Chen Z, Muller D, Xing H G and Jena D 2020 *Physica Status Solidi b* **257** 1900567–1
- [37] Hickman A et al 2019 *IEEE Electron Device Lett.* **40** 1293–6

- [38] Okumura H 2012 Formation mechanism of extended defects in AlN grown on SiC {0001} and their reduction by initial growth control *PhD Thesis* Kyoto University (<https://doi.org/10.14989/doctor.k16861>)
- [39] Choi U, Jung D, Lee K, Kwak T, Jang T, Nam Y, So B and Nam O 2020 *Phys. Status Solidi a* **217** 1900694–1
- [40] Chaudhuri R, Bader S J, Chen Z, Muller D A, Xing H G and Jena D 2019 *Science* **365** 1454–7
- [41] Hickman A, Chaudhuri R, Li L, Nomoto K, Bader S J, Hwang J C, Xing H G and Jena D 2020 *IEEE J. Electron Devices Soc.* **9** 121–4
- [42] Tan I H, Snider G L, Chang L D and Hu E L 1990 *J. Appl. Phys.* **68** 4071–6
- [43] Jessen G H, Fitch J R C, Gillespie J K, Via G, Crespo A, Langley D, Denninghoff D J, Trejo J M and Heller E R 2007 *IEEE Trans. Electron Devices* **54** 2589–97
- [44] Tang Y et al 2015 *IEEE Electron Device Lett.* **36** 549–51
- [45] Li G et al 2014 *Appl. Phys. Lett.* **104** 193506
- [46] Wang R et al 2012 *IEEE Electron Device Lett.* **33** 661–3
- [47] Kozodoy P, Xing H, DenBaars S P, Mishra U K, Saxler A, Perrin R, Elhamri S and Mitchel W C 2000 *J. Appl. Phys.* **87** 1832–5
- [48] Bader S J, Chaudhuri R, Schubert M F, Then H W, Xing H G and Jena D 2019 *Appl. Phys. Lett.* **114** 253501–1
- [49] Poncé S, Jena D and Giustino F 2019 *Phys. Rev. Lett.* **123** 096602
- [50] Chaudhuri R, Bharadwaj S, Miller J, Bader S J, Hickman A, Xing H G and Jena D 2019 2D electron-hole gas bilayers in undoped AlN/GaN/AlN *Int. Conf. Nitride Semiconductors*
- [51] Bader S J, Chaudhuri R, Hickman A, Nomoto K, Bharadwaj S, Then H W, Xing H G and Jena D 2019 *Technical Digest—Int. Electron Devices Meeting, IEDM* (Piscataway, NJ: IEEE) pp 4–7
- [52] Li G et al 2012 *IEEE Electron Device Lett.* **33** 661–3
- [53] Hahn H, Reuters B, Pooth A, Noculak A, Kalisch H and Vescan A 2013 *Japan. J. Appl. Phys.* **52** 19–21
- [54] Shealy J B et al 2017 *IEEE MTT-S Int. Symp. Digest* (Piscataway, NJ: IEEE) pp 1476–9
- [55] Hodge M D et al 2018 *Technical Digest—Int. Electron Devices Meeting, IEDM* (Piscataway, NJ: IEEE) pp 1–25
- [56] Miller J, Wright J, Xing H G and Jena D 2020 *Phys. Status Solidi a* **217** 1900786–1
- [57] Bozzi M, Georgiadis A and Wu K 2011 *IET Microw. Antennas Propag.* **5** 909–20
- [58] Bozzi M, Perreggini L and Tomassoni C 2019 *23rd IEEE Workshop on Signal and Power Integrity* (Piscataway, NJ: IEEE) pp 1–4
- [59] Bertrand M et al 2018 *IEEE MTT-S Int. Symp. Digest* (Piscataway, NJ: IEEE) pp 875–8
- [60] Li Y, Yang L A, Zou H, Zhang H S, Ma X H and Hao Y 2017 *IEEE Electron Device Lett.* **38** 1290–3
- [61] Asadi M J, Jin R, Ding G, Hwang J C, Scarbrough D and Goldsmith C L 2019 *J. Microelectromech. Syst.* **28** 910–8
- [62] Djeraji T and Wu K 2012 *Prog. Electromagn. Res. C* **26** 139–51