ON-Resistance of Ga_2O_3 Trench-MOS Schottky Barrier Diodes: Role of Sidewall Interface Trapping

Wenshen Li, *Member, IEEE*, Kazuki Nomoto, *Member, IEEE*, Zongyang Hu, Debdeep Jena, *Senior Member, IEEE*, and Huili Grace Xing, *Senior Member, IEEE*

***Abstract*— We present a comprehensive study of the ON-resistance (R_{ON}) of Ga_2O_3 trench-MOS Schottky barrier diodes (SBDs), with a focus on the effect of sidewall interface trapping. Capacitance–voltage characteristics of MOS-capacitors and current–voltage characteristics of trench SBDs were all repeatedly measured under increasing forward-bias stress voltage to at least +15 V. Both reveal an increase in negative charges trapped near the MOS interface under increasing forward bias, as well as slow detrapping. The slow detrapping in trench SBDs causes a current collapse and a delayed turn-on behavior in the trench SBDs due to sidewall depletion. Through modeling of the fresh R_{ON}, we found that the sidewall depletion can be eliminated under sufficiently high forward bias. Interestingly, the dynamic R_{ON} under the forward-bias stress is lower than the fresh R_{ON}. Such an anomalous behavior is well-explained by analytical calculation of the apparent differential R_{ON}, which can be lowered by a modulation of fin-channel conductivity under forward bias. This study highlights the importance of sidewall interface quality in trench-MOS SBDs and calls for scrutiny on the interpretation of the apparent differential R_{ON}, as artificially low values may arise due to the voltage dependence of R_{ON}.**

***Index Terms*— Ga_2O_3, interface-trapped charge, power semiconductor devices, Schottky diodes, trench-MOS.**

I. INTRODUCTION

As an ultrawidebandgap semiconductor material with a bandgap of 4.5–4.7 eV, β-Ga_2O_3 is quite unique since it can be grown from the melt, allowing for high quality and potentially low-cost single crystalline substrates [1].

Manuscript received January 2, 2021; revised March 3, 2021; accepted March 17, 2021. Date of publication April 2, 2021; date of current version April 22, 2021. This work was supported in part by the Air Force Office of Scientific Research (AFOSR) under Grant FA9550-20-1-0148 and Grant FA9550-18-1-0529 and in part by the NSF National Nanotechnology Coordinated Infrastructure (NNCI) Program which is carried out at Cornell Nanoscale Facility under Grant ECCS-1542081. The review of this article was arranged by Editor P. J. Fay. *(Corresponding author: Wenshen Li.)*

Wenshen Li, Kazuki Nomoto, and Zongyang Hu are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA (e-mail: wl552@cornell.edu).

Debdeep Jena and Huili Grace Xing are with the Department of Materials Science and Engineering, School of Electrical and Computer Engineering, Kavli Institute at Cornell for Nanoscale Science, Cornell University, Ithaca, NY 14853 USA (e-mail: grace.xing@cornell.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3067856.

Digital Object Identifier 10.1109/TED.2021.3067856

The ultrahigh critical electric field of ~8 MV/cm [2] and a decent electron mobility of ~200 $cm^2/V \cdot s$ [3] lead to a Baliga's figure of merit (BFOM) higher than 4H-SiC and GaN, making Ga_2O_3 a promising material for power electronics applications [4]. In recent years, fast progress has been made on the demonstration of Ga_2O_3 power devices. With a lateral device topology, a breakdown voltage (BV) over 2 kV has been reported in both Schottky barrier diodes (SBDs) [5] and transistors [6]. With a vertical device topology, enhancement-mode vertical transistors with a BV up to 2.6 kV has been demonstrated [7], as well as vertical SBDs with a BV over 1 kV [8]–[11] and a BFOM close to 1 GW/cm^2 [12].

To take full advantage of the high critical field of Ga_2O_3 in SBDs without incurring excessive reverse leakage current, reduced surface field (RESURF) techniques are generally required [13], [14]. In fact, we recently argued that it is impossible to unleash the potential of an ultrawide bandgap semiconductor in a conventional SBD topology and further outlined the guiding principles on how to design trench-MOS SBDs (or trench SBDs in short) [14]. Among various diode structures employing RESURF [13], the trench SBD [Fig. 1(a)] is particularly attractive for Ga_2O_3 since it does not require p-type doping, which is difficult in Ga_2O_3. In fact, this trench or vertical fin-based device structure is also applicable to vertical transistors [15]. Due to the requirement of only one type of doping, vertical fin-based diodes and transistors are uniquely positioned as promising power device candidates for other (ultra)wide bandgap materials, particularly for those without high-quality p-n junctions. Reduction of the reverse leakage current has been convincingly demonstrated in Ga_2O_3 trench SBDs [9], [12], [16]. Due to the RESURF, a higher maximum electric field can be sustained in the drift region, which in turn benefits the specific ON-resistance (R_{ON}) and the ON-state voltage drop (V_{ON}) under a given voltage rating [14].

Since a trench SBD involves coverage of MOS-structures over the sidewalls of the fin channels, the quality of the MOS-interfaces requires scrutiny, especially considering that the fin channels are typically formed by dry etching. In Ga_2O_3 vertical fin transistors with similar sidewall MOS-interfaces, a presence of acceptor-like interface states is observed [17]. Negative charge trapping due to such interface states is found to induce hysteresis in trench SBDs [18] and lower

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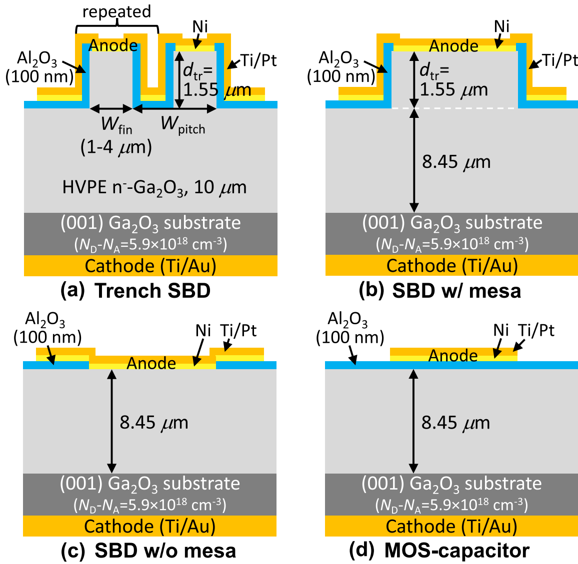

Fig. 1. Schematic cross sections of the devices fabricated on the same wafer. (a) Trench-MOS SBDs. (b) Regular SBDs with mesa. (c) Regular SBDs without mesa. (d) MOS-capacitors fabricated on the etched (001) surface.

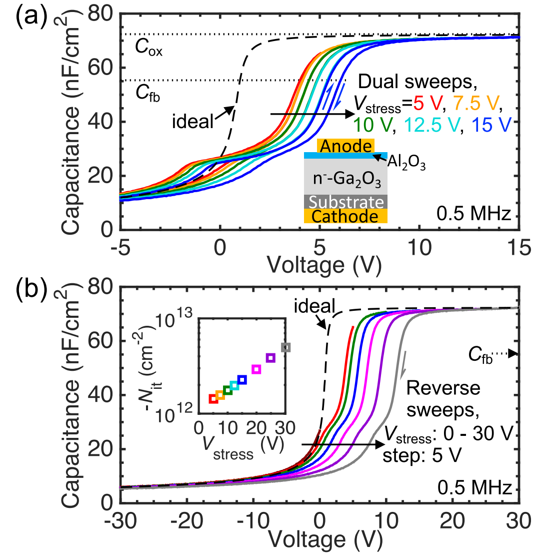

Fig. 2. High-frequency capacitance–voltage (C–V) measurements of the cofabricated MOS-capacitors. Repeated measurements were performed with a fixed reverse-bias limit of −30 V and an increasing forward-bias limit (stress voltage), which was stepped up from 0 to 30 V. Under each stress voltage (V_{stress}), three repeated dual-direction sweeps were performed starting from −3 V. (a) First dual sweeps under V_{stress} up to 15 V. The ideal C–V curve is shown in the dashed line. The subsequently repeated dual sweeps (not shown) largely follow the first reverse sweeps. (b) First reverse sweeps. Inset shows a plot of the extracted trapped interface-trapped charge density ($|N_{it}|$) under each V_{stress} value. A probing frequency of 0.5 MHz and a sweep rate of 0.44 V/s were used for all sweeps. No hold time was employed.

the ON-current [19]. The charge trapping effect can be directly observed in MOS-capacitors, and a positive shift of the flab-band voltage (V_{fb}) upon repeated measurements is reported from multiple studies [18], [20]–[23]. The interface quality is expected to be improved as the surface preparation and interface treatment techniques develop over time, as already shown in a recent study [24]. Nevertheless, the impact of interface trapping on the device performance requires careful analysis and assessment.

In this work, we study the influence of sidewall interface trapping on Ga_2O_3 trench SBDs under repeated forward-bias stressing up to +15 V, i.e., the dynamic behavior under forward bias. The diodes under study have fin channels oriented along the [010] direction and (100)-like sidewalls, which have a lower negative interface-trapped charge density ($|N_{it}|$) than other orientations [19]. Still, current collapse and delayed turn-on behaviors are observed under high forward-bias stress voltages, as a result of the increase of $|N_{it}|$ and the associated sidewall depletion. Analytical models for both the fresh and dynamic differential R_{ON} are successfully developed.

II. Device Fabrication

Fig. 1(a) shows the schematic cross section of the Ga_2O_3 trench-MOS SBDs. The epitaxial wafer consists of a 10-μm drift layer grown by halide vapor phase epitaxy (HVPE) on a (001) n-type Ga_2O_3 substrate. The net doping concentration of the drift layer is 1–2 × 10^{16} cm^{-3} as extracted from capacitance–voltage (C–V) measurements [9]. The fin channels have fin widths (W_{fin}) of 1–4 μm and a fin height or trench depth (d_{tr}) of 1.55 μm. The Schottky contact metal is Ni (30 nm) and the sidewall metal stack is Ti/Pt (40/40 nm). The fabrication process is described in [9] and [19]. After the formation of fin channels by dry etching, the wafer was soaked in HCl and then HF each for 20 min to remove the dry etch damage. The MOS-structures consist of a 100-nm Al_2O_3 dielectric layer deposited at 300 °C by plasma-assisted atomic layer deposition (ALD) with trimethylaluminum and oxygen plasma. Together with the fabrication of the trench SBDs, three other vertical diode structures were cofabricated on the same wafer, including regular SBDs with mesa, regular SBDs without mesa, and MOS-capacitors on etched (001) surface, as shown in Fig. 1(b)–(d), respectively.

III. Device Characterization

A. MOS Capacitors

Repeated C–V measurements were performed on the MOS-capacitors to investigate charge trapping effects. The reverse-bias limit was fixed at −30 V, whereas the forward-bias limit (stress voltage) was stepped up from 0 to 30 V. Under each stress voltage (V_{stress}), three repeated dual-directional sweeps were performed starting from −30 V. Fig. 2(a) shows the first dual sweeps under stress voltages up to 15 V. An ideal C–V curve without interface trapping is also shown as a reference, which is analytically calculated based on the measured net doping profile [9] using the method illustrated in [25]. In the calculation, a Ni work function of 5.15 eV and a β-Ga_2O_3 electron affinity of 4.0 eV [26] were used. The dielectric constant of Al_2O_3 (ε_{ox}) is extracted to be 8.2 ε_0 from the measured accumulation capacitance at +30 V.

The positive stress voltage is found to induce right shift of the C–V curves, indicating trapping of negative charges

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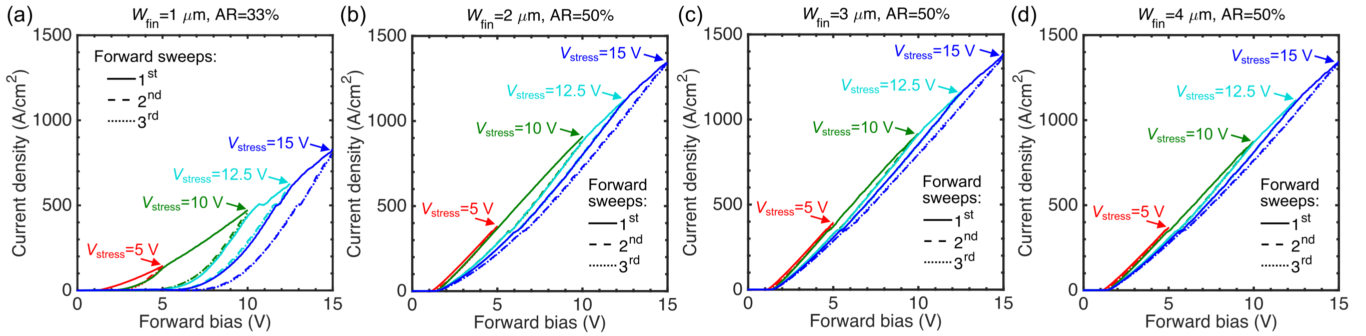

Fig. 3. Forward I–V characteristics under repeated measurements of the trench SBDs with different fin widths (W_{fin}) and similar fin AR. (a) $W_{\text{fin}} =$ 1 μm and AR = 33%. (b) $W_{\text{fin}} = 2$ μm and AR = 50%. (c) $W_{\text{fin}} = 3$ μm and AR = 50%. (d) $W_{\text{fin}} = 4$ μm and AR = 50%. The forward-bias limit was sequentially increased from 5 to 15 V. At each value, three repeated forward sweeps were performed. All I–V curves were measured under pulsed conditions with a base voltage of 0 V, a pulse width of 8.36 μs, and a duty cycle of 0.836%.

near the dielectric–semiconductor interface. Several important observations are as follows: 1) the most significant right shift is induced by the first forward sweeps; 2) the right shift is not recovered by the reverse sweeps back to -30 V, indicating that detrapping is a slow process and the responsible trap states have deep energy levels; 3) an interface-state ledge near 0 V is observed [27], which corresponds to the presence of localized density of interface states; and 4) the repeated sweeps largely follow the first reverse sweeps to the right of the interface-state ledges, similar to what we observed before [18], indicating that no significant further charge trapping is induced by the repeated sweeps. These phenomena are consistent with previous observations on MOS-capacitors under controlled stress voltage and stress time [23].

Fig. 2(b) shows the first reverse sweeps, which are used to extract ΔV_{fb}. N_{it} (<0) as a function of V_{stress} is extracted based on ΔV_{fb} with respect to the ideal V_{fb}, as shown in the inset. Under $V_{\text{stress}} = +30$ V, $|N_{\text{it}}|$ of 5.0×10^{12} cm^{-2} is extracted, similar to previous reports [18], [20], [22]. The interface charge trapping may arise from deep interface states or bulk traps within the dielectric [23]. It is worth noting that even in transistors fabricated based on exfoliated (100) Ga_2O_3 fakes, $|N_{\text{it}}|$ as high as 1–2 $\times$ 10^{13} cm^{-2} is responsible for the observed enhancement-mode operation [28].

B. Trench-MOS SBDs

Fig. 3 shows the forward I–V characteristics of the trench SBDs with different W_{fin} under repeated measurements. Similar to the C–V measurements, the forward-bias limits (stress voltages) were stepped up, and three repeated forward sweeps were performed under each stress voltage. A pulsed condition was used to avoid self-heating effects and to ensure a constant voltage sweeping rate. The fin area ratio (AR), which is defined as the ratio of W_{fin} to the width of the pitch (W_{pitch}), is 33% for $W_{\text{fin}} = 1$ μm and 50% for $W_{\text{fin}} = 2-4$ μm.

For all the measured trench SBDs, a decrease of the ON-current density is observed after the first sweeps, and the turn-on is also delayed. This dispersion is attributed to the trapping of negative charges at the sidewall interface due to the voltage stressing. The presence of negative charges at the fin sidewalls will cause sidewall depletion, thus reducing the ON-current density of the trench SBDs [19]. Trench SBDs with smaller W_{fin} suffer more dramatic decrease in the current since the same sidewall depletion width will have a larger impact on the fin conductivity percentagewise. The fact that the second and third sweeps are near identical indicates that the charge trapping was not recovered within the duration of the measurements (tens of seconds) and the charge trapping is mainly determined by V_{stress}, similar to the observations on the MOS-capacitors. The decrease of the current is more significant with higher V_{stress}, indicating an increase of $|N_{\text{it}}|$ with increasing V_{stress}, which is also similar to the observations in MOS-capacitors. These features suggest that the charge trapping behavior on the (100)-like sidewall is qualitatively the same as on the etched (001) surface.

Since V_{stress} is stepped up sequentially, the first sweeps under a new V_{stress} value would first follow the repeated sweeps under the previous V_{stress}. When the forward bias (V_F) is higher than the previous V_{stress}, V_F is swept across a fresh voltage range. As a result, the I–V curve of the first sweep would then resemble the behavior of a fresh device. Indeed, a distinct change of slope is observed in the first sweeps when V_F is equal to the previous V_{stress} value (e.g., near $V_F = 12.5$ V for the first sweeps under $V_{\text{stress}} = 15$ V).

It should be noted that a fresh device behavior could be recovered after illumination by UV-C light, which can lead to effective detrapping [29]. Alternatively, the charge trapping effects can be mitigated under elevated temperature due to the increase of the emission rate. Such an effect has been shown in GaN trench-MOS barrier Schottky (TMBS) rectifiers [30]. Ga_2O_3 devices have shown great promise for high-temperature applications [31], [32]. For real applications under high temperatures, the interface trapping issue is expected to be much less severe, although further investigations are necessary.

To understand the impact of the induced charge trapping on the ON-resistance, the corresponding differential specific R_{ON} of the trench SBDs is plotted in Fig. 4. Since the repeated sweeps are nearly identical, only the differential R_{ON} of the third sweeps is plotted. They can be viewed as the dynamic R_{ON} ($R_{\text{ON,dynamic}}$), as they are influenced by the charge trapping. In addition, R_{ON} of the first sweeps over the fresh voltage range (the upper envelope of the first sweeps) is plotted, representing the fresh R_{ON} ($R_{\text{ON,fresh}}$) without prior voltage stressing. Interestingly, the differential $R_{\text{ON,dynamic}}$ has lower minimal values than the differential $R_{\text{ON,fresh}}$, despite the fact that the actual nondifferential R_{ON} is higher under repeated

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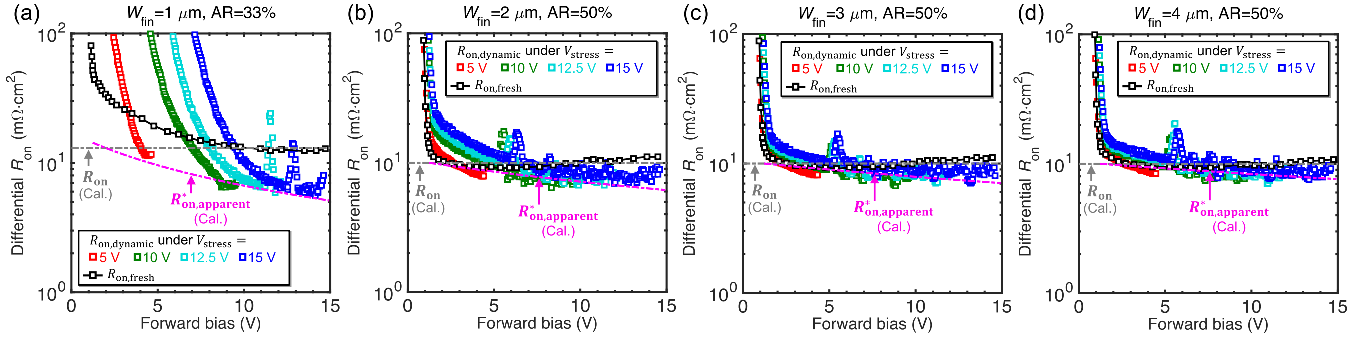

Fig. 4. Extracted differential specific ON-resistance (R_{ON}) of the trench SBDs from forward I–V characteristics in Fig. 3. (a) $W_{fin} = 1$ μm and AR = 33%. (b) $W_{fin} = 2$ μm and AR = 50%. (c) $W_{fin} = 3$ μm and AR = 50%. (d) $W_{fin} = 4$ μm and AR = 50%. Differential R_{ON} from the third I–V sweeps is extracted as $R_{ON,dynamic}$ (red, green cyan, and blue, a color scheme consistent with Fig. 3). In addition, the differential R_{ON} of the upper envelope curve of the first sweeps is extracted as $R_{ON,fresh}$ (black). The analytically calculated R_{ON} (gray) and $R^*_{ON,apparent}$ (magenta) based on (1) and (8), respectively, are indicated by dotted–dashed lines.

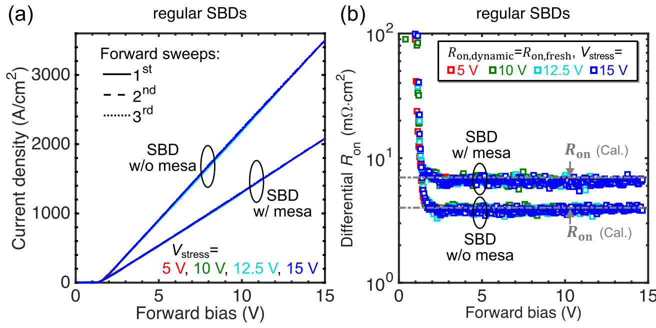

Fig. 5. (a) Forward I–V characteristics of the regular SBDs under repeated measurements. A pulse width of 0.5 μs and a duty cycle of 0.05% were used for the pulsed measurements to sufficiently suppress self-heating. All measurement sequence and other conditions are the same with the measurements on the trench SBDs shown in Fig. 3. To rule out the possible influence of the pulse width on the charge trapping, we also performed the measurements using the same pulse width as used for trench SBDs, and still no dispersion is observed. (b) Extracted differential R_{ON} of regular SBDs from the third I–V sweeps.

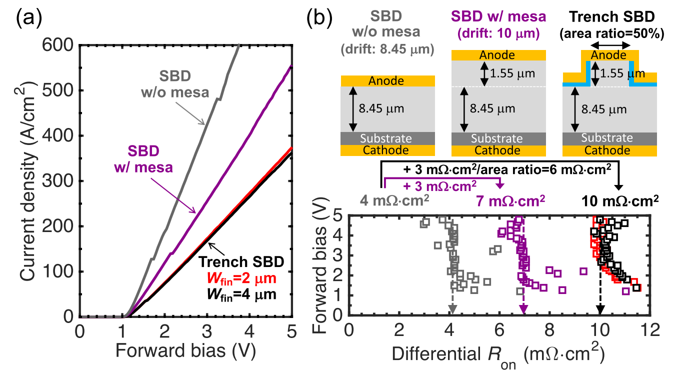

Fig. 6. (a) Comparison of the first forward pulsed I–V sweeps up to 5 V from all three types of diodes. (b) Extracted differential specific R_{ON} from the first pulsed forward I–V sweeps and the corresponding schematic cross section of the 3 different types of devices. Reprinted from Li *et al.* [9] © 2018 IEEE.

sweeps due the reduction of the ON-current. This arises from steeper slopes of the I–V curves under repeated sweeps when the forward bias approaches the stress voltage. We will model this behavior in Section III-C.

C. Regular SBDs

As comparisons, forward I–V characteristics were measured on the regular SBDs under the same measurement sequence, as shown in Fig. 5(a). In contrast with the trench SBDs, no dispersion of the I–V curves is observed. This suggests that the dispersion in trench SBDs is solely due to the sidewall interface, but not from the planar Schottky contacts. For a direct comparison, the first sweeps up to 5 V from all three types of diodes are plotted together in Fig. 6(a).

Fig. 5(b) shows the extracted differential R_{ON}, which is constant when the forward bias is beyond the turn-on voltage, as expected from an ideal SBD.

IV. ON-RESISTANCE MODELING

A. R_{ON} Model for $R_{ON,fresh}$

As can be seen from Fig. 5(b), $R_{ON,fresh}$ of the regular SBDs with and without mesa is 4 and 7 $m\Omega \cdot cm^2$, respectively. In comparison, $R_{ON,fresh}$ of the trench SBDs with an AR of 50% is ∼10 $m\Omega \cdot cm^2$, as can be seen in Fig. 4(b)–(d). These numbers show arithmetic progression and can be well-understood by considering the differences in the conduction paths in these devices, as shown in Fig. 6(b). Based on these observations, we have developed a simple model for the specific R_{ON} of trench SBDs [9], [12]

$$R_{ON} = R_1 + \frac{R_2}{AR} \tag{1}$$

where R_1 includes the contribution from all the resistive components below the fin channels and R_2 captures the contribution from the fin channels.

Fig. 7 shows the extracted $R_{ON,fresh}$ as a function of the fin AR, as well as the calculated R_{ON} based on (1) with $R_1 = 4$ $m\Omega \cdot cm^2$ and $R_2 = 3$ $m\Omega \cdot cm^2$. A very good match between the measured and the calculated $R_{ON,fresh}$ is observed. For $W_{fin} \geq 2$ μm, the differential $R_{ON,fresh}$ is nearly constant with the forward bias after ∼3 V [see Fig. 4(b)–(d)], and $R_{ON,fresh}$ plotted here is extracted at 5 V. However, in the case of $W_{fin} = 1$ μm, the extracted $R_{ON,fresh}$ gradually decreases with increasing forward bias until ∼10 V, after which it reaches a constant value [see Fig. 4(a)]. We found that only $R_{ON,fresh}$ at 10 V matches with the model, whereas $R_{ON,fresh}$ at 5 V is much higher than the calculation, suggesting the existence of sidewall depletion below 10 V in devices with $W_{fin} = 1$ μm. The higher forward bias required to eliminate

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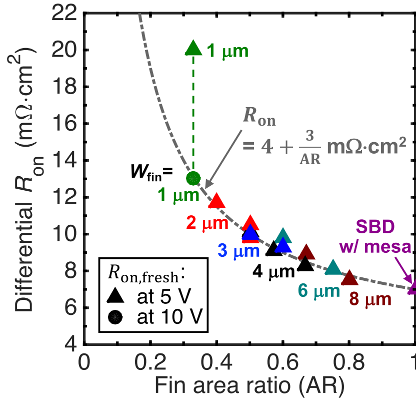

Fig. 7. Differential fresh R_{ON} under pulsed measurements versus the fin AR. The R_{ON} values are all extracted from the first measurements at either 5 V (triangle) or 10 V (circle). The dotted–dashed line shows the calculated R_{ON} from the analytical model [see (1)].

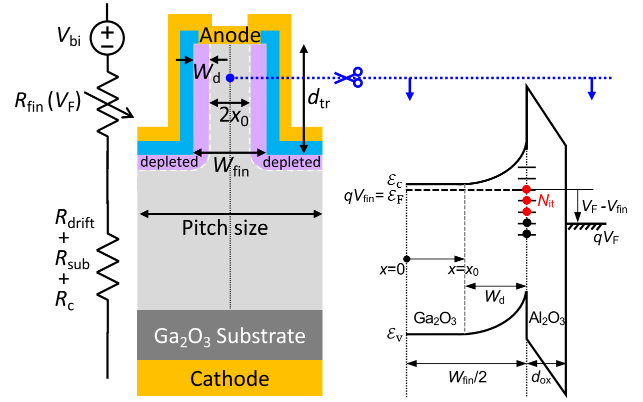

Fig. 8. Left: schematic of R_{ON} components within a unit cell of a trench SBD. Right: schematic band diagram along a horizontal cutline across the fin channel, under the presence of negative interface-trapped charge near the dielectric–semiconductor interface and a forward bias of V_F.

the sidewall depletion in 1-μm fin channels is likely due to the higher aspect ratio of the fin channel, which reduces the average voltage drop across the MOS-structure at the sidewall.

Note that the underlying assumption of (1) is that the MOS-structure at the fin sidewall is under a near flat-band condition and there is no conductivity enhancement due to electron accumulation. Since the measured $R_{ON,fresh}$ matches with the model and does not decrease further with increasing forward bias, it can be concluded that either accumulation does not occur at the fin sidewalls due to Fermi-level pinning or that the mobility near the sidewall is much lower than in the bulk such that the accumulated electrons do not enhance the conductivity appreciably. Either way, the sidewall depletion can be eliminated with a sufficiently high forward bias.

B. Apparent Differential R_{ON} Model for $R_{ON,dynamic}$

To understand the behavior of $R_{ON,dynamic}$, it is important consider the effect of sidewall depletion due to the negative N_{it} induced by prior forward-bias stressing. Fig. 8 shows the schematic cross section of a unit cell of the trench SBD in the presence of sidewall depletion and the corresponding equivalent circuit after turn-on. Here, V_{bi} is the built-in voltage drop associated with the Schottky barrier. The resistive components include the fin-channel resistance (R_{fin}), the drift-region resistance (R_{drift}), substrate resistance (R_{sub}), and lumped contact resistance (R_c). Among them, R_{fin} is not a constant and can be modulated by V_F applied to the MOS-structure at the fin sidewall and thus is represented as a variable resistor. With the equivalent circuit established, we have under $V_F > V_{bi}$

$$J_{ON} = \frac{V_F - V_{bi}}{R_{ON}} \tag{2}$$

where J_{ON} is the ON-current density and $R_{ON} = R_{fin}(V_F) + R_{drift} + R_{sub} + R_c$. The apparent differential R_{ON} ($R_{ON,apparent}$) is obtained from (2) by taking derivative with respect to V_F

$$\frac{1}{R_{ON,apparent}} = \frac{dJ_{ON}}{dV_F} = \frac{1}{R_{ON}} - \frac{V_F - V_{bi}}{R_{ON}^2} \cdot \frac{\partial R_{ON}}{\partial V_F}. \tag{3}$$

As V_F increases, R_{fin} decreases due to the reduction of the sidewall depletion width. As a result, the second term at the right-hand side of (3) is positive, resulting in $R_{ON,apparent} < R_{ON}$. This qualitatively explains the observations in Fig. 4. It is worth noting that (3) is universally applicable to all diodes. Thus, one should be cautious about interpreting $R_{ON,apparent}$ as it may be artificially lower than the actual R_{ON}.

For the calculation of R_{fin}, the sidewall depletion width (W_d) is assumed to be constant along the fin channel. The effective conduction width of the fin channel is $2x_0$, where x_0 is the undepleted width within half of the fin channel such that $x_0 + W_d = W_{fin}/2$, as shown in Fig. 8. With such definitions, the specific R_{fin} can be written as $R_{fin} = d_{tr}W_{pitch}/(2eN_D\mu x_0)$, where N_D is the net donor concentration and μ is the electron mobility. Thus

$$\frac{\partial R_{fin}}{\partial V_F} = -\frac{d_{tr}W_{pitch}}{2eN_D\mu x_0^2} \cdot \frac{\partial x_0}{\partial V_F}. \tag{4}$$

The depletion width is modulated by V_F through the electrostatic relationships across the MOS-structure on the sidewall, whose band diagram is also shown in Fig. 8. Technically, the electrostatic potential is distributed from source to drain along the fin channel, but for simplicity, we assume that it can be approximated by a single average value V_{fin}. According to the band diagram, we have

$$V_F - V_{fin} - V_{fb} = -\frac{eN_DW_d^2}{2\varepsilon_s} - \frac{eN_DW_dd_{ox}}{\varepsilon_{ox}} - \frac{eN_{it}d_{ox}}{\varepsilon_{ox}} \tag{5}$$

where $\varepsilon_s = 10\ \varepsilon_0$ is the dielectric constant of Ga_2O_3 and d_{ox} is the thickness of Al_2O_3. By applying $\partial/\partial V_F$ to both sides of (5), $\partial x_0/\partial V_F$ in (4) can be obtained. It can be shown that $\partial N_{it}/\partial V_F = e^2N_DW_dD_{it}\varepsilon_s^{-1} \cdot \partial W_d/\partial V_F$, where D_{it} is the interface-trap density. By using the depletion-layer capacitance $C_d = \varepsilon_s/W_d$, the insulator capacitance $C_{ox} = \varepsilon_{ox}/d_{ox}$, and the capacitance associated with the interface traps $C_{it} = e^2D_{it}$, we have

$$1 - \frac{\partial V_{fin}}{\partial V_F} = eN_D\left(\frac{1}{C_d} + \frac{1}{C_{ox}} + \frac{C_{it}}{C_{ox}C_d}\right) \cdot \frac{\partial x_0}{\partial V_F}. \tag{6}$$

By combining (3), (4), and (6), $R_{ON,apparent}$ as a function of V_F can be obtained. It is convenient to define an effective capacitance $C_{eff} = \left(C_d^{-1} + C_{ox}^{-1} + C_{it}C_{ox}^{-1}C_d^{-1}\right)^{-1}$ and an effective forward bias $V_{F,eff} = (V_F - V_{bi}) \cdot (1 - \partial V_{fin}/\partial V_F)$

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such that

$$R_{\text{ON,apparent}} = \frac{R_{\text{ON}}}{1 + \frac{R_{\text{fin}}}{R_{\text{ON}}} \cdot \frac{C_{\text{eff}} V_{F,\text{eff}}}{e N_D x_0}}. \tag{7}$$

As the model captures the impact of sidewall depletion due to the negative N_{it}, the calculated $R_{\text{ON,apparent}}$ is essentially $R_{\text{ON,dynamic}}$.

Consider a special case when $x_0 = W_{\text{fin}}/2$, i.e., the sidewall depletion is completely overcome by V_F and a flat-band condition is achieved. We approximate V_{fin} by the potential in the middle of the fin channel such that $V_{\text{fin}} \simeq [1 - R_{\text{fin}}/(2R_{\text{ON}})] \cdot (V_F - V_{\text{bi}})$. According to (1), $R_{\text{fin}} = R_2/\text{AR}$. C_d is given by $C_d = \varepsilon_s/L_D$, where $L_D = \sqrt{k_B T \varepsilon_s/(e^2 N_D)}$ is the Debye length [25]. Consequently, we obtain $R_{\text{ON,apparent}}$ under the flat-band condition, which is denoted as $R^*_{\text{ON,apparent}}$

$$R^*_{\text{ON,apparent}} = \frac{R_1 + \frac{R_2}{\text{AR}}}{1 + \left(\frac{R_2}{\text{AR} \cdot R_1 + R_2}\right)^2 \cdot \frac{C_{\text{eff}}(V_F - V_{\text{bi}})}{e N_D W_{\text{fin}}}}. \tag{8}$$

Note that $R^*_{\text{ON,apparent}}$ is essentially $R_{\text{ON,dynamic}}$ at $V_F = V_{\text{stress}}$, where $V_{\text{stress}} \geq 10$ V for $W_{\text{fin}} = 1$ μm and $V_{\text{stress}} \geq 5$ V for $W_{\text{fin}} \geq 2$ μm. This is because under these conditions, V_{stress} is sufficiently high such that sidewall depletion is eliminated, which is precisely the condition where (8) is derived.

By using a measured N_D of $\sim 1 \times 10^{16}$ cm^{-3} in the fin channel [9], a measured V_{bi} of 1.23 V [19], and with D_{it} as the only fitting parameter, we obtained good matches between the calculated $R^*_{\text{ON,apparent}}$ and measured $R_{\text{ON,dynamic}}$ under $D_{\text{it}} = 8 \times 10^{11}$ cm^{-2}eV^{-1}, as shown in Fig. 4. Notably, the dependence on the fin width is well-captured by the model and explains why a smaller difference between $R_{\text{ON,fresh}}$ and $R_{\text{ON,dynamic}}$ is observed in devices with a larger W_{fin}. The extracted D_{it} corresponds only to fast interface traps and thus is not directly related to the previously discussed N_{it}, which includes all trapping effects (from both fast and slow traps). The D_{it} value of 8×10^{11} cm^{-2}eV^{-1} is similar to the D_{it} value we extracted from similar fin sidewall interfaces using the subthreshold swing of fin transistors [7] and comparable with D_{it} values extracted at $(\bar{2}01)$- [33], [34] and (100)-oriented interfaces [35].

In our current device structures, N_{it} on the fin sidewalls cannot be directly measured. Doing so would require dedicated MOS-capacitors fabricated on the sidewalls only. Nevertheless, we can estimate $|N_{\text{it}}|$ after the application of V_{stress} based on the change of the turn-on voltage (V_{ON}). In the trench SBDs with $W_{\text{fin}} = 2 - 4$ μm, $V_{\text{ON}} \sim 1.3$ V is not affect by V_{stress} up to 15 V, indicating that fin channel is not fully depleted at $V_F = V_{\text{ON}}$ even under the presence of N_{it}. Consequently, the upper limit of $|N_{\text{it}}|$ can be estimated from $C_{\text{ox}} V_{\text{ON}}/(2e) + N_D W_{\text{fin}}/2$, of which the first term gives the average sheet charge density balanced by the forward bias and the second term gives the sheet charge density balanced by the space charge in the fin channel under full depletion. Using $W_{\text{fin}} = 2$ μm, the upper limit of $|N_{\text{it}}|$ under $V_{\text{stress}} = 15$ V is estimated to be $\sim 1.3 \times 10^{12}$ cm^{-2}. On the other hand, the turn-on voltage (V_{ON}) of the trench SBDs with $W_{\text{fin}} = 1$ μm increases to ~ 7 V after $V_{\text{stress}} = 15$ V is applied, indicating that the fin channel is fully depleted below V_{ON}. By using the same method, $|N_{\text{it}}|$ of $\sim 2.1 \times 10^{12}$ cm^{-2} is estimated under $V_{\text{stress}} = 15$ V. This value is similar to the value extracted from planar MOS-capacitors [inset of Fig. 2(b)]. However, it is higher than in the case of $W_{\text{fin}} = 2 - 4$ μm, likely due to the fact that the average voltage drop across the sidewall MOS-structure ($V_F - V_{\text{fin}}$) is higher with $W_{\text{fin}} = 1$ μm as a result of a larger R_{fin}.

While the apparent V_{ON} may increase due to the depletion of the fin channels, it is worth noting that the Schottky contact properties (barrier height, ideality factor, and so on) are not affected. Of course, the on–off ratio of the diode may be affected due to the lowering of the ON-current by sidewall interface trapping.

For general cases where $V_F < V_{\text{stress}}$, (7) cannot be easily evaluated, as R_{fin}, R_{ON}, V_F, and C_d are all functions of x_0, which depends on the knowledge of N_{it}. Still, qualitative understanding on the behavior of $R_{\text{ON,apparent}}$ can be obtained. When x_0 is small, $C_{\text{eff}} \propto (W_{\text{fin}}/2 - x_0)^{-1}$, $R_{\text{ON}} \sim R_{\text{fin}} \propto x_0^{-1}$, and $V_{\text{F, eff}} \sim (V_F - V_{\text{bi}})/2$, thus, it can be shown from (7) that $R_{\text{ON,apparent}}$ decreases with increasing x_0. As x_0 increases with increasing V_F during the repeated forward I–V sweeps, $R_{\text{ON,apparent}}$ decreases with increasing V_F. This agrees with the behavior of measured $R_{\text{ON,dynamic}}$ [see Fig. 4]. In addition, as V_{stress} increases, x_0 during the repeated sweeps decreases under the same V_F as a result of more trapped interface charges. Consequently, $R_{\text{ON,apparent}}$ should increase with increasing V_{stress} under the same V_F. Again, this correctly captures the behavior of $R_{\text{ON,dynamic}}$ measured experimentally.

V. Conclusion

We investigated the ON-resistance of β-Ga_2O_3 trench-MOS SBDs under both fresh and forward-bias stressed conditions to uncover the role of sidewall interface trapping. Repeated C–V measurements on planar MOS-capacitors reveal an increase of negative interface-trapped charge density under increasing forward-bias stress voltage, with very slow detrapping at room temperature ($\gg$10 s of seconds). On the other hand, forward-bias voltage stressing of trench SBDs induces current collapse and a delayed turn-on behavior as a result of sidewall depletion due to the negative N_{it}. The sidewall depletion can be eliminated with sufficiently high forward bias. Interestingly, the differential dynamic R_{ON} from the repeated forward I–V sweeps is lower than the differential fresh R_{ON}. This apparently anomalous behavior is due to the modulation of fin-channel resistance by the forward bias under the presence of the negative N_{it}. Both the fresh and dynamic R_{ON} are well-modeled analytically, and a D_{it} value of 8×10^{11} cm^{-2}eV^{-1} is extracted at the (100)-like sidewall interfaces. This study reveals the importance of the sidewall interface quality to trench-MOS SBDs in general and points out that one should excise caution when interpreting the apparent differential R_{ON}, which could be artificially lowered due to the voltage dependence of R_{ON}.

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