Breakdown Mechanisms in β-Ga_2O_3 Trench-MOS Schottky-Barrier Diodes

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***Abstract*— The breakdown mechanisms of >1kV β-Ga_2O_3 trench-MOS Schottky-barrier (SB) diodes (SBDs) are investigated during step-stressed voltage measurements. We demonstrate the use of current leakage noise to characterize leakage mechanisms. Comparing the normalized current noise characteristics of a set of trench-MOS SBDs to a metal-oxide-semiconductor capacitor (MOS-CAP) and a planar SBD test structure, the origin of two leakage mechanisms can be discerned. At low biases, leakage is dominated by barrier tunneling at the SB interface. At higher biases, non-reversible soft-breakdown events are observed, with a sharp increase in leakage current associated with breakdown at the oxide interface. Beyond these non-reversible soft-breakdown events, localized Al_2O_3 leakage paths dominate the leakage noise signature. Changes in the dominant leakage mechanism, under reverse bias stress, have implications for the voltage ratings and lifetimes of reduced surface electric field (RESURF) devices that incorporate oxide layers for enhanced breakdown fields.**

***Index Terms*— Breakdown mechanisms, current noise, degradation, Ga_2O_3, MOS-CAP, Schottky diodes, trench-MOS, vertical power devices.**

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I. Introduction

β-Ga_2O_3-based devices are promising in both power and RF applications [1]. A bandgap of 4.9 eV and breakdown field of 8 MV/cm allow for high-voltage operation, beyond the capabilities of GaN and SiC [2]. Significant progress has already been made in the field of power devices, with breakdown voltages as high as 8 kV reported in lateral devices [3]. However, increasing breakdown voltage in lateral devices intrinsically reduces the current handling.

Vertical devices offer a path to realizing a high current density device, with breakdown voltages higher than that of competing wide bandgap semiconductors. As a unipolar semiconductor [4], the fabrication of β-Ga_2O_3 Schottky-barrier (SB) diodes (SBDs) offers the most promising route to achieving vertical devices with high-field handling. Planar SBDs with average breakdown fields at the SB of 5.7 MV/cm and corner fields as high as 7 MV/cm have been reported [5]. Reduced surface electric field (RESURF) techniques have been successfully demonstrated in trench-MOS SBDs, to reduce the field at the SB interface of planar diodes [6].

Failure points of trench-MOS SBD structures are well understood under bias-swept conditions [7], [8]. However, it is critical to understand how OFF-state leakage mechanisms evolve under constant bias stress, as this more accurately mirrors the real-world reliable operation of the devices. In this work, we demonstrate a transition between two distinct leakage mechanisms in a trench-MOS SBD, during a step-stressed breakdown measurement. Analysis of the current noise during step-stressed measurements indicates a low-voltage leakage current through the SB, and a transition to leakage through the passivating oxide at higher voltages.

II. Experimental Details

Vertical trench-MOS β-Ga_2O_3 SBDs were studied with fin widths and separations ranging from 1 to 3 μm, with a fin height of 1.1 μm, and a drift region with a thickness of 10 μm, as shown schematically in Fig. 1(a), with the edge-termination of the field plate shown in Fig. 1(e). Details of the device fabrication can be found in Li [7]. The trenches are lined with a 105 nm ALD Al_2O_3 layer. A Ti/Au layer at the bottom of the substrate formed a cathode, while a Ni anode

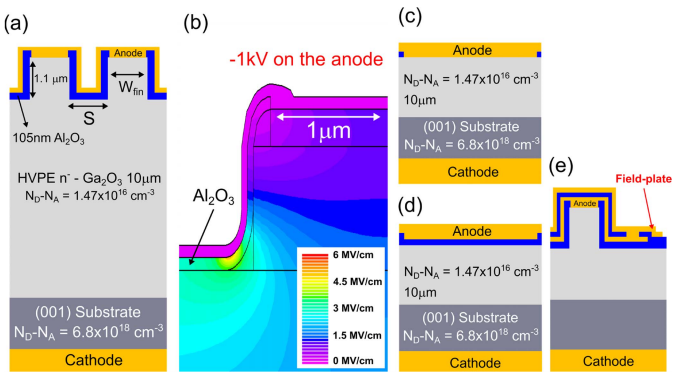

Fig. 1. (a) Schematic of a trench-MOS β-Ga_2O_3 SBD, with 10 μm drift region. The fin height is 1.1 μm, with a variable fin width (W_{fin}) and fin separation (S). (b) Field distribution of a diode corner, with a fin separation of 2 μm and a fin width of 2 μm (-1 kV applied to the anode). Peak fields were observed at bottom of trench, in the oxide corners. (c) Field-plated Planar SBD and (d) field-plated MOS-CAP structures. (e) Edge-termination of the trench-MOS SBD structure, shown in (a).

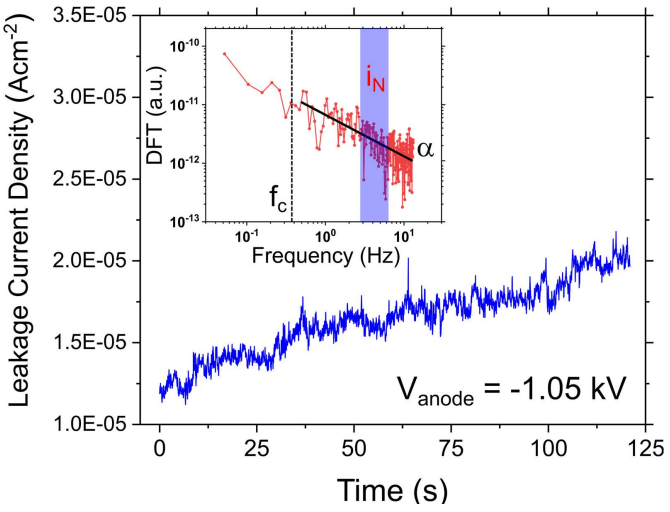

Fig. 2. Example of leakage current noise (for a diode fin width = 1.5 μm and fin separation = 1.5 μm), with an anode bias of -1.05 kV. DFT of current noise is shown in the inset, with the position of the high pass filter (f_c), and the log-spaced window used to extract i_N marked. A linear fit of the DFT slope is used to extract the spectral power density exponent, α.

was deposited across the fin tops and conformally coated the dielectric in the trenches. The presence of the sidewall metal achieves a RESURF effect within the fins. This RESURF effect is demonstrated by the TCAD simulations shown in Fig. 1(b), simulated using SILVACO ATLAS; the peak field is shifted from the metal–semiconductor interface at the top of the fin to the oxide-coated fin corners. For all simulations, the trench bottom corner of the trench-MOS SBD was modeled as a curved surface, with the same radius of curvature for all structures. This radius of curvature was set to 200 nm, based on FIB cross-section reported in [7].

To study the breakdown of trench-MOS SBDs under reverse bias, step-stress measurements were performed, with the sample wafer submerged in Fluorinert. The anode was biased for a period of 120 s, in steps of -50 V up to breakdown. To achieve the voltage step, the anode was ramped at -0.5 V/s for a period of 100 s; this slow ramp was found to be essential to avoid early breakdown. The leakage current was measured, at each voltage plateau, via a virtual-grounded metal chuck, in contact with the cathode. A Keithley 2636B source meter was used to measure the cathode leakage current, while a Keithley 2657A 3kV source meter was used to apply a negative bias to the anode. The measurement system's current resolution was 10 fA.

The current noise at each step of the step-stress measurement was quantified using the method previously outlined by Dalcanale [9]. Following each voltage ramp, the leakage current through the anode was sampled at a frequency of approximately 26 Hz, while the device was held at constant bias, as shown in Fig. 2. A discrete Fourier transform (DFT) of the leakage current was taken, using a Hann windowing function, as shown in the inset of Fig. 2. The sampling rate limited the upper frequency detection limit to 13 Hz, and the 120 s step duration gave a frequency resolution of 8.33 mHz. Over the frequency range 0.3–13 Hz, the DFT was divided into five equal log-frequency spaced bins. The noise power spectral density exponent, α, was extracted by fitting a slope to the averaged values of each window (see inset). A window, covering the range 2.9–6.2 Hz, was used to extract a noise current (i_N), as shown in the inset of Fig. 2. The distribution of amplitudes within the central window was fitted using a Weibull distribution, with the shape factor giving the noise current i_N. To separate changes in i_N caused by device degradation from changes caused by an increase in leakage current, the normalized noise current (NNC) is used, with i_N being normalized to the averaged leakage (i_{Av}) current during each step.

III. Results

A. Simulated Field Profiles

Silvaco ATLAS 2-D simulations were performed for a range of device dimensions. The bandgap of β-Ga_2O_3 at 300 K was set to 4.9 eV and the electron mobility to 200 $cm^2V^{-1}s^{-1}$. The dielectric constant of β-Ga_2O_3 was set to 10 and Al_2O_3's dielectric constant to 12. The models used in the simulations were Fermi–Dirac statistics and Shockley–Read–Hall statistics. Fig. 3 shows the electric field at the center of the SB interface, for fins of varying width and a fixed fin separation of 1 μm. For fins with widths <25 μm, the field scaling with voltage is weaker than that of a planar SBD, i.e., field clamping is observed. All devices used in this study have fin widths <3 μm, and so we expect the RESURF effect to be present in all devices studied [7], [8].

Fig. 4 shows the impact of fin separation on the field profile across the width of a fin, with the cutline taken across the bottom of the fin, offset 1 nm below the β-Ga_2O_3–oxide interface (in the trenches). Fin separation is observed to have an insignificant effect on the peak fields close to the oxide corners, while fields in the trench bottom (either side of the fin) are observed to increase with decreasing fin separation. This suggests that fin separation should have a minimal impact on the breakdown voltage of the device over the range of fields considered.

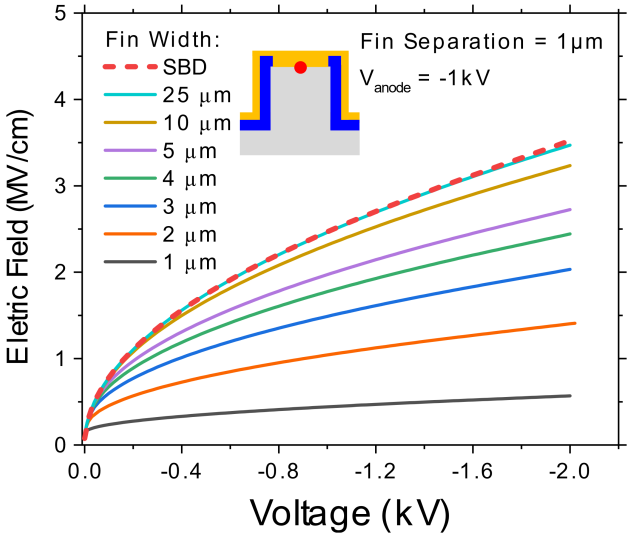

Fig. 3. Simulated field-voltage scaling at the anode for fins with a constant fin separation (fin separation = 1 μm), and varying fin widths. The loss of sidewall clamping in wider fins is demonstrated, with the field at the center of the 25 μm fin scaling like that of a planar interface. The red dot on the device schematic indicates the position at which the field was determined in the simulation.

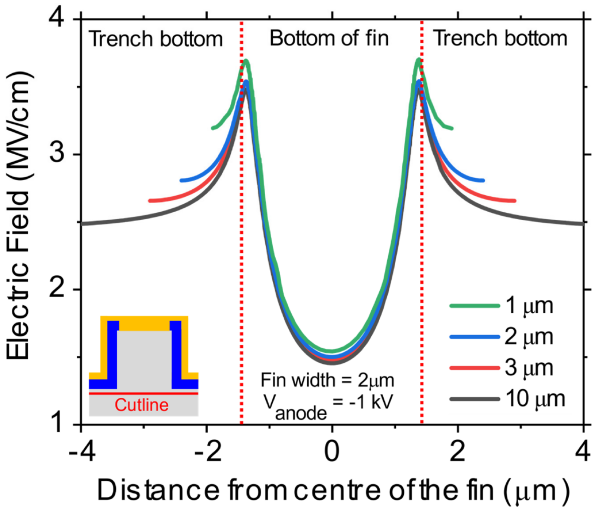

Fig. 4. Simulated field profiles for a variety of fin separations (fin width = 2 μm), with the cutline taken at 1 nm below the Ga_2O_3–oxide interface in the bottom of the trenches on either side of the fin (indicated in the bottom left inset). The red dotted lines indicate the approximate boundaries between the bottom of the fin and the trench bottom. The peak fields are approximately constant across all geometries, with the fields below the Ga_2O_3–oxide interface in the trench bottoms increasing with decreasing fin separation.

B. Leakage Current Noise Measurements

Fig. 5 shows the leakage current of three representative trench-MOS SBDs, with differing dimensions. The leakage current is observed to increase slowly with increasing bias, for biases <0.5 kV. All diodes exhibit two distinct types of soft-breakdown events. The first is characterized by reversible spikes in leakage current during a voltage step, with little change in the leakage baseline, as shown in the inset of Fig. 5. The second soft-breakdown behavior is characterized by a sharp increase in the leakage current between voltage

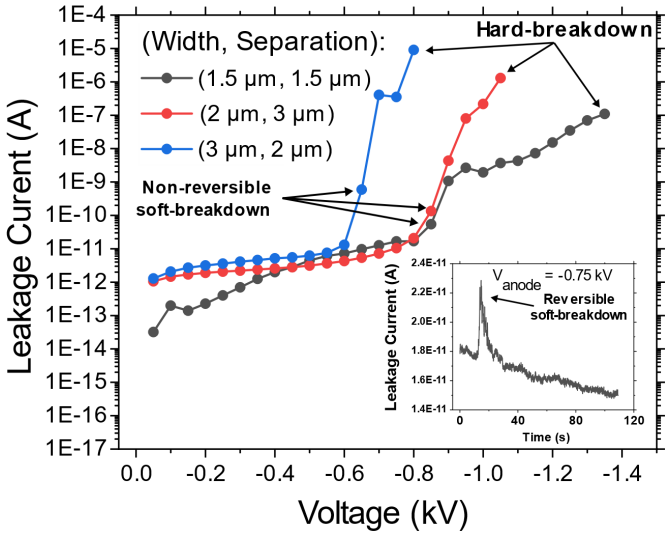

Fig. 5. Stepped-stress leakage characteristics of a representative set of trench-MOS SBDs. Between each voltage step, the anode is ramped over the period of 100 s (leakage here not shown). System resolution is 10 fA. The leakage current is resolution limited at biases lower than 100 V. Non-reversible soft-breakdown voltages are taken to be the first voltage at which an elevated leakage current is observed. The final voltage step defines the breakdown voltage of each device. (Inset: Leakage current of the fin width = 1.5 μm diode at −0.75 kV. A reversible soft-breakdown event, characterized by the presence of current spike, is labeled.)

steps. This jump in leakage current is non-reversible. After the non-reversible soft-breakdown event has occurred, the reversible current spikes are no longer observed. At higher voltages than that of the non-reversible soft-breakdown, hard-breakdown of the device is observed. Hard-breakdown of the devices is characterized by a sudden increase in device current to the measurement compliance of 1 mA, with the corresponding breakdown voltage being the voltage of the final voltage step (Fig. 5). The hard-breakdown voltage is not observed to strongly correlate with the fin width or fin separation due to the limited number of devices tested in this study. It is expected that the breakdown will not be impacted significantly by changes to the fin separation (see Fig. 4), while any dependence of the breakdown voltage on fin width would only be apparent after measuring a sufficiently large number of devices, as demonstrated in [7], owing to non-uniformity in device epi-quality and processing variations [7]. There was also no strong dependence of either leakage current or soft-breakdown voltage on fin width or separation, with the variation between diodes with the same geometry being comparable to the variation between those with different geometries.

The corresponding noise analysis of the trench-MOS SBD's leakage currents, in Fig. 5, is shown in Fig. 6. The non-reversible soft-breakdown events are labeled, with the voltage defined as the first step in which an elevated leakage current is observed. Across all measured diodes, a generic behavior was observed: There is a decrease in the NNC before the non-reversible soft-breakdown event, albeit with some variation in magnitude. Following this soft-breakdown, the NNC increases, and stays approximately constant until hard-breakdown. The NNC magnitude following soft-breakdown was broadly similar for all devices.

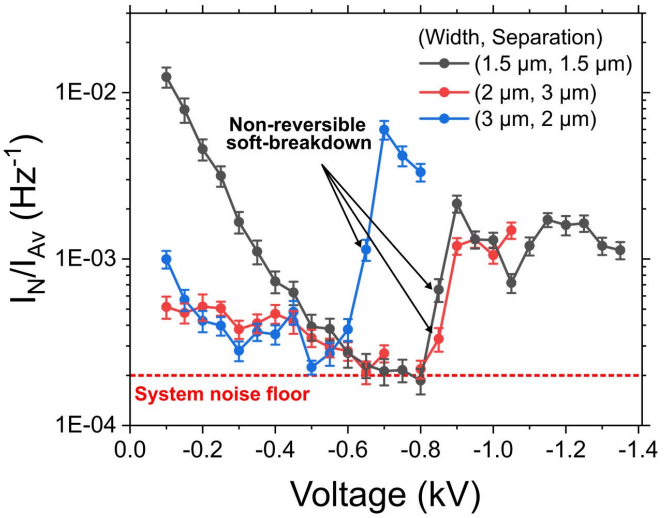

Fig. 6. NNC for a representative set of trench-MOS SBDs. The non-reversible soft-breakdown events in each diode lead to a jump in the noise level. Points below 100 V are disregarded due to the current resolution of the system.

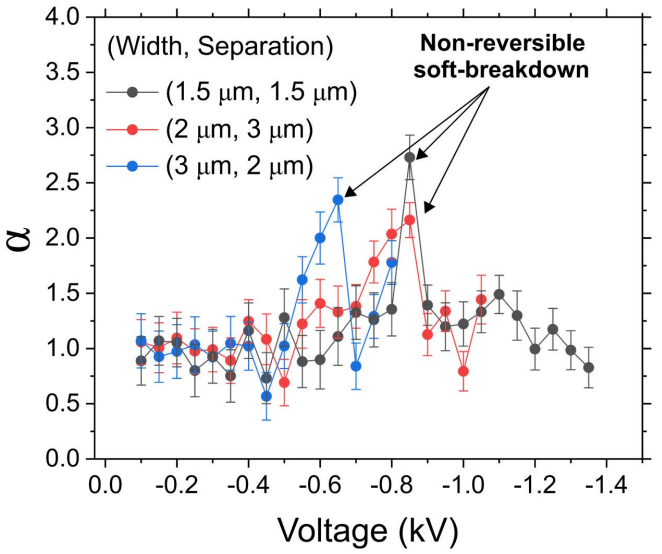

Fig. 7. Power spectral density exponent extracted at each voltage step, for all three diodes in Figs. 5 and 6. The voltage steps at which each non-reversible soft-breakdown event occurs are labeled. Points below 100 V are disregarded due to the current resolution of the system.

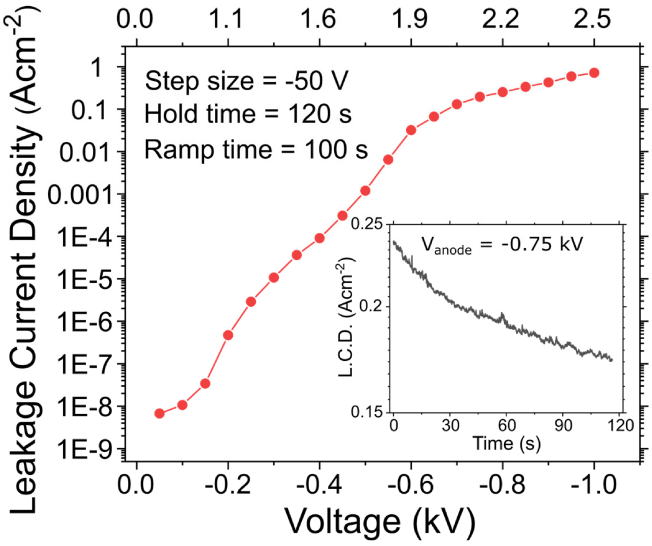

Fig. 8. Stepped-stress leakage characteristics of a planar SBD, diameter = 90 μm. Between each voltage step, the anode is ramped over the period of 100 s (leakage here not shown). The corresponding values of field are extracted from simulations, 10 nm below the semiconductor–metal interface at the center of the SBD. (Inset: Time dependence of leakage current at −0.75 kV.)

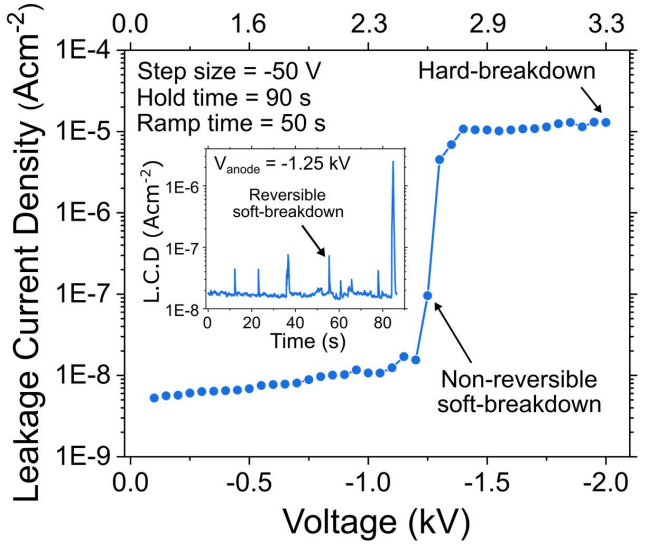

Fig. 9. Stepped-stress leakage characteristics of a MOS-CAP structure with dimensions 160 × 170 μm. Between each voltage step, the anode is ramped over the period of 50 s (leakage here not shown). The corresponding values of field are extracted from simulations. (Inset: Leakage current at −1.25 kV. Reversible soft-breakdown events, characterized by the presence of current spikes are visible throughout the measurement.)

The power spectrum exponent, α, is extracted at each voltage step in Fig. 5. At low voltage, all diodes exhibit an exponent of ∼1, corresponding to 1/f noise, as shown in Fig. 7. The exponent increases to a value of ≥2 before the non-reversible soft-breakdown, dropping to a value close to 1 immediately after soft-breakdown. The presence of the obvious reversible current spikes did not have a significant impact on the value of alpha at each voltage step; removing those current spikes from each step shifted α by a value within error of the original value.

In order to understand the origin of the leakage current and noise current in the trench structure, we analyze possible leakage paths using both MOS-CAP structures and a planar SBD structures [Fig. 1(c) and (d)]. Using these structures, it is possible to isolate the leakage behavior of the oxide layer and the SB interface. The step-stress breakdown characteristic of a planar SBD is shown in Fig. 8. The leakage current increases with each voltage step. The leakage current at −0.75 kV, shown in the inset, is representative of the behavior at all voltage steps, with no current spikes observed. A non-reversible soft-breakdown event is not observed over the course of the measurement, with a hard-breakdown at −1 kV.

Fig. 9 shows the breakdown characteristics of a MOS-CAP structure. Unlike the SBD structure, the leakage current of this device remains approximately constant below 1 kV. The

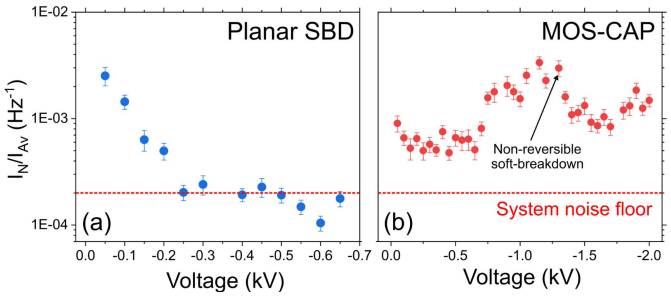

Fig. 10. NNC at each voltage step. (a) Planar SBD with a ramp time of 100 s and voltage hold of 120 s. Above 200 V, the system noise floor is reached. (b) 160 × 170 μm MOS-CAP structure with a ramp and hold time of 70 s.

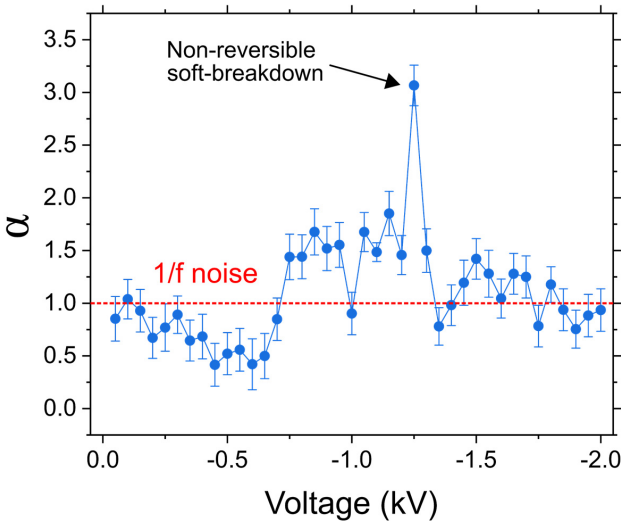

Fig. 11. Power spectral density exponent extracted at each voltage step for the MOS-CAP structure. The voltage step of the non-reversible soft-breakdown event is labeled.

MOS-CAP undergoes a non-reversible soft-breakdown event above 1 kV, indicated by the sharp jump in leakage current, and a hard-breakdown event, at approximately 2 kV. The current spikes, characteristic of reversible soft-breakdown, are observed for all measured MOS-CAPs (see inset). These spikes are observed for voltages >50 V, with a significant increase in their frequency as the non-reversible soft-breakdown voltage is approached. They are not observed after the soft-breakdown, although they may simply be obscured by the orders of magnitude increase in the leakage current.

The NNC for both the planar SBD and the MOS-CAP structures is shown in Fig. 10. The noise current for the planar SBD decreases as voltage increases, as shown in Fig. 10(a). In contrast, for the MOS-CAP, the NNC varies around a level of approximately 2×10^{-3} Hz^{-1} both before and after soft-breakdown [Fig. 10(b)]. All measured MOS-CAP structures exhibit similar behavior. We note, with reference to Fig. 3, the voltage range covered in Fig. 10(a) covers all relevant fields observed in the trench-MOS diodes. Although the hard-breakdown voltage of the 3 μm is the lowest (Fig. 5), the breakdown field is highest, because of the stronger scaling of field with voltage in the 3 μm fin, when compared to 2 μm (see Fig. 3). Therefore, the highest surface field, across the SB interface, reached in Fig. 5 is 1.35 MV/cm, at −0.8 kV for the fin width = 3 μm, which is equivalent to −0.3 kV for a planar SBD.

Fig. 11 shows the power spectrum density exponent α as a function of voltage for the MOS-CAP structure. An increase in α is observed, from <1, to approximately 1.5 before the non-reversible soft-breakdown event. After soft-breakdown, 1/f noise is observed.

IV. Discussion

The trench-MOS SBD's leakage currents (Fig. 5) can be attributed to two distinct leakage paths; leakage at the SB interface, and leakage through the trench bottom oxide corners and trench bottom oxide. Leakage through the fin side wall is unlikely as the RESURF effect reduces the fields in these regions [see Fig. 1(b)]. The NNC for the trench structure, Fig. 6, shows the presence of these two distinct noise regimes during the step-stressed measurement. In the first, from −0.1 kV until soft-breakdown, a linear decrease in $\log_{10}(i_N/i_{Av})$ is observed across all diodes. The second regime, observed after soft-breakdown, is characterized by a sharp increase in the noise current until hard-breakdown. Decomposing the trench-MOS SBD structure into constituent components, the normalized noise appears to be a composite of the behavior observed in the planar SBD and the MOS-CAP structure.

The low voltage noise behavior (below the non-reversible soft-breakdown voltage) of the trench-MOS SBD can be explained with reference to the noise current of the planar SBD structure in Fig. 10(a). The low voltage noise behavior of the trench-MOS SBDs and the noise behavior of the planar SBD are qualitatively the same, with a linear decrease in $\log_{10}(i_N/i_{Av})$ with voltage. This suggests that in the first regime (Fig. 6), the noise and leakage currents in the trench-MOS are mediated by the bulk leakage current over the SB interface.

Simulations of the planar SBD suggest that the maximum field over the metal–semiconductor interface, far away from the device edges observed in Fig. 8, is 2.5 MV/cm. The field at the first voltage step (−50 V) is 0.55 MV/cm. Above 0.2 MV/cm the dominant leakage mechanism across the SB is barrier tunneling, as demonstrated by Li [10]. This leakage mechanism should lead, in the absence of barrier degradation, to a reversible leakage current. Indeed, no change or degradation was observed for multiple voltage sweeps over the range of 0–0.4 kV (not shown). The decrease in NNC as a function of voltage, observed for the planar SBD in Fig. 10(a), can be explained by the relative scaling of the noise current i_N and the leakage current. i_N was observed to increase during the measurement, but the absolute leakage current scaled more quickly. As a result, normalizing i_N to the leakage current leads to a decreasing NNC.

While the low voltage behavior of the trench-MOS SBDs can be explained with reference to the planar SBD structure, the high voltage noise behavior can be explained with reference to the MOS-CAP noise current, Fig. 10(b). Both reversible and non-reversible soft-breakdown events occur for

both structures. It seems reasonable that these events are related to a time-dependent breakdown mechanism over the oxide interface, as described in [11]. The leakage current observed before the non-reversible soft-breakdown (Fig. 9) is possibly mediated by preexisting defects in the oxide layer. Both the MOS-CAP structures and the trench-MOS SBDs exhibit non-reversible soft-breakdown events, and both have an approximately constant NNC after these events. This suggests that the non-reversible soft-breakdown event in the trench structures is related to a change in the dominant leakage path, from the SB interface at lower voltages to a newly seeded leakage path in the oxide layer at higher voltages.

The seeding of highly resistive soft-breakdown paths in oxide layers has been previously discussed by Degraeve [12]. Degradation of this type is consistent with the jump in NNC after the non-reversible soft-breakdown events shown in Fig. 6. An increase in NNC suggests that any increase in leakage current is preferentially confined to a localized leakage path, as opposed to an increase in the number of leakage paths [13]. A transition from bulk leakage at the SB interface to leakage through a leakage path in the oxide represents a transition to a more localized current path with a correspondingly smaller number of fluctuators responsible for the noise. Hence there is an increase in the fractional change in current associated with changes in trap occupancy and an increase in the NNC.

Degradation of the oxide layer is furthermore supported by the change in the power spectral density exponent during the breakdown measurements of trench-MOS SBD, Fig. 7. The value of $\alpha = 1$ at low voltages is indicative of 1/f noise associated with uncorrelated bulk leakage across an interface [14]. This value was then observed to increase from $\alpha = 1$ to $\alpha = 2$ before the non-reversible soft-breakdown event. In this region, reversible soft-breakdown current spikes are observed as seen in Figs. 5 and 9 inserts. We note that the FFT of an impulse has $\alpha = 2$, so the increase in α is consistent with the presence of multiple current spikes. The fact that α was unchanged by the removal of the obvious spikes would suggest the presence of multiple impulse (reversible soft-breakdown) events on a timescale too short to be resolved in the measurement. These spikes and soft-breakdown events are absent in the planar SBD, but present for the MOS-CAP breakdown measurements (Fig. 9). Following the irreversible soft-breakdown $\alpha = 1$, and is consistent with the permanent degradation of the oxide layer via the formation of a percolation path, as discussed in [12] and [13]. A similar behavior is observed in the MOS-CAP structure, Fig. 11, while the value of α is approximately 1 for the planar SBD structure throughout the measurement.

The hard-breakdown of the MOS-CAP structure occurs at a voltage of approximately 2 kV, which corresponds to a field of 3.3 MV/cm in the bulk of the oxide (Fig. 9). Similar breakdown voltages/fields were observed across all measured MOS-CAP structures. This is lower than the oxide breakdown field consistently observed at the device field corners described by Li [7], during swept-voltage breakdown measurements of trench-MOS diodes. This discrepancy can be explained by a degradation of the oxide under high bias stress. The stepped stress measurements performed in this study subjected the oxide layer in each device to a prolonged bias stress, when compared to breakdown measurements in which the voltage is swept at a constant rate [7]. This prolonged bias stressing will lead to charging and defect creation in the oxide, triggering premature breakdown.

While the RESURF effect significantly enhances the breakdown voltages of these trench-MOS SBDs, the transition of the leakage mechanism under prolonged bias stress ultimately leads to device failure. The design and deposition of the dielectric layer in these devices require careful consideration to avoid a significant reduction in the operating voltages of real-world devices. This challenge is fundamental in all devices employing MOS/MIS junctions to implement RESURF effect (i.e., field plating and junction termination extension technologies), including both lateral devices such as high electron-mobility transistors and vertical devices such as trench SBDs [3], [5], [8]. Li [15] and Allerstam *et al.* [16] argued that the challenge of managing high electric fields is particularly acute in (ultra)wide bandgap semiconductors, insofar that the semiconductor can sustain an electric field higher than the practical electric field in the insulator. For example, considering the breakdown field of a widely used wide bandgap semiconductor and dielectric, the practical achievable field in GaN is ~3 MV/cm versus ~2 MV/cm in SiO_2(including the effect of TDDB). One way to cope with this challenge is to develop Schottky or p-n junctions with sufficiently high energy barriers [17], [18], for instance, a barrier height of >2.5 eV for Ga_2O_3 is necessary to reach 6 MV/cm in Ga_2O_3. Schottky or p-n junctions allow the current to flow through the junction without undergoing TDDB as in a MOS/MIS junction, therefore, presenting an attractive solution to this challenge [16].

V. Conclusion

In this work, we have demonstrated that, under bias stressing of trench-MOS β-Ga_2O_3 SBDs, the dominant leakage mechanism transitions from the SB to a degraded Al_2O_3 dielectric layer. This has significant implications for the applications and suitable voltage range for β-Ga_2O_3 trench-MOS SBDs. The higher achievable breakdown voltage afforded by the RESURF technique introduces potentially life-limiting fields in the Al_2O_3. This merits further investigation into the mean time to failure of such structures, for more realistic upper voltage limits. This study highlights the importance to develop suitable MOS/MIS junctions, as well as high-barrier Schottky and p-n junctions in (ultra)wide bandgap semiconductors to harness the high field afforded by these materials.

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