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# In Situ Crystalline AlN Passivation for Reduced RF Dispersion in Strained-Channel AlN/GaN/AlN High-Electron-Mobility Transistors

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**The recent demonstration of $\approx$ 2 W mm$^{-1}$ output power at 94 GHz in AlN/GaN/AlN high-electron-mobility transistors (HEMTs) has established AlN as a promising platform for millimeter-wave electronics. The current state-of-art AlN HEMTs using ex situ-deposited silicon nitride (SiN) passivation layers suffer from soft gain compression due to trapping of carriers by surface states. Reducing surface state dispersion in these devices is thus desired to access higher output powers. Herein, a potential solution using a novel in situ crystalline AlN passivation layer is provided. A thick, 30+ nm-top AlN passivation layer moves the as-grown surface away from the 2D electron gas (2DEG) channel and reduces its effect on the device. Through a series of metal-polar AlN/GaN/AlN heterostructure growths, it is found that pseudomorphically strained $\leq$15 nm thin GaN channels are crucial to be able to grow thick AlN barriers without cracking. The fabricated recessed-gate HEMTs on an optimized heterostructure with 50 nm AlN barrier layer and 15 nm GaN channel layer show reduction in dispersion down to 2 $-$ 6% compared with 20% in current state-of-art ex situ SiN-passivated HEMTs. These results demonstrate the efficacy of this unique in situ crystalline AlN passivation technique and should unlock higher mm-wave powers in next-generation AlN HEMTs.**

## 1. Introduction

With the need for faster electronic communication and high bandwidths in both commercial and defense application spaces, there is a growing demand of high-power signal amplification in the millimeter-wave (mm-wave) frequency range of 30–300 GHz. III-nitride semiconductors are the premier materials of choice for mm-wave power amplifiers (PAs) because of their wide bandgaps and high electron saturation velocities.[1] Thanks to suitable material properties and over two decades of scientific and technological development and commercialization, GaN high-electron-mobility transistor (HEMT)-based PAs have demonstrated power outputs in the mm-wave frequency higher than competing material technologies such as Si, GaAs, and InP. Current state-of-art GaN PAs have demonstrated exceptional output powers of 40 W mm$^{-1}$ and 30 W mm$^{-1}$ at 4 and 8 GHz, respectively, in field-plated metal-polar GaN HEMTs,[2,3] 15 W mm$^{-1}$ in X-band (7–11 GHz) GaN HEMTs on AlN,[4] and >8 W mm$^{-1}$ at upto 94 GHz using N-polar GaN HEMTs.[5,6]

The ultrawide-bandgap semiconductor aluminum nitride (AlN) is a newly emerging platform[7] for mm-wave integrated circuits (MMICs). It offers the possibility of integrating both active components such as p- and n-channel transistors for PAs, low-noise amplifiers (LNAs), and radio frequency (RF) CMOS and passive components such as AlN bulk acoustic wave (BAW) filters[8] and SiC substrate-integrated waveguides (SIWs).[9] The workhorse of this platform is the scaled AlN/GaN/AlN HEMTs-based amplifiers that can be used for both PAs and LNAs to transmit and receive functions. These AlN HEMTs promise mm-wave signal amplification at power levels higher than those measured currently in GaN HEMT-based PAs. The high thermal conductivity (340 W mK$^{-1}$), high breakdown field[10,11] of AlN, and larger polarization and band offset with respect to GaN are expected to boost the performance of AlN HEMTs. This has led to a rising interest of the community in these AlN buffer-based HEMT heterostructures. There have been numerous reports of epitaxial growth of AlN/GaN/AlN and AlGaN/GaN/AlN structures using different techniques and substrates.[12–18] These heterostructures have been used to demonstrate AlN-based HEMTs for RF amplification[4,10,14,16,18] and high-power switching applications.[11,19]

In particular, recent AlN HEMTs on SiC[4,20,21] have made giant strides toward fulfilling the promise of high-mm-wave

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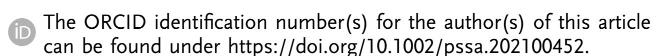
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**DOI: 10.1002/pssa.202100452**

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output powers at frequencies upto 94 GHz. They have shown good direct current (DC) characteristics with high on-currents of $>3$ A $mm^{-1}$ and small-signal characteristics with $f_T/f_{MAX}$ of 123/233 GHz. The state-of-art-scaled T-gate AlN/GaN/AlN HEMTs on SiC have demonstrated output powers of 3.3/2.2 W $mm^{-1}$ at 10/94 GHz, respectively, without field plates.[20,21] In addition, AlGaN/GaN/AlN HEMTs on single-crystal AlN substrates recently demonstrated phenomenal 15 W $mm^{-1}$ in the X-band,[4] further demonstrating the potential of this platform for high-power amplification. Although these results are remarkable for device technology early in its development stage, they are still below the state-of-art GaN HEMTs' output powers of upto 8 W $mm^{-1}$ at 94 GHz.[6,22,23] It was found[21] that the DC-RF dispersion due to surface states is what limits the capability of the current generation of AlN HEMTs to truly achieve its potential.

**Figure 1**b shows the cross section of the current state-of-art AlN/GaN/AlN RF HEMTs.[21] Positively charged surface donor states are expected to be present on the as-grown heterostructure surface, which is ≈6 nm away from the 2D electron gas (2DEG) channel. If these surface states are not controlled or passivated, they capture electrons from the transistor channel and cause current collapse and DC-RF dispersion under large signal operation.[24,25] The typical way to counter this effect is to deposit silicon nitride (SiN) to passivate the surface states after HEMT fabrication.[26,27] For the AlN HEMT in Figure 1b, ex situ SiN passivation layer was deposited using plasma enhanced chemical vapor deposition (PECVD) as the last step in the HEMT fabrication process. Pulsed $I_D$–$V_D$ measurement results of these devices are shown in Figure 1a. The device demonstrated an on-current dispersion of ≈20% and ≈1 V knee voltage walkout for quiescent gate/drain biases of −6/10 V. This dispersion translates to soft gain compression in large-signal measurement results[21] at high input powers. Clearly, ex situ SiN passivation is not completely successful in suppressing RF dispersion from the surface states in these devices. A more effective passivation of these surface states is hence desired to unlock the true potential of the AlN/GaN/AlN HEMTs and exceed power outputs of the state-of-art GaN HEMTs.[5,6]

In this work, we propose and demonstrate a solution to control DC-RF dispersion using an in situ crystalline AlN passivation scheme for AlN/GaN/AlN HEMTs. The proposed scheme is shown in Figure 1c. Instead of a thin, ≈5 nm AlN barrier, a thick, >30 nm AlN layer is grown on top of a compressively strained GaN channel. In addition to acting as the electrostatic barrier layer for the 2DEG, this AlN layer takes the as-grown surface far from the 2DEG channel and hence reduces carrier trapping. We show experimentally that the GaN channel layer should be pseudomorphically strained to the AlN buffer layer for this scheme to work. A thin <15 nm GaN channel layer maintains in-plane compressive strain >2% and consequently allows the growth of the 30+ nm-thick crack-free AlN passivation layer on top. Low-sheet-resistance 2DEG is demonstrated over one-quarter of the 4 in. wafer. Demonstration devices are fabricated using a new recessed-gate AlN HEMT process. Pulsed $I_D$–$V_D$ measurements on these devices show a reduced DC-RF dispersion of 2 − 6%, the best device showing a 10× reduction compared with the ≈20% dispersion seen in ex situ SiN-passivated AlN HEMTs. These results confirm the efficacy of this new in situ passivation technique to help increase the high-power RF performance of next-generation AlN HEMTs.

## 2. Results

The metal-polar AlN/GaN/AlN HEMT heterostructure consists of a top AlN barrier layer, a thin GaN channel layer, and a >0.5 μm-thick AlN buffer layer epitaxially grown on a resistive 6H silicon carbide (SiC) substrate. The relatively low lattice mismatch of <1% AlN with respect to SiC enables the heteroepitaxial growth of 0.5–1.0 μm-thick, crack-free AlN buffer layers on

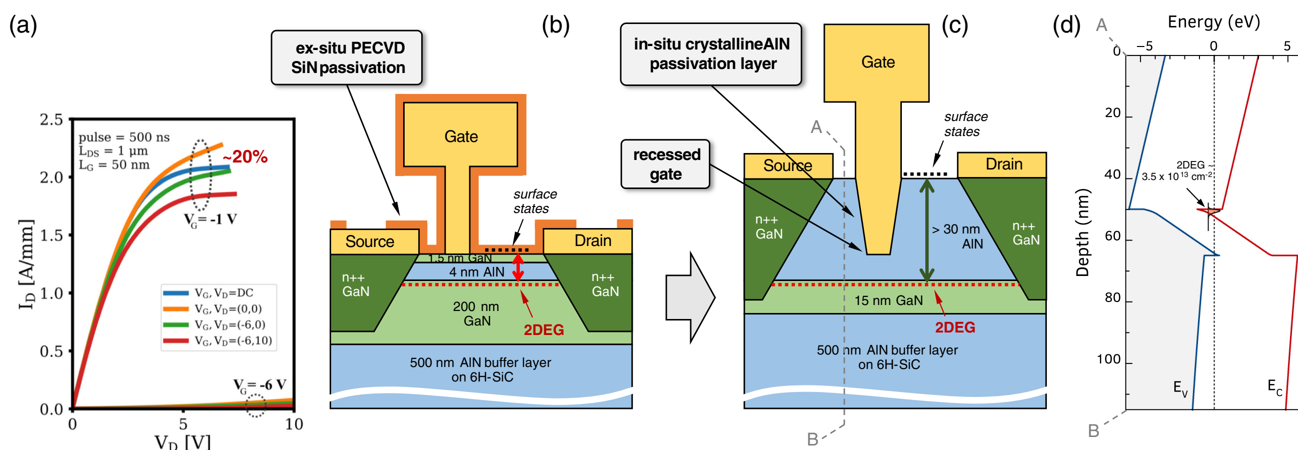


Figure 1. a) Pulsed $I_D$–$V_D$ measurement results for the current state-of-art AlN/GaN/AlN RF HEMTs. Hickman et al.,[21] showing a ≈20% DC-RF dispersion due to surface states. Reproduced with permission.[21] Copyright 2021, IEEE. b) Schematic of the state-of-art AlN/GaN/AlN RF HEMTs with ex situ SiN passivation. The surface states on the as-grown surface are present ≈6 nm away from the 2DEG and are not effectively suppressed using PECVD SiN. c) Schematic of the proposed AlN/GaN/AlN HEMT with in situ crystalline AlN passivation layer. A >30 nm AlN top layer acts both as a barrier for the 2DEG and makes sure that the surface states are far from the 2DEG channel. A recessed gate is required to keep the gate close to the channel and maintain the transconductance and speeds. d) A self-consistent 1D Schrodinger−Poisson band simulation[28] of an as-grown AlN/GaN/AlN structure with 50 nm of AlN passivation layer and 15 nm GaN channel layer. A 2DEG of density ≈ $3.5 \times 10^{13}$ $cm^{-2}$ is expected at the top AlN/GaN interface.


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SiC. In addition, the high thermal conductivity of SiC makes it a suitable substrate for mm-wave AlN HEMT PAs. Figure 1d shows the energy band diagram of the as-grown heterostructure, calculated using a self-consistent 1D Schrodinger–Poisson solver.[28] A 2DEG channel is induced at the top GaN/AlN interface[29] without the need of impurity doping due to the positive polarization difference. The 2DEG density in the as-grown heterostructure electrostatically depends on the thicknesses of the GaN channel layer and AlN barrier layer.[30] In general, beyond the critical GaN channel thickness of $\approx 3$ nm, thicker GaN or AlN layers result in higher 2DEG densities. The high polarization difference between AlN and GaN results in 2DEG densities of $2-3\times10^{13}\,\text{cm}^{-2}$ in an as-grown 4 nm AlN/200 nm GaN/500 nm AlN heterostructure with room-temperature mobilities of $\approx 720\,\text{cm}^2\,\text{Vs}^{-1}$. When processed into scaled RF HEMTs,[21] the high 2DEG density translates to low access resistances and high on-currents of $>3\,\text{A mm}^{-1}$, high extrinsic transconductance of $0.8\,\text{S mm}^{-1}$, and high speeds with $f_T/f_{MAX}$ of 123/233 GHz.

Making the AlN top barrier layer thicker, >30 nm in the AlN/GaN/AlN structure, should move the surface states away from the 2DEG channel. The thicker AlN barrier layer is also expected to increase the as-grown 2DEG density compared with a 4 nm AlN barrier layer. This should further reduce the access resistance in the final HEMTs, an additional advantage of the proposed in situ AlN passivation layer. However, incorporating this proposed AlN passivation scheme into the AlN HEMT process poses the following challenges. From the epitaxial growth perspective, a 2.4% lattice mismatch between GaN and AlN crystals makes it challenging to grow thick AlN layers on relaxed GaN without cracking. Careful control of the layer strains is necessary to prevent cracking. From the transistor perspective, the gate needs to be close to the 2DEG to maintain electrostatic control over the channel. Therefore, this passivation technique makes it necessary to incorporate a recess-gate geometry. The optimum design of the in situ crystalline AlN-passivated AlN/GaN/AlN HEMT is shown in Figure 1c.

The following sections tackle the challenges listed earlier. First, the growth of thick AlN barrier layers is demonstrated by ensuring almost pseudomorphically strained GaN channel layers. Next, the resultant 2DEG transport is characterized and a well-controlled recess etch process is demonstrated which preserves the 2DEG. Finally, the results of the fabricated in situ-passivated AlN/GaN/AlN HEMTs are presented, that demonstrate the successful reduction of the DC-RF dispersion.

### 2.1. GaN Channel Strain in AlN/GaN/AlN Heterostructures

The in-plane lattice constant of a relaxed wurtzite AlN crystal $a_0^{\text{AlN}} = 3.112$ Å is smaller than that of GaN $a_0^{\text{GaN}} = 3.189$ Å. The resulting ≈2.4% in-plane lattice mismatch makes the epitaxial growth of thick AlN barrier layers on relaxed GaN challenging. Consider the case of AlN/GaN HEMT heterostructures, where the AlN barrier layer is under tensile strain on "relaxed" GaN buffer layers. There exists a critical coherent thickness $t_{cr}$ below which the AlN layer remains strained to GaN. Using Blanc's estimate[31] of $t_{cr} \approx \mathbf{b}_e/2f$, where $\mathbf{b}_e = 0.3189$ nm is the Burgers' vector length in strained AlN and $f = 0.024$ is the lattice mismatch between AlN and relaxed GaN, results in a critical thickness of ≈6.5 nm. Beyond this thickness, the tensile-strained AlN layer relaxes and releases the strain energy in the form of cracks along hexagonal planes. This has been observed experimentally in AlN/GaN HEMT structures,[32] where structures with AlN barriers >7 nm showed hexagonal cracks on the surface in atomic force microscopy (AFM) scans. These cracks lead to a suppression of the 2DEG mobility and are undesired in a device heterostructure.

Now consider the AlN/GaN/AlN HEMT structure which is grown on relaxed AlN buffer layers. If the GaN channel layer is "compressively strained" to the AlN buffer layer (i.e., the GaN lattice constant is closer to that of AlN compared with its relaxed state), a smaller lattice mismatch $f$ between the top AlN barrier layer and the GaN channel is obtained. $f$ decreases with increase in in-plane compressive strain $\epsilon_{xx}^{\text{GaN}}$ in the GaN layer. Consequently, the coherent critical thickness $t_{cr}$ of the AlN barrier layer is expected to increase with $\epsilon_{xx}^{\text{GaN}}$ through the relation $t_{cr}(\epsilon_{xx}^{\text{GaN}}) \approx b_e/2f(\epsilon_{xx}^{\text{GaN}})$, where $t_{cr}$ and $f$ are functions of $\epsilon_{xx}^{\text{GaN}}$.

The calculated critical thickness of the top AlN barrier layer in an AlN/GaN/AlN HEMT structure is shown in **Figure 2**a. When the GaN channel is completely relaxed, the critical thickness of AlN is $t_{cr}(\epsilon_{xx}^{\text{GaN}} = 0) \approx 6.5$ nm. This is similar to the AlN/GaN HEMT structure.[32] The cartoon in Figure 2e shows the situation when AlN layer thicker than $t_{cr}(\epsilon_{xx}^{\text{GaN}} = 0)$ is grown on a relaxed GaN channel layer. The AlN barrier layer relaxes to relieve the strain and forms cracks. On the other extreme, in AlN/GaN/AlN HEMT, the whole structure can also be pseudomorphic to the AlN buffer, which means $\epsilon_{xx}^{\text{GaN}} = -2.4\%$. Under such conditions, the AlN barrier layer is no longer under any tensile strain, and the critical thickness of the relaxed layer thus approaches infinity. The cartoon in Figure 2c shows this desired condition. Growth conditions can lead the crystal to be in a state between the above two extremes, where the GaN layer starts to partially relax and the top AlN layer builds up some tensile strain. Therefore, the strain in the GaN layer $\epsilon_{xx}^{\text{GaN}}$ is the critical parameter for enabling the growth of thick AlN layers for our proposed in situ passivation scheme. From Figure 2a, it is clear that a compressive strain of >2% in the GaN layer is desired to grow crack-free in situ AlN passivation layers thicker than 30 nm.

The compressive strain in the GaN layer, $\epsilon_{xx}^{\text{GaN}}$, in turn depends on its thickness $t_{\text{GaN}}$. The exact relation between the strain and thickness of an epitaxial layer depends on the growth technique, growth modes, growth temperature, starting substrate, etc. Hence, to experimentally determine the relationship between $t_{\text{GaN}}$ and $\epsilon_{xx}^{\text{GaN}}$ in our heterostructures, a series of 100 nm AlN barrier/GaN/500 nm AlN heterostructures were grown using plasma-assisted molecular beam epitaxy (PA-MBE) on 6H-SiC substrates. Only the GaN layer thickness $t_{\text{GaN}}$ was varied between these samples. Details of the epitaxial growths are provided in the Experimental Section.

Reciprocal space mapping (RSM) using X-ray diffraction was conducted on these AlN/GaN/AlN heterostructures around the SiC (1112)/GaN (114) peaks to extract the in-plane lattice spacings of the GaN layer. Reciprocal space maps for AlN/GaN/AlN samples with $t_{\text{GaN}} = 15$, 30, 200 nm are shown in **Figure 3**. The samples, labeled A, B, and C, respectively, are shown in **Table 1**.

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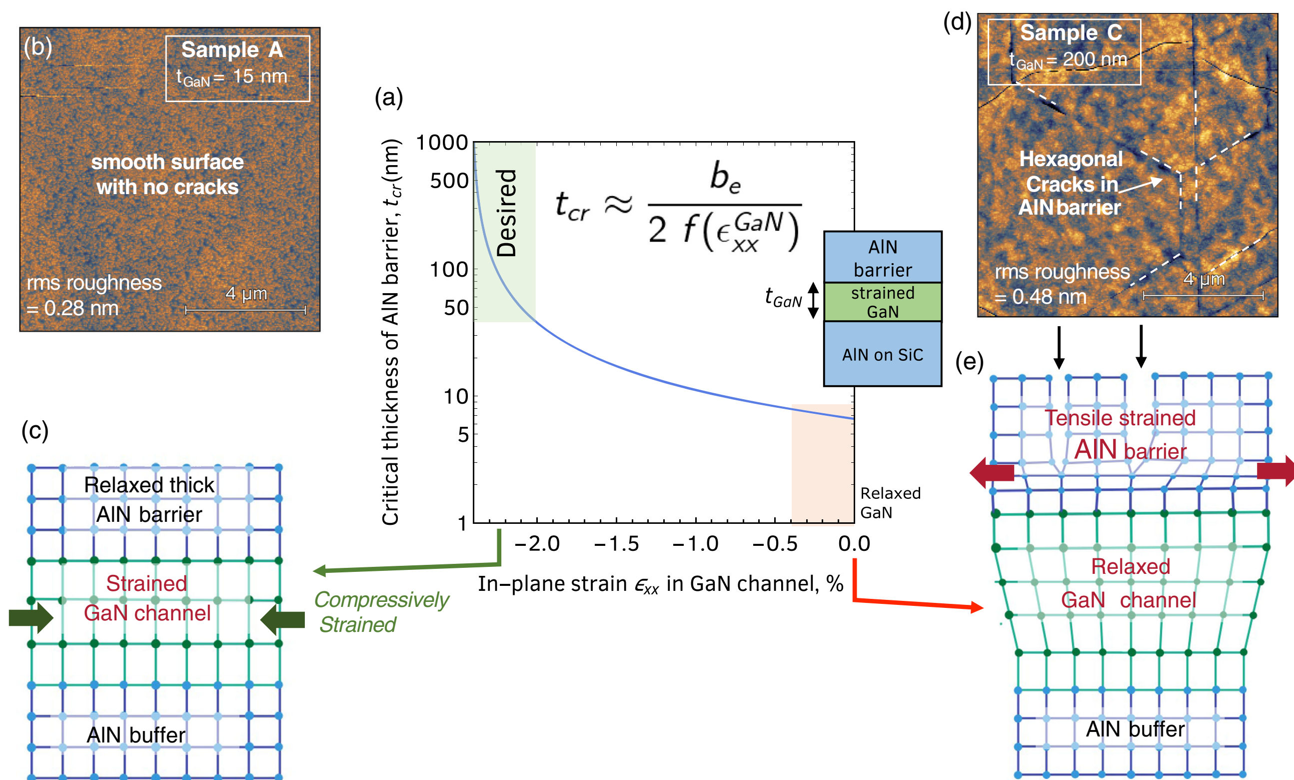


**Figure 2.** a) The calculated dependence of the critical coherent thickness of the AlN passivation/barrier layer on the compressive strain of GaN layer in the AlN/GaN/AlN structure. A higher GaN compressive strain results in larger AlN critical thickness. A GaN channel layer almost pseudomorphic to AlN with >2% compressive strain is desired to grow thick >30 nm AlN barrier layers which will act as in situ passivation. b,d) The AFM scans of the surface of AlN/GaN/AlN samples A and C with 15 nm and 200 nm of GaN channel layers, respectively. Hexagonal cracks are observed on the surface of sample C, which form to relieve the tensile strain in the AlN barrier, as shown in e). Sample A, however, shows smooth surface with no cracks as the whole structure is pseudomorphic to AlN, as shown in c).

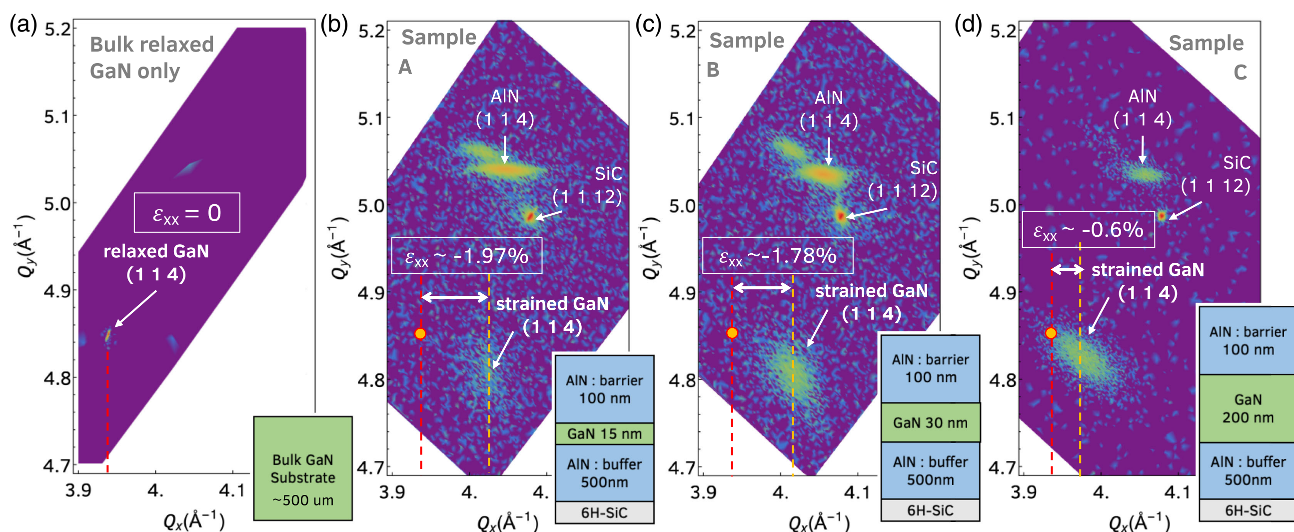


**Figure 3.** a) X-ray diffraction reciprocal space map of a control bulk GaN substrate showing the (114) reciprocal reference space point of a relaxed GaN layer. b,c,d) The RSM for a series of AlN/GaN/AlN samples with GaN layer thicknesses of 15 nm, 30 nm, 200 nm. The in-plane compressive strain in the GaN layers, extracted with respect to the relaxed GaN (114) point, decreases with increase in the GaN layer thickness.


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**Table 1.** Summary of the AlN/GaN/AlN heterostructure studied in this work with their corresponding structural and 2DEG transport properties. The strain in GaN channel layers $\epsilon_{xx}^{GaN}$ was extracted from the X-ray diffraction reciprocal space maps shown in Figure 3 and 4. Hall effect measurements were used to determine the 2DEG density $n_s$, room-temperature mobility $\mu_n$, and the sheet resistance $R_{sheet}$. The high sheet resistance in sample C, due to crystal cracking, makes is difficult to reliably determine the 2DEG mobility and charge densities.

| Sample ID | Heterostructure $t_{AlN}/t_{GaN}/t_{AlN}$ | $\epsilon_{xx}^{GaN}$ | Surface morphology | 300 K $n_s$ [$\times 10^{13}$ cm$^{-2}$] | 300 K $\mu_n$ [cm$^2$ Vs$^{-1}$] | 300 K $R_{sheet}$ [Ω sq$^{-1}$] |
|---|---|---|---|---|---|---|
| A | 100/15/500 | −1.97% | Smooth with no cracks | 4.24 | 297 | 495.2 |
| B | 100/30/500 | −1.78% | No cracks in as-grown structure but optically visible cracks during device processing | 4.86 | 316 | 406 |
| C | 100/200/500 | −0.6% | Cracks in as-grown structure, visible in AFM | – | – | $2.51 \times 10^5$ |
| D | 50/15/500 quarter 4" wafer | −1.97% | Smooth, no cracks | 3.57 | 358 | 428 |

RSM scan was also conducted on single-crystal bulk GaN substrate for calibration. The extracted in-plane spacing of $a_0^{GaN} = 3.189$ Å from the bulk GaN sample agrees with the relaxed GaN lattice constant value. From the RSMs from the AlN/GaN/AlN structures, it is clear that the in-plane lattice constants of the GaN layers are smaller than $a_0^{GaN}$, confirming the compressive strain. Using $a_0^{GaN}$ as the reference, the strains in the GaN layers $\epsilon_{xx}^{GaN}$ of different thicknesses are extracted from their in-plane lattice spacings. The extracted strains $\epsilon_{xx}^{GaN}$ are shown in Table 1 and in **Figure 4** as a function of $t_{GaN}$. Data from other AlN/GaN/AlN samples with $t_{GaN} = 9$ and 22 nm are also included. It clearly seen that a thinner GaN layer is more compressively strained to AlN as expected. Comparing the data in Figure 2 and 4, we infer that a GaN channel layer thinner than 15 nm is required in an AlN/GaN/AlN structure to maintain a >2% compressive strain and thereby grow the desired in situ crack-free AlN passivation layer of >30 nm. The finite lattice constant difference between the strained GaN channel and fully relaxed AlN is a result of a slight elastic relaxation, which is not expected to generate extra dislocations between the two.

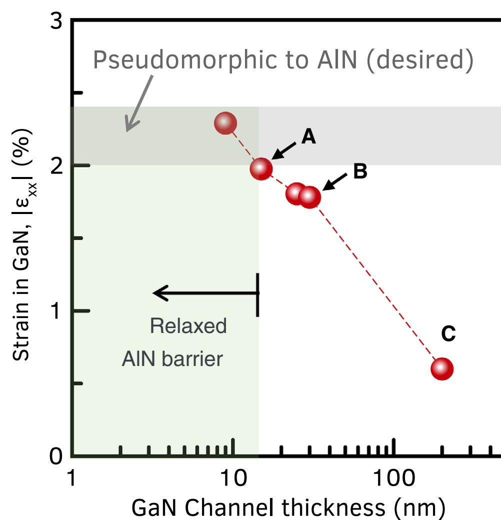


**Figure 4.** Experimental dependence of the in-plane compressive strain in the GaN layer as a function of its thickness in an MBE-grown AlN/GaN/AlN heterostructure grown on 6 H SiC. The strains are extracted from X-ray diffraction reciprocal space maps shown in Figure 3. The results show that GaN channel thickness of <15 nm results in the >2% compressive strain desired for growing >30 nm-thick AlN passivation layers. The finite lattice constant difference between the strained GaN channel and fully relaxed AlN is a result of a slight elastic relaxation, which is not expected to generate extra dislocations.

The differences in the strains in AlN/GaN/AlN samples with different $t_{GaN}$ are also directly evident from the corresponding surface morphology. Figure 2b,d shows the 10 × 10 μm AFM scans of the surface of AlN/GaN/AlN samples A and C. Both these samples have a 100 nm AlN barrier grown on top of the GaN layer. Sample A, with ≈2% compressively strained 15 nm GaN channel layer, shows a very smooth surface with sub-nanometer root-mean-square roughness of 0.28 nm. In contrast, sample C, with an almost relaxed ($\epsilon_{xx}^{GaN} \approx 0.5\%$) 200 nm GaN channel layer, exhibits clear hexagonal cracks on the as-grown AlN surface. These are similar to those seen in AlN/GaN HEMT structures[32] and signify that the top AlN layer relieved its high tensile strain by cracking. These cracks lead to the sample being highly resistive, with 3-orders-higher sheet resistance compared with sample A and B. It is also worth pointing out that even though sample B, with 30 nm GaN channel, did not show cracks on the as-grown surface, hexagonal cracks developed during the device fabrication process, which were visible under an optical microscope. This further provides the experimental evidence that a thin, <15 nm GaN channel layer is needed in the AlN/GaN/AlN structure to grow a thick in situ passivation AlN layer with desired structural properties.

### 2.2. 2DEG Transport in In Situ-Passivated AlN/GaN/AlN Heterostructures

In addition to the structural properties, optimal 2DEG transport is necessary for the HEMT. The as-grown 2DEG sheet resistance determines the access resistances in the recessed-gate AlN HEMT shown in Figure 1c. A low sheet resistance is thus desired. It is found that, for a given AlN passivation layer thickness, a thinner GaN layer results in higher sheet resistance due to both lower charge density and lower mobilities.

In AlN/GaN/AlN structure, the 2DEG density $n_s$ depends electrostatically both on the AlN barrier layer and on the GaN channel layer. Specifically, for a given AlN barrier layer thickness in an AlN/GaN/AlN heterostructure, a thinner GaN layer results in a lower 2DEG density.[18] The measured room-temperature 2DEG densities for samples A, B, and C in this study are shown


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in Table 1. Sample C was found to be too resistive with sheet resistance of $>10^5\,\Omega\,\text{sq.}^{-1}$, and therefore the 2DEG density mobility could not be reliably determined through Hall measurements. This due to the cracks in the AlN barrier layer, further emphasizing the need for strained GaN layers. The lower 2DEG density in sample A, with 15 nm GaN channel layer, compared with sample B, with 30 nm GaN channel layer, confirms the expected trend of lower $n_s$ in thinner GaN channels for the same AlN thicknesses.

Simultaneously, a thinner GaN channel layer in the AlN/GaN/AlN structure has been found to result in a lower 2DEG room-temperature mobility $\mu_n$. This experimental trend is supported independently both by data from controlled studies in our group and by literature reports[11–14,17] of AlN/GaN/AlN heterostructure growths. Interestingly, this trend is independent of the epitaxial growth method (e.g., metal organic chemical vapor deposition vs. MBE) and the starting substrates (Si, SiC, sapphire, bulk AlN). The probable causes are the dislocation densities, proximity to the bottom interface, higher confinement field in the well, etc. The exact reason however is not clear at this moment and is being actively investigated in the community.

Thus, for thinner GaN channel layers, a combination of lower 2DEG densities $n_s$ with the lower mobilities $\mu_n$ results in higher 2DEG sheet resistance through $R_{\text{sheet}} = 1/q_e\mu_n n_s$. Hence, even though the thinnest possible GaN channel layer is desired structurally, the thicker the channel, the better 2DEG transport. As a trade-off, a 15 nm GaN channel layer thickness is chosen for fabricating and testing in situ-passivated HEMTs. According to the experimental evidence, this is the thickest GaN channel that allows growth of the thick AlN passivation layer ($\epsilon_{xx}^{\text{GaN}} \approx 2\%$), while maintaining a "transistor-worthy" 2DEG sheet resistance for the device.

With the optimum heterostructure now determined, a quarter-of-4 in wafer of the in situ-passivated AlN/GaN/AlN HEMT structure was grown for fabricating devices. The sample, labeled D, had a 50 nm AlN passivation layer/15 nm GaN channel layer/500 nm AlN buffer layer on a 6H-SiC substrate. **Figure 5**a shows the sheet resistance map of the as-grown wafer. The wafer shows the presence of the 2DEG across the whole wafer surface and good uniformity with a sheet resistance of $\approx 450\,\Omega\,\text{sq.}^{-1}$ at room temperature.

To test the effect of the passivation layer on the transport of the 2DEG, temperature-dependent Hall effect measurements were carried out on the AlN/GaN/AlN HEMT structure with and without the thick AlN passivation layer. A $10 \times 10$ mm piece diced from the quarter wafer D and a 4 nm AlN/30 nm GaN/500 nm AlN heterostructure sample were measured from 300 K down to 10 K. The 4 nm "thin-barrier" heterostructure is representative of the structure used in the current state-of-art RF AlN HEMTs[10] without in situ passivation. The results of the temperature-dependent Hall measurements are shown in Figure 5b,c,d.

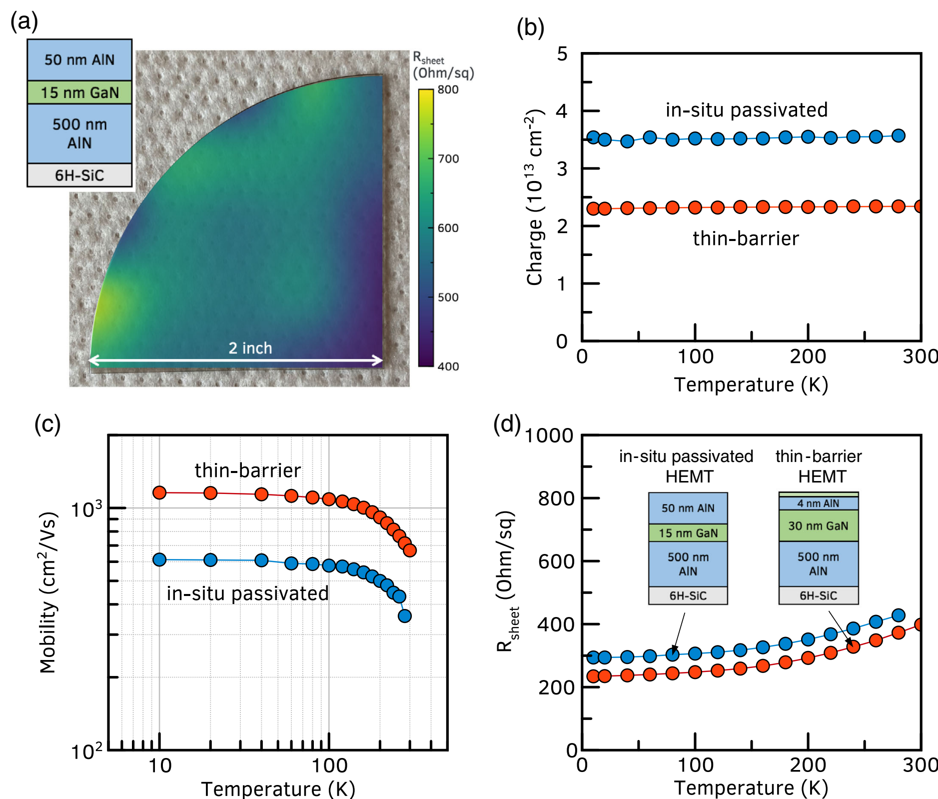


**Figure 5.** a) Sheet resistance map of an in situ-passivated 50 nm AlN/15 nm GaN/500 nm AlN heterostructure, sample D, grown on a-quarter-of-4 in. SiC wafer. The 2DEG is present across the whole wafer. b,c,d) The results of temperature-dependent Hall effect measurements comparison between an in situ-passivated and a thin-barrier AlN/GaN/AlN structure. The in situ-passivated sample shows higher charge and lower mobility compared with the thin-barrier structure. However both show almost similar sheet resistance, confirming the suitability for transistor fabrication.

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From the charge densities plot in Figure 5b, the in situ-passivated structure shows a higher 2DEG density of $3.5 \times 10^{13}$ cm$^{-2}$ compared with $2.2 \times 10^{13}$ cm$^{-2}$ for the thin-barrier structure, both of which agree to simulated densities. They do not freeze out on cooling, as expected from polarization-induced 2DEGs. Figure 5c shows the temperature dependence of 2DEG mobilities. The mobilities for the thin-barrier structure are $\approx$650 and 1100 cm$^2$ V$^{-1}$s$^{-1}$ at 300 and 10 K. These values are comparable with mobilities reported previously[12–14,17,18] in these AlN/GaN/AlN heterostructures. In contrast, the 2DEG mobilities in the in situ-passivated AlN/GaN/AlN heterostructure are $\approx$350 and 600 cm$^2$ V$^{-1}$s$^{-1}$ at 300 and 10 K. It is $\approx 2\times$ lower than the thin barrier sample throughout the measured temperature range, albeit at a $\approx 1.5\times$ higher charge density. This trend of lower 300 K mobility at higher densities is expected as optical phonon scattering, which is the dominant electron scattering mechanism at room temperature in III-nitride semiconductors, increases with 2DEG density.[33] However the exact cause of the lower mobility is under investigation, especially at low temperatures. The trade-off between charge density and mobility results in a comparable sheet resistance of $\approx$400 and $\approx$250 at 300 and 10 K in both the structures, as shown in Figure 5d. Therefore, moving from a thin barrier to in situ AlN-passivated structure is not expected to drastically affect the access resistances of the AlN/GaN/AlN HEMTs.

A thick 50 nm AlN passivation layer in the as-grown sample D heterostructure necessitates a recess etch in the HEMT channel region, that is, the region right under the gate in Figure 1c. This is to ensure that the gate metal is placed close to the 2DEG channel to maintain high gate-channel capacitance and transconductance. In the thin-barrier devices without in situ passivation, the gate metal is deposited directly on the as-grown heterostructure surface. Hence it is also important to characterize the post-etch 2DEG transport as this will determine the HEMT channel performance.

To do so, in situ-passivated sample B (100 nm AlN/30 nm GaN/500 nm AlN) and a diced $10 \times 10$ mm piece from wafer D (50 nm AlN/15 nm GaN/500 nm AlN) were chosen for a blanket etch test. The top AlN layer in these AlN/GaN/AlN samples was etched away in short $\approx$5 nm steps using low-power $BCl_3$-based inductive-coupled plasma (ICP) dry etches. This simulates the etch which the 2DEG in the channel region sees during the recess etch process in the final HEMT fabrication. Hall effect measurements were carried out after each successive etch to characterize the 2DEG. **Figure 6** shows the measured 2DEG density, mobilities, and sheet resistance as a function of the remaining top AlN barrier layer thickness in the two samples. From Figure 6a, the measured 2DEG densities in both samples B and D agree with the densities expected from a self-consistent 1D Schrodinger–Poisson simulation of their respective layer structures. The 2DEG density slowly decreases as the AlN barrier becomes thinner, completely disappearing at a critical thickness of $\approx$3 nm. Correspondingly, the 2DEG mobilities, both at 300 and at 77 K, maintain their as-grown value till AlN thickness of $\approx$20 nm and then start to decrease, as shown in Figure 6b,c. As the AlN layer gets thinner, the sheet resistance, shown in Figure 6d,e, exhibits orders of magnitude jump from $\approx 400\ \Omega$ sq$^{-1}$ in the as-grown structures to $\approx 1$ M$\Omega$ sq$^{-1}$ at a thickness of <3 nm. A good electrostatic control over the 2DEG densities is thus demonstrated with the etch process, with important information of the 2DEG resistance as a function of recess depth thickness. This information is very valuable for AlN HEMT device design and modeling. They provide the option to design both enhancement (E)-mode and depletion (D)-mode AlN HEMTs depending on the gate recess depth. Furthermore, these results demonstrate that the low-power recess etch process is ready to be incorporated into the transistor fabrication process.

### 2.3. Reduced Dispersion in AlN/GaN/AlN HEMTs

To test the in situ crystalline AlN passivation scheme, scaled recessed-gate RF HEMTs were fabricated on $10 \times 10$ mm diced pieces of the quarter wafer D. The details of the fabrication process are presented in the Experimental Section. A relatively shallow recess etch was used in these demonstrated HEMTs. The resultant gate-to-channel distance is $\approx$15 nm. Also, instead of a T-gate, the gate head was placed directly on the AlN surface. The device geometry and dimensions are shown in the inset of **Figure 7**.

The DC characteristics of the fabricated HEMTs devices are shown in Figure 7a,b. A maximum on-current of $\approx$1 A mm$^{-1}$ and high $I_{on}/I_{off}$ ratio of $\approx$7 orders are measured in the device with a gate length $L_G = 230$ nm. The impressive 7 order $I_{on}/I_{off}$ ratio is higher than the 2–4 orders, typically observed in ex situ SiN-passivated AlN HEMTs.[21] The peak $g_m$ is $\approx$0.2 S mm$^{-1}$, which is understandably lower than $\approx$0.8 S mm$^{-1}$ measured in ex situ-passivated AlN HEMTs[21], due to a larger gate channel distance and a lower 2DEG mobility in the 15 nm channel. This translates to relatively low cutoff frequencies of $f_T/f_{MAX} = 51/75$ GHz for a device with $L_G = 180$ nm. However, these results confirm that the new self-aligned recessed-gate HEMT process works and is suitable for device fabrication.

To characterize the DC-RF dispersion in the devices, pulsed $I_D$–$V_D$ measurements were carried out using 500 ns pulse width and 0.05% duty cycle. The results from two in situ-passivated AlN HEMTs with gate lengths $L_G = 230$ and 70 nm are shown in Figure 7c,d. The HEMTs show an on-current dispersion of $\approx$2% and $\approx$6% and knee voltage walkout of <0.2 V at quiescent gate/drain biases of −4/8 V. These are drastically lower than 20% measured in the state-of-art ex situ SiN-passivated AlN HEMTs[21], shown in Figure 1a, albeit at a slightly different bias and current level. However, the low-dispersion results across multiple devices serve as an experimental confirmation that the in situ crystalline AlN passivation technique is indeed effective in reducing the RF dispersion in these AlN/GaN/AlN HEMTs. Interestingly, both the devices show signs of "negative" dispersion, with the DC $I_D$ lower than the pulsed $I_D$ under quiescent gate/drain bias of −4/8 V. This is beneficial for large-signal performance of a HEMT and the reason for this behavior is currently under investigation. Future devices with scaled T-gates and deeper recess etches, shown in Figure 1c, should show better small signal characteristics and translate the advantage of the lower DC-RF dispersion to the large signal performance.


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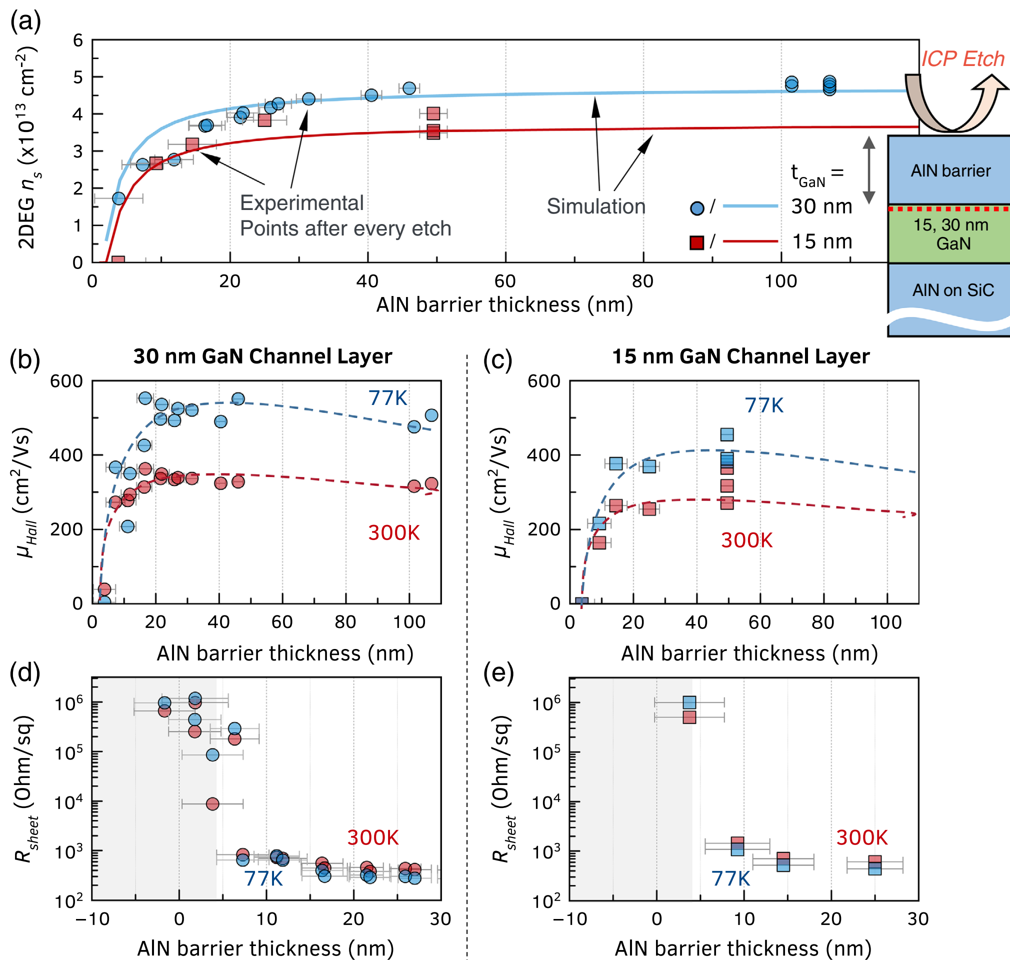


**Figure 6.** 2DEG transport in in situ-passivated AlN/GaN/AlN samples B and D as a function of remaining AlN barrier/passivation layer thickness to characterize the effect of the gate recess etch on the channel. Hall effect measurements are carried out after each step to remove the top passivation layer in short steps using low-power ICP dry blanket etches. a) A good agreement to the measured and expected 2DEG charge density as a function of AlN thickness is observed, confirming good charge control of the channel. b,c) The 2DEG mobility as a function of barrier thickness, which remains constant at large thicknesses but drops below the remaining AlN barrier thickness of ≈ 10 nm. d,e) The sheet resistance remains ≈400 Ω $sq^{-1}$ as the remaining AlN barrier thickness decreases to ≈ 3 nm, after which the sample becomes resistive.

## 3. Conclusion

In summary, this work presents in situ crystalline AlN as a potential passivation technique for III-nitride RF HEMTs. The efficacy of this passivation scheme is demonstrated on AlN/GaN/AlN RF HEMTs. Through a theoretical model and a series of epitaxial growths, it is found that a <15 nm GaN channel layer is necessary for growing 30+ nm-thick AlN passivation layers in these heterostructures. Large-area growths of the optimized in situ-passivated AlN/GaN/AlN HEMT structures are conducted on quarter-of-4 in. SiC wafer. A sheet resistance of ≈450 Ω $sq^{-1}$ and 2DEG density of $3.5 \times 10^{13}$ $cm^{-2}$ are measured across the wafer at room temperature, which is suitable for HEMT fabrication. The 2DEG is also shown to survive the low-power ICP etch for forming the recess gates. Pulsed $I_D$–$V_D$ measurements on the fabricated scaled recess-gate RF HEMTs show a much reduced RF dispersion down to $\approx 2-6\%$, which is almost an order of magnitude lower compared with the dispersion in previously reported ex situ SiN-passivated AlN/GaN/AlN HEMTs.

As the RF dispersion from the surface states limits the RF power outputs of the current state-of-art AlN/GaN/AlN HEMTs, it is expected that the new passivation scheme and the recess-gate HEMT fabrication process developed as part of this work should push the output powers even higher. The next generation of in situ-passivated AlN HEMTs with aggressive scaled T-gates should be able soon confirm this. These devices will further benefit from improvement of 2DEG mobility in the channel region and incorporation of an etch-stop layer in the thick AlN barrier layer. Suppression of surface dispersion using the in situ AlN passivation technique will also allow investigations into other potential mechanisms limiting the output powers of the AlN HEMTs such as dispersion from AlN point defects and bulk traps.

To the authors' best knowledge, this work is the first demonstration of in situ passivation of HEMTs using thick "crystalline"


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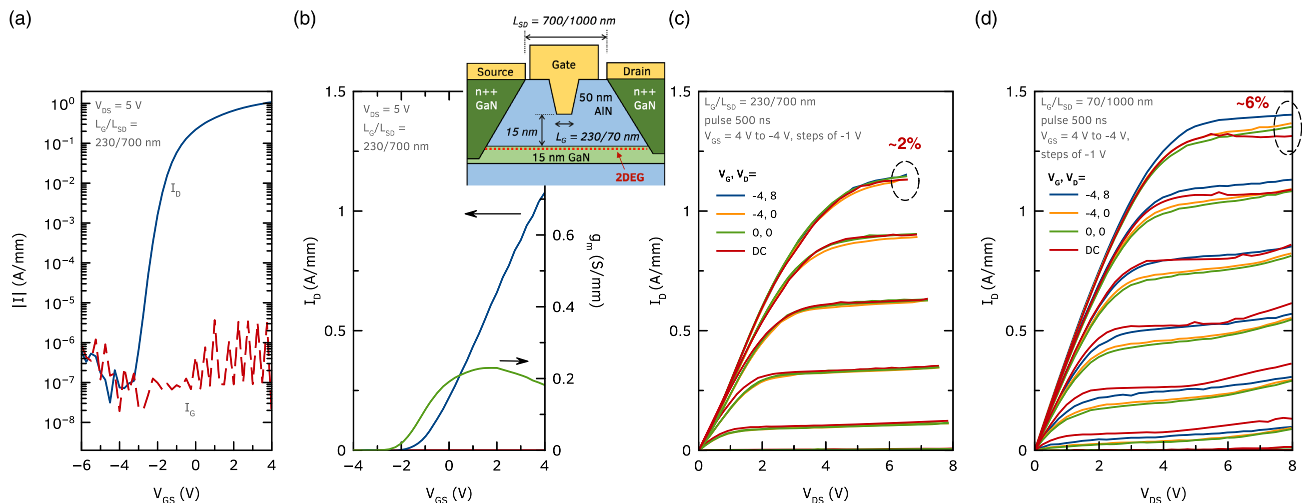

**Figure 7.** a,b) DC characteristics of a scaled, in situ-passivated AlN/GaN/AlN HEMT with a recessed gate length $L_G = 230$ nm and gate channel distance of 15 nm. The device shows good transfer characteristics with on/off ratio of 7 orders and a maximum on-current >1 A mm$^{-1}$. c,d) Pulsed $I_D$–$V_D$ measurement results from two representative in situ-passivated AlN/GaN/AlN HEMTs with different gate dimensions. The low DC-RF dispersion of ≈ 2% and ≈ 6% across multiple devices confirms the efficacy of this in situ crystalline AlN passivation scheme compared with the ex situ PECVD SiN (shown in Figure 1a) for AlN/GaN/AlN HEMTs.

AlN layers, which also act as barrier layers for the 2DEG. Previously, in situ "amorphous" AlN has been used to demonstrate passivation of MBE-grown GaN HEMTs.[34] However, these layers require a low-temperature MBE growth condition at >200 °C below the growth temperature of the rest of the heterostructure. The crystalline AlN passivation layer in this work is grown as part of the HEMT structure growth and does not need separate growth calibrations. Even though the metal-polar AlN/GaN/AlN HEMT is used as a demonstration in this work, this passivation technique is not limited to this structure and can be applied to other III-nitride heterostructures as well by appropriately controlling the strains in the layers. As the findings of this work are not affected by polarity, this passivation technique should also be beneficial to heterostructures grown on N-polar AlN such as N-polar GaN/AlN HEMTs.

## 4. Experimental Section

*Epitaxial Growth of AlN/GaN/AlN Heterostructures*: The heterostructures studied in this work were grown using a Veeco Gen10 PAMBE system on insulating 6 H-silicon carbide (SiC) substrates. The substrates were ultrasonicated in acetone, methanol, and isopropanol for 15 mins each before loading into the MBE system. The smaller 10 × 10 mm pieces were mounted on 3 in.-lapped silicon wafers using liquid indium metal. The quarter-of-4 in. wafer was mounted using a specially fabricated molybdenum substrate holder. The substrates were outgassed at 200 and 500 °C for 7 and 2 h, respectively, before introducing into the MBE growth chamber. Standard gallium (Ga) and aluminum (Al) effusion cells were used to provide the metal fluxes, and nitrogen (N) active species were supplied using a Veeco RF plasma source. N plasma power of 400 W corresponding to a growth rate of 0.42 μm h$^{-1}$ was used. The whole heterostructure was grown at a substrate temperature of ≈750 − 770 °C. The AlN on SiC nucleation layer of ≈50 nm was grown in a slight N-rich condition with Al:N flux ratio of ≈0.9. The rest of the ≈450 nm AlN buffer layer was grown in metal-rich conditions with Al:N flux ratio of ≈1.1. After the AlN buffer layer growth, the GaN channel layer and AlN barrier/passivation layer of the desired thicknesses were grown by controlling the Al and Ga shutters. The growth was monitored using in situ reflection high-energy electron diffraction (RHEED) to ensure optimum growth conditions.

*AlN HEMT Fabrication*: The in situ-passivated AlN/GaN/AlN HEMT process started with the MBE-regrown ohmic contacts. The as-grown heterostructure was patterned using a $SiO_2$/chromium mask and dry etched using ICP etch to expose the 2DEG sidewall. The sample was then reintroduced into the MBE chamber where n++GaN with [Si] ≈1 × 10$^{20}$ cm$^{-2}$ was grown to form the ohmic contacts. Devices were isolated using ion implantation, followed by deposition of Ti/Au ohmic metal. Two-step lithography was used to form the recessed T-gates. A $SiO_2$/chromium/ZEP520 mask was deposited and patterned using electron beam lithography (EBL) to define the gate stem length. The AlN passivation/barrier layer was etched to the desired depth using the low-power ICP etch. A second PMGI SF9/ZEP520a mask was deposited and patterned using EBL, which defined the gate head dimensions. Ni/Au metal was then deposited via e-beam evaporation, followed by lift-off to form the T-gates.

## Acknowledgements

This work was supported by Semiconductor Research Corporation (SRC) Joint University Microelectronics Program (JUMP), AFOSR (grant FA9550-20-1-0148), and by the National Science Foundation (NSF) (grants 1710298, 1534303, Platform for the Accelerated Realization, Analysis, and Discovery of Interface Materials (PARADIM) under Cooperative Agreement no. DMR-2039380. Characterizations and measurements were carried out in part at Cornell Nanoscale Facilities, supported by NSF grant NNCI-2025233, and in part at Cornell Center for Materials Research Shared Facilities, supported through the NSF MRSEC program (DMR-1719875) and NSF MRI (DMR-1429155 and DMR-1338010) programs.

## Conflict of Interest

The authors declare no conflict of interest.

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## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

epitaxy and semiconductor processing, high-electron-mobility transistors, high-frequency devices

Received: July 9, 2021
Revised: September 15, 2021
Published online: October 14, 2021

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