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Multi-level Analog Programmable Graphene Resistive Memory with Fractional Channel Ferroelectric Switching in Hafnium Zirconium Oxide

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***Abstract*—This paper reports multi-level programming of ferroelectrically modulated resistive memory in two-dimensional atomically thin graphene. The ferroelectric film utilized is hafnium zirconium oxide (HZO). The device uses a graded potential across the graphene resistor for fractional ferroelectric switching of the underlying HZO, which in turn produces an analog modulation of graphene resistance. A multi-level modulation of 13.3% was achieved in a graphene resistor of 22 kΩ nominal resistance, with programming voltages from 0 to 8.5 volts to achieve symmetric and asymmetric programming of up to 31 distinct resistive levels of memory. This device has potential of storing analog values for neuromorphic computing. The device architecture constitutes a thickness of ~20nm, which allows for high spatial density integration and aggressive voltage scaling.**

Keywords—neuromorphic computing; fractional ferroelectric switching; analog memory; graphene; hafnium zirconium oxide.

I. INTRODUCTION

Neuromorphic computing has gained significant attention due to its potential for ultra-low power, high efficiency, and parallel Multiply-Add-Compute (MAC) processing required for implementing deep neural networks (DNN) [1]–[3]. Perceptron blocks, an array of MAC units, are the building blocks for neuromorphic computing. Resistive synaptic weights require analog levels of conductance modulation, which are key to large scale DNN implementation when high densities of the weights are needed [4]. For example, ferroelectric field-effect transistor (FE-FET)-based analog synaptic devices with silicon and germanium channels have been previously demonstrated, which use partial polarization switching in the gate hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$ abbreviated as HZO) to realize multi-level resistance modulation [5], [6]. The switching is achieved with identical gate voltage pulses of 50-100 ns and 3-5 MV/cm fields.

Multi-level resistive random access memory (RRAM) is a promising approach for non-volatile memory (NVM) due to its high speed and energy efficiency [7]. Silver-silicon memristors and hafnium oxide resistive switches have previously demonstrated synaptic operation for RRAM, with extensive additional circuitry and multiple identical voltage pulses for resistor programming [8]–[10]. Resistive memory based on 2-D materials is highly desirable due to the ability to modulate resistance across grain-boundaries, with the potential to individually switch ferroelectric domains in HZO of length 20-40 nm [11]. This paper reports on a graphene-on-HZO resistance readout memory device using fractional channel switching of the ferroelectric HZO for analog resistance modulation in the graphene.

II. DEVICE ARCHITECTURE

Figure 1 shows the schematic of the fractional programming device. The film structure is chosen to enable high density, compatible with CMOS integration. Ferroelectric HZO is intrinsically limited to <20 nm, with alumina capping of 2-3nm. Graphene has atomic thickness. Hence, thickness < 10 nm are possible. Voltages V_1 and V_2 are applied across the graphene resistor, while the bottom electrode at V_3 is grounded. The coercive voltage is $V_C = \frac{E_C}{t}$, for a HZO film of thickness t and coercive field E_C. If all dipoles in HZO are switched upwards before programming, 3 cases are possible: (1) For $V_1, V_2 < V_C$, no point along the graphene resistor exceeds V_C, and the ferroelectric domains are unaffected. (2) For $V_1 > V_C, V_2 < V_C$, a fraction of the total resistor length L (denoted by L') exceeds V_C, and the domains in this region are switched down. (3) For $V_1, V_2 > V_C$, all the domains are switched down. Negative voltages can be similarly used for fractional or complete up-switching of HZO domains.

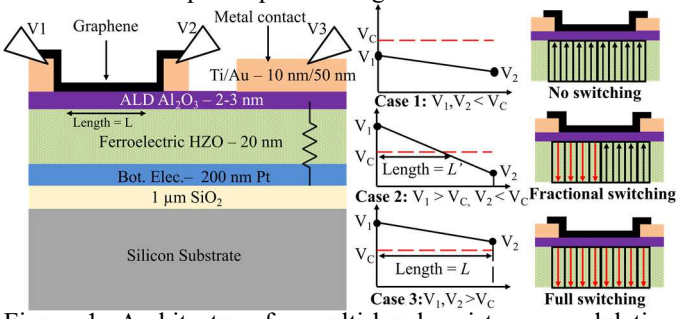

Figure 1: Architecture for multi-level resistance modulation: 2-dimensional graphene on ferroelectric HZO as a resistive layer to achieve a graded potential along the length of the resistor. The bottom Pt (voltage V_3) is accessed and set to ground through the local breakdown of the HZO. 3 different switching cases for resistor terminal voltage V_1, V_2 and coercive voltage V_C demonstrate no, fractional, or full switching. Switching modulates graphene resistance as a multi-level analog resistive memory.

Device Fabrication: 1 µm thermal oxide (SiO_2) was grown on 100 silicon, followed by sputtering and patterning of 200 nm platinum (Pt) as the bottom electrode. Alternating layers of hafnium oxide and zirconium oxide were then deposited by atomic layer deposition (ALD) at 200 ^{0}C using $[(CH_3)_2N]_4Hf$, $[(CH_3)_2N]_4Zr$ and H_2O as the pre-cursors for Hf, Zr, and O respectively [12], with a total thickness of 20 nm, followed by a 3 nm capping layer of alumina (Al_2O_3) in an Arradiant ALD system. Rapid thermal annealing (RTA) for 1 minute in N_2 atmosphere in the range of 250-600 ^{0}C was used to transition the HZO to the orthorhombic phase, which is responsible for ferroelectricity in the material. 100 nm gold (Au) top electrodes were then deposited by thermal evaporation and patterned with a lift-off process. Finally, CVD-grown graphene with sheet resistance of ~ 5-10 kΩ/□ was transferred as the resistive layer with a wet-transfer process, followed by patterning using O_2 plasma [13].

III. EXPERIMENTAL RESULTS

Ferroelectric Characterization: A Sawyer-Tower circuit was used for ferroelectric characterization, with top-electrode only probing. Figure 2 shows the polarization vs electric field (PE) loops of 80 µm diameter HZO capacitors with 1 kHz (83 µs rise/fall time) continuous wave (CW) positive up negative down (PUND) triangular pulses for anneal temperatures from 300-600 ^{0}C, and a control sample that was not annealed. The experimentally observed optimal anneal temperature range to achieve ferroelectricity in HZO is 300-500 ^{0}C with a maximum remnant polarization (P_r) of 15.8 µC/cm^2 and typical coercive field E_C of 1-2 MV/cm. P_r decreases, and E_C increases for anneal temperatures <300 ^{0}C and >500 ^{0}C.

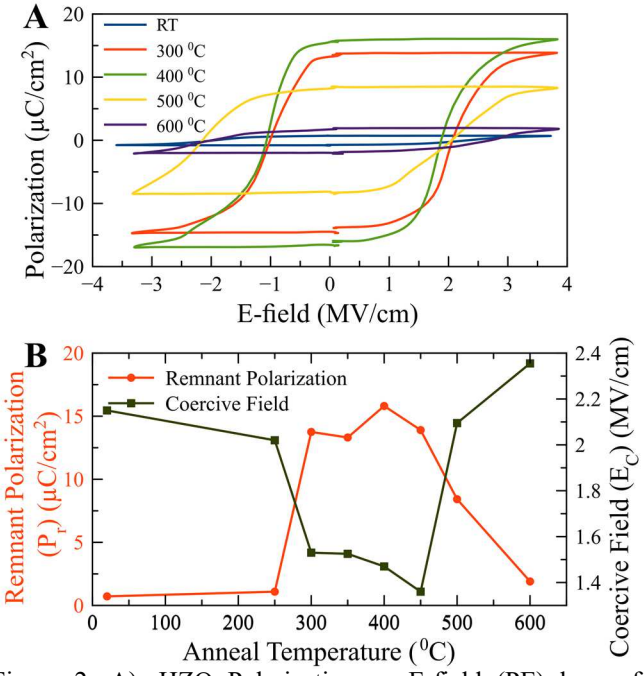

Figure 2: A). HZO Polarization vs E-field (PE) loops for anneal temperate between 200-600 ^{0}C, and control sample at room temperate (RT) B). Remnant polarization (P_r) and coercive field (E_C) as a function of anneal temperature to identify optimal RTA conditions.

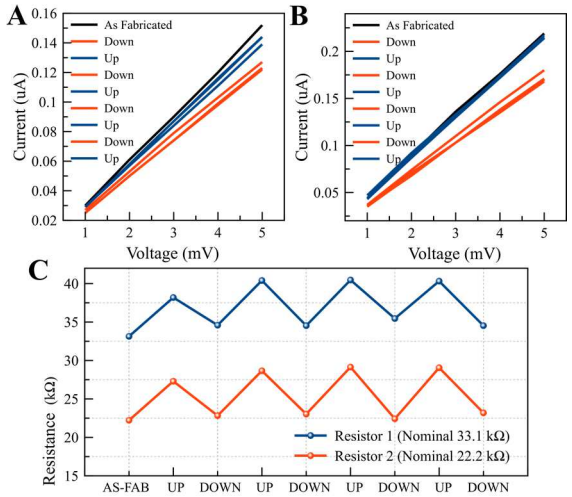

Figure 3: A). and B). DC-IV plots of graphene resistor readout with 1-5 mV bias after up and down switching of the entire length of HZO with E >> E_C, showing reversible resistance modulation between two distinct states. C). Plots of the two distinct resistances on up and down switching cycles.

Hard-switching 2-level resistance modulation: To demonstrate two distinct memory levels of graphene resistive memory with ferroelectric switching, terminals V_1 and V_2 were shorted and continuous wave triangular pulses >V_C and < –V_C were applied to hard-switch (down and up respectively) the entire length of HZO under the graphene. For the tested graphene resistors of 20-35 kΩ of length 80 µm, the measured percentage change in resistance between the two levels was observed to be between 15-30% as shown in Figure 3. The variation in the nominal as-fabricated graphene resistors was attributed to non-uniformities in the CVD graphene due variable grain sizes in different resistors. The differences in fractional change of resistance value during switching can be attributed to graphene-HZO interfacial variations which can influence the ferroelectrically-induced graphene resistance change. For example, a continuous interface between the HZO and graphene would lead to all ferroelectric domains modulating the carriers in graphene, whereas any deviation from this due to imperfect adhesion or trapped charges will limit the number of ferroelectric domains that modulate graphene resistance.

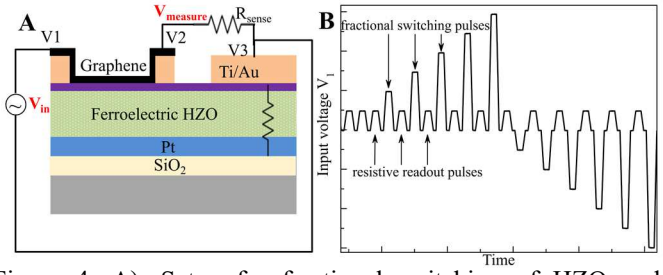

Figure 4: A). Setup for fractional switching of HZO and resistive readout of analog programming of memory in graphene B). Example waveform for V_{in} with increasing *voltage pulses for increased fractional switching in HZO, alternating with resistive readout at small biases.*

Fractional-switching multi-level resistance modulation: Figure 4A shows the setup for fractional ferroelectric switching and resistive readout measurements. The CW input voltage V_{in} is applied across a series combination of the modulated graphene resistor R_g and a fixed sense resistor R_{sense}. The other end of R_{sense} and the Pt bottom electrode are connected to ground. Hence, the potential difference across the graphene resistor is:

$$\Delta V = V_1 - V_2 = V_{in}\left(\frac{R_g}{R_{sense} + R_g}\right)$$

By choosing a suitable R_{sense} and appropriate V_{in}, a target potential difference ΔV can be realized, which in turn enables control of the extent of fractional switching. V_2 (measured with a NIDAQ) is a direct measurement of R_g, which is modulated due to the fractional switching. For this report R_{sense} = 11.8 kΩ was used, which provides appropriate voltage division with the 20-30 kΩ graphene-on-HZO resistors that were tested. Figure 4B shows a representative input waveform for V_{in}. Successively increasing voltage pulses are applied such that they: 1. Produce sufficiently large electric field through the HZO and initiate switching and 2. Generate fractional switching along the length of the graphene resistor. Alternating with the switching pulses, resistive readout of the switching is performed at small voltage biases which does not produce any switching current.

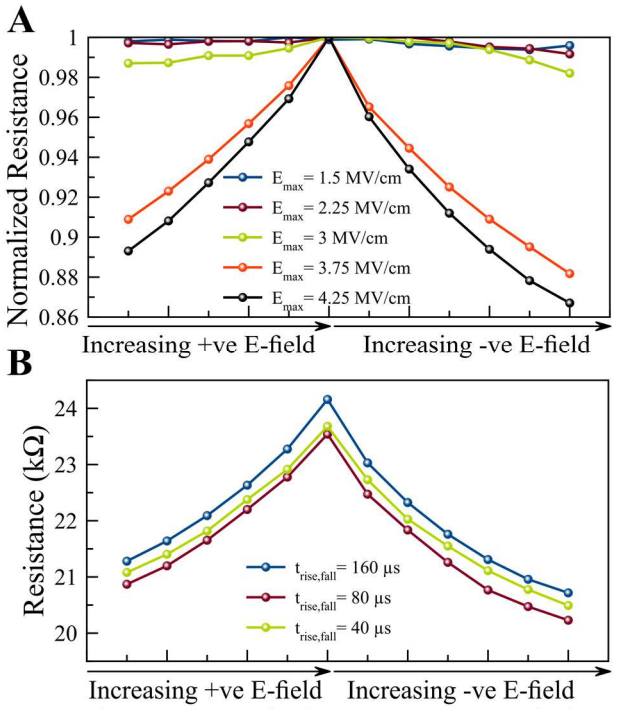

Figure 5: A). Readout of normalized resistance of a 22 kΩ graphene resistor for increasing peak applied E-field (E_{max}). E_{max} < 3 MV/cm produces minimal fractional switching and almost no resistance modulation. Larger E_{max} up to 4.25 MV/cm produces up to 13.3 % fractional change in resistance. B). Frequency-dependence of resistance programmability with varying input pulse rise and fall times (40, 80, and 160 µs) shows little variation in the analog levels achieved, indicating stable fractional ferroelectric switching with pulse frequencies from 3.1 to 12.5 kHz.

Symmetric input for fractional ferroelectric switching: Figure 5A shows a plot of the normalized resistance of a nominally 22 kΩ graphene resistor for increasing maximum E-field (E_{max}) and corresponding decreasing negative $-E_{max}$, from ±1.5 MV/cm to ±4.25 MV/cm with symmetrically increasing and decreasing positive and negative pulses respectively (6 switching pulses each). For $|E_{max}|$ < 3 MV/cm, resistance programmability is <2%, likely due to limited fractional switching in the channel. For larger values of E_{max}, analog programmability of the resistance is achieved with larger fractional switching of HZO, and a peak resistance modulation of 13.3% was measured for E_{max} = 4.25 MV/cm. The largest value for $|E_{max}|$ was limited to 4.25 MV/cm to prevent dielectric breakdown in HZO. Figure 5B plots the programmed resistance levels for 3 different rise/fall/hold times (40, 80, and 160 µs) of the 6-pulse switching input waveform. The result shows a weak frequency-dependence of the analog levels achieved with each voltage, indicating that the switching is stable on these timescales.

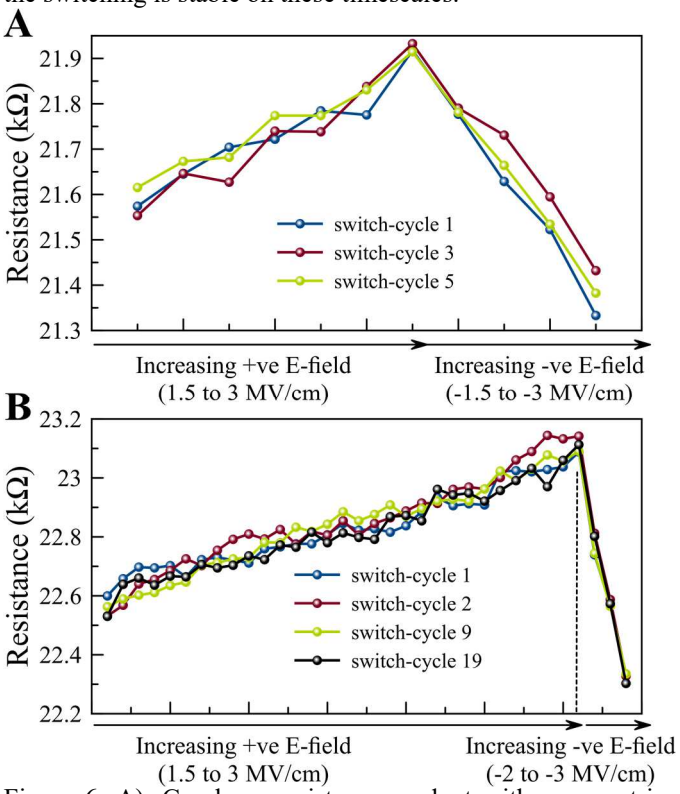

Figure 6: A). Graphene resistance readout with asymmetric fractional switching in HZO using higher granularity on the down-switching cycle (7 and 31 states respectively) and coarse control on up-switching (4 and 3 states respectively). The data shows repeatable and reversible control of graphene resistance modulation, showing multi-level ferroelectrically-induced analog resistance control.

Asymmetric input for fractional ferroelectric switching: To demonstrate the ability to achieve different numbers of analog levels on the up and down switching cycles, asymmetric input waveforms were applied such that a larger number of input pulses were applied for down-switching (n_{down}) for higher

granularity with increasing E-fields, and fewer pulses were applied for coarser up-switching (n_{up}). Figures 6A and 6B show two separate test cases where $n_{down} = 7, n_{up} = 4$ and $n_{down} = 31, n_{up} = 3$ respectively for a range of E-fields from 1.5 to 3 MV/cm. The CW input switching demonstrates reversible and repeatable resistance programmability in both cases, with discrete levels of graphene resistance readout as an outcome of resistance modulation due to the fractional switching of the underlying HZO over multiple cycles.

IV. Discussion

For analog resistance control, the variation in each of the individual resistance states is limited by the input voltage control and is noisy because no averaging was performed in each switching measurement. With finer voltage control and higher averaging, the repeatability of this measurement can be substantially improved, especially for applications in neuromorphic computation where analog weights need infrequent updating. The number of resistance states is dependent on the grain-size of the graphene and the HZO domains. With typical lengths of 20-40 nm for the domains, individual domain control for a 1 µm long graphene resistor can yield 25-50 states for resistive control which will enable aggressive scaling of the technology for storage of weights.

The device architecture and the analog resistance modulation scheme presented in this paper is well-suited for extension to other 2D-on-ferroelectric systems. In particular, III-V ferroelectrics such as scandium aluminum nitride ($Al_xSc_{1-x}N$) have box-like PE loop characteristics and substantially larger remnant polarization > 100 µC/cm^2, which can enable larger resistance control [14], provided that the large coercive field (> 4 MV/cm) can be reduced for CMOS-compatible operation and to ensure that the graphene current-carrying limits are not exceeded [15]–[17].

V. Conclusions and Future Work

In conclusion, this paper presents multi-level analog programmability of resistive readout memory in 2-dimensional graphene resistors on top of 20 nm ferroelectric HZO using programming voltages up to 8V with 13% resistance modulation of a nominal 22 kΩ resistor. The architecture lays down the groundwork to integrate the stack in arrays, integrated with CMOS. The programmable stack also can be micromachined to form released NEMS ferroelectric switches with partial polarization switching for ultra-low power analog computational MEMS devices.

Acknowledgments

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