# N-polar GaN/AlGaN/AlN high electron mobility transistors on single-crystal bulk AlN substrates

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## ABSTRACT

Recent observation of high density polarization-induced two-dimensional electron gases in ultra-thin N-polar GaN layers grown on single-crystal AlN has enabled the development of N-polar high electron mobility transistors (HEMTs) on AlN. Such devices will take advantage of thermal and power handling capabilities of AlN, while simultaneously benefitting from the merits of N-polar structures, such as a strong back barrier. We report the experimental demonstration of N-polar GaN/AlGaN/AlN HEMTs on single-crystal AlN substrates, showing an on-current of 2.6 A/mm with a peak transconductance of 0.31 S/mm. Small-signal RF measurements revealed speeds exceeding $f_t/f_{max} = 68/100$ GHz. These results pave the way for developing RF electronics with excellent thermal management based on N-polar single-crystal AlN.

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Recently observed two-dimensional electron gas (2DEG) induced by polarization in a N-polar GaN/AlGaN/AlN heterostructure grown on single-crystal bulk AlN substrates opened the possibility of developing RF electronics with excellent thermal management.[1] Taking advantage of the combination of large thermal conductivity ($\sim$340 W/m · K)[2] and energy bandgap ($\sim$6.1 eV), high electron mobility transistors (HEMTs) on single-crystal AlN substrates benefit from high breakdown voltage and an efficient heat conduction path from the active region.[3] Importantly, for HEMTs with AlN buffer layers, no deep level dopants are needed. This is in contrast to the conventional Al(Ga)N/GaN HEMTs, where deep level dopants are needed to compensate high unintentional doping concentration of thick epitaxial GaN buffer layers in order to suppress the buffer leakage current and RF loss. These advantages of AlN HEMTs gave rise to increased interest in utilizing AlN for high-power, high-frequency, and extreme environment applications.[4–15] Highly scaled AlN/GaN/AlN HEMTs on SiC, enabled by large bandgap and spontaneous polarization of AlN,

have previously demonstrated an effective breakdown field of 2 MV/cm and a cutoff frequency of 161 GHz.[16]

AlN HEMTs can further benefit from single-crystal bulk AlN substrates. Whereas heterostructures grown on foreign substrates (SiC, Si, or sapphire) show a relatively high dislocation density of $10^9$–$10^{10}$ cm$^{-2}$ throughout the device structure, homoepitaxial AlN films can achieve a remarkably low dislocation density of $10^4$–$10^5$ cm$^{-2}$ on single-crystal AlN substrates, thanks to the absence of lattice mismatch at the growth interface.[9] This reduced dislocation density is favorable for device reliability, improved breakdown voltage, and higher thermal conductivity.[17] Furthermore, the recently reported high thermal boundary conductance between the homoepitaxial AlN film and bulk AlN substrates indicates that such substrates may allow efficient heat removal by the elimination of the boundary.[18] The importance of high thermal boundary conductance for heat removal has been highlighted in a previous study, where it was theoretically shown that the temperature rise due to dissipated power is lower for AlN grown on single-crystal AlN substrates

compared to AlN grown on SiC or diamond substrates, despite the higher thermal conductivity of SiC ($\sim$420 W/m · K) and diamond ($\sim$2000 W/m · K).[19]

In addition to the advantages of a homoepitaxial AlN buffer layer, a N-polar HEMT on bulk AlN substrates is expected to benefit from the reverse polarization field of N-polar heterostructures, which unlocks the potential for a strong back barrier and improved large-signal RF performance.[20–22] This is evidenced by the current state-of-the-art N-polar HEMT that exhibits an output power over 8 W/mm up to 94 GHz.[23] Furthermore, together with the recent discovery of two-dimensional hole gases in metal-polar GaN/AlN heterostructures grown on the bulk AlN substrates of the opposite polarity,[24] the development of N-polar HEMTs presented in this work further raises hope for the manufacture of CMOS-augmented nitride integrated circuits for applications in RF and power electronics.[11]

Despite these advantages, N-polar HEMTs on bulk AlN substrates have not yet been demonstrated. This is primarily due to the

difficulties in ensuring reliable gate control, stemming from a low Schottky barrier height of N-polar GaN,[25,26] and problems associated with epitaxial growth on chemically reactive N-polar AlN substrates, such as polarity inversion. To combat this challenge in epitaxy, a novel *in situ* surface cleaning technique was recently developed to enable high-quality N-polar AlN homoepitaxy.[27,28] This prior work has paved the way for the demonstration of N-polar HEMTs on bulk AlN platform in this work.

Here, we demonstrate the DC and RF performance of N-polar HEMTs on single-crystal AlN substrates. Taking advantage of the high conductivity polarization-induced two-dimensional electron gas (2DEG), the N-polar device exhibits promising DC and RF characteristics, such as an on-current of 2.6 A/mm and a maximum oscillation frequency ($f_{max}$) of 100 GHz.

The device structure used in this study, along with a simulated energy band diagram and electron density profile under the gate, is shown in Figs. 1(a)–1(c). The boundary conditions used for the
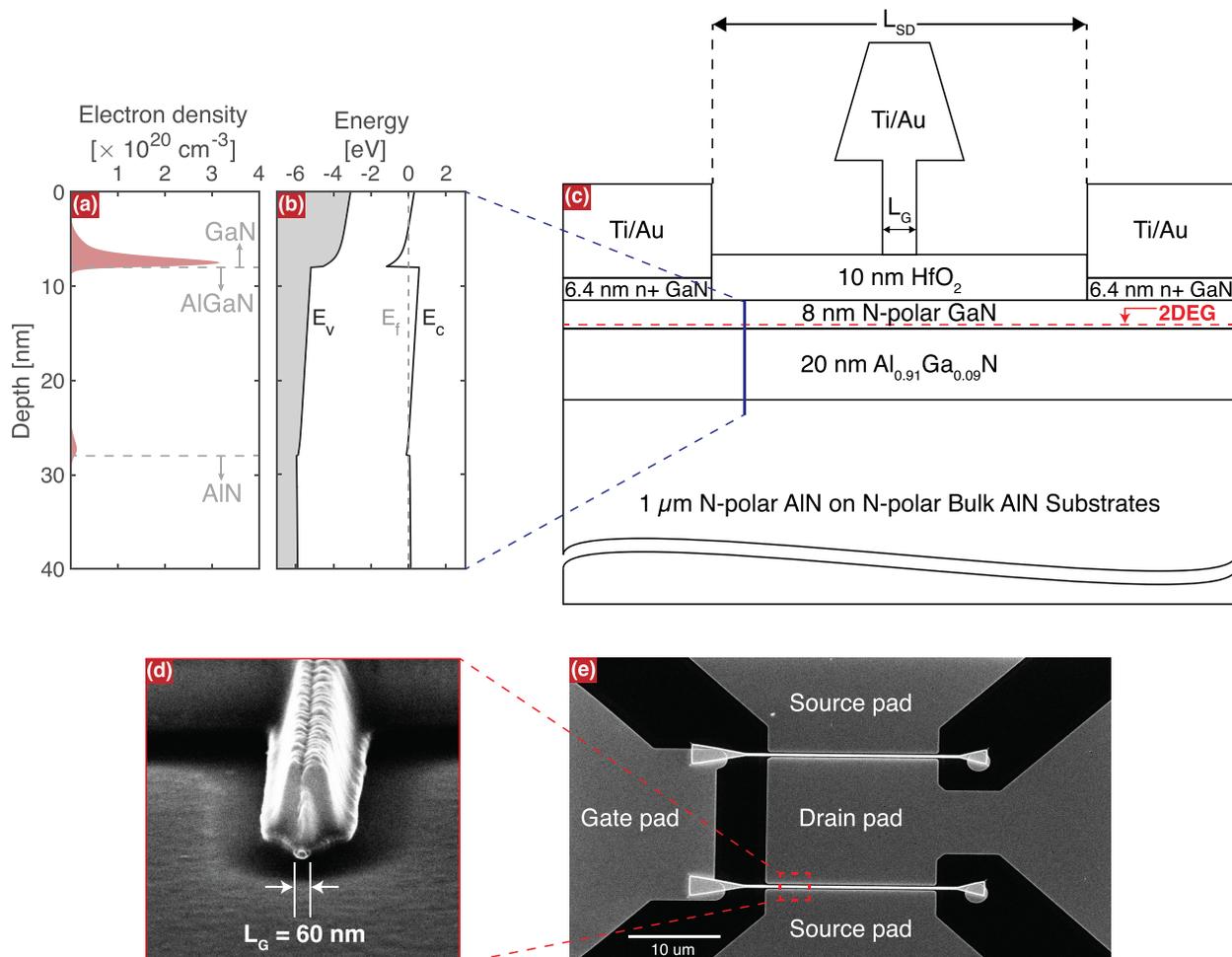


**FIG. 1.** (a) An electron density profile and (b) energy band diagram under the gate simulated by a self-consistent 1D Schrödinger–Poisson solver. (c) Cross-sectional representation of scaled N-polar GaN/Al$_{0.91}$Ga$_{0.09}$N/AlN HEMTs on bulk AlN substrates with an EBL defined T-gate. SEM images of (d) a 60 nm T-gate cross section and (e) top-down view of a fully processed HEMT with W$_G$ = 2 × 25 $\mu$m and L$_{SD}$ = 800 nm.

simulation include a surface barrier height of 0.3 eV for N-polar GaN[29,30] and a zero electric field deep inside the bulk AlN. Other material parameters used for the simulation are listed in Ref. 1. The n+ GaN/GaN/AlGaN/AlN epitaxial structure was grown by plasma-assisted molecular beam epitaxy (PAMBE) on 100 $\mu$m thick free standing N-polar AlN substrates with a dislocation density $<$ $10^4$ cm$^{-2}$ from Asahi-Kasei Corporation.[31] The as-grown N-polar heterostructure consists of a 1 $\mu$m AlN buffer layer, a 20 nm Al$_{0.91}$Ga$_{0.09}$N impurity blocking layer,[32] and a 8 nm GaN channel capped with a heavily Si-doped 6.4 nm n+ GaN layer ($N_D \sim$ $10^{20}$ cm$^{-3}$). Further details on epitaxial growth of such heterostructures are presented in Ref. 1. The purpose of the n+ GaN capping layer is the easy formation of non-alloyed ohmic contacts as an alternative to epitaxially regrown contact technology. The absence of an electrically resistive top barrier in this N-polar heterostructure enables the *in situ* growth of n+ GaN. Non-alloyed source and drain ohmic contacts are formed by simply depositing metal pads on top and removing the excess n+ GaN that is not needed. However, with a thin 8 nm GaN channel and no etch stop layer, n+ GaN recess etching can give rise to plasma damage on the channel and etch non-uniformity issues. The effect of nonselective n+ GaN etch on device performance and reliability would need to be carefully investigated in the future. It should be noted that in Fig. 1(c), although the schematic is drawn as if the n+ GaN etch was stopped right at the GaN surface, it may not be an accurate depiction due to the absence of an etch stop layer.

Prior to device fabrication, room temperature Hall-effect measurements showed an electron mobility of 487 cm$^2$/V · s and an electron density of $5.3 \times 10^{13}$ cm$^{-2}$, resulting in a sheet resistance of 242 $\Omega$/sq. Although a self-consistent calculation using a 1D Schrödinger– Poisson solver suggests the existence of a parallel 2DEG channel at the bottom Al$_{0.91}$Ga$_{0.09}$N/AlN interface, no measurable conductivity was observed in a control sample in which the epitaxial growth was stopped after the AlGaN layer. Therefore, the charge transport in the epitaxial structure is likely to be dominated by the 2DEG channel at the GaN/Al$_{0.91}$Ga$_{0.09}$N interface and the conductive n+ GaN layer on top. Hall-effect measurements performed on a separately grown N-polar n+ GaN layer on semi-insulating Bulk GaN

substrates revealed an electron mobility of 58 cm$^2$/V · s and an electron density of $5.2 \times 10^{14}$ cm$^{-2}$, corresponding to a sheet resistance of 209 $\Omega$/sq. Capacitance–voltage (C–V) profiling may help to confirm the nonexistence of the parallel channel, but accurate C–V data were not attained due to high leakage currents.

Device fabrication began with the blanket deposition of a 10 nm Al$_2$O$_3$ layer via thermal atomic layer deposition (ALD) to protect the underlying N-polar layer during device processing. Source and drain non-alloyed ohmic contacts were then defined by photolithography, and Al$_2$O$_3$ in the opened contact windows was removed prior to the deposition of the Ti/Au/Ni (40/100/10 nm) ohmic metal stack. Next, mesa isolation was performed by BCl$_3$ inductively coupled plasma (ICP) etch that extended 10 nm into the Al$_{0.91}$Ga$_{0.09}$N layer. Prior to the gate dielectric deposition, the remaining Al$_2$O$_3$ was removed and the n+ GaN cap between source and drain contacts was removed via low power, timed BCl$_3$ ICP etch at a rate of 1.8 nm/min using the previously deposited Ti/Au/Ni metal stack as a hard mask. After global-recess etching of n+ GaN, 10 nm ALD HfO$_2$ was blanket deposited at 300 °C. Finally, T-shaped gates were defined by electron beam lithography (EBL) using a ZEP520a/PMGI/ZEP520a tri-layer resist stack and metalized by Ti/Au (40/300 nm) e-beam evaporation. Figures 1(d) and 1(e) show scanning electron microscope images of a fully processed device as well as a cross section of a T-gate. The devices discussed in this study were not passivated. Unless otherwise specified, all measured HEMTs in this study feature an 800 nm source-to-drain distance (L$_{SD}$), a 2 × 25 $\mu$m device width (W$_G$) with a gate pitch of 20 $\mu$m, and a T-gate placed in the middle of the source-to-drain spacing with a 60 nm gate length (L$_G$).

Following the n+ GaN recess etching, room temperature Hall-effect measurements in van der Pauw geometry were performed to assess the recess etch depth. Comparing with the as-grown structure, a 2DEG density was reduced from $5.3 \times 10^{13}$ to $3.8 \times 10^{13}$ cm$^{-2}$, resulting in a sheet resistance of 322 $\Omega$/sq. These values match well with those of a separately grown sample without a n+ GaN capping layer, from which a 2DEG density of $4.1 \times 10^{13}$ cm$^{-2}$ and a sheet resistance of 311 $\Omega$/sq were measured. Therefore, we expect the final etch depth to be reasonably close to the thickness of a n+ GaN capping layer.
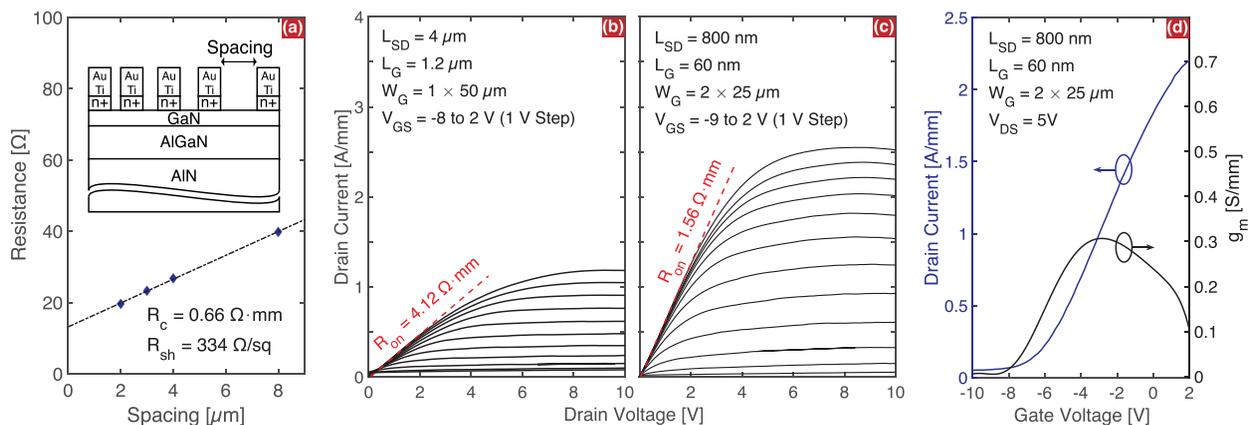


**FIG. 2.** (a) Linear TLM analysis, measured after the global recess etching of the n+ GaN capping layer. Output characteristics of (b) a long-channel HEMT with a rectangular gate defined by photolithography and (c) a scaled HEMT with an EBL defined T-gate, demonstrating a good device scaling behavior. (d) Transfer characteristics of a scaled HEMT in a linear scale, showing a peak extrinsic transconductance of 0.31 S/mm.

After the recess etch, a contact resistance of $R_C = 0.66\ \Omega \cdot$ mm (from the metal pad to the 2DEG) and a sheet resistance of $R_{sh} = 334\ \Omega/$sq were extracted by the transfer length method (TLM), as shown in Fig. 2(a), which is in good agreement with the Hall-effect measurement results. This unoptimized contact resistance is relatively high compared to that of N-polar HEMTs with regrown contacts commonly reported in the literature.[33,34] However, a contact resistance as low as 0.14 $\Omega \cdot$ mm has been reported using an *in situ* n+ GaN capping layer without regrowth process,[22] and therefore, we believe a lower contact resistance will be achieved in the future.

Figures 2(b) and 2(c) show measured output curves ($I_D\ V_D$) of a long-channel HEMT with a rectangular gate defined by photolithography and a scaled HEMT with an EBL defined T-gate, respectively. It is seen that the on-resistance ($R_{on}$) decreases from 4.12 to 1.56 $\Omega \cdot$ mm and the maximum drain current ($I_D$) increases from 1.2 to 2.6 A/mm, demonstrating good scaling behavior. This high drain current with excellent saturation demonstrates high potential of N-polar HEMTs on bulk AlN substrates.

The DC transfer measurements shown in Fig. 2(d) revealed relatively modest pinch-off characteristics with an off-state drain current exceeding 50 mA/mm, which is caused by high gate leakage. The exact causes of this high leakage current are not fully understood and require further investigation. The DC transfer measurement also revealed a peak extrinsic transconductance $g_m = 0.31$ S/mm. Following $g_m^{int} = C_{gs}v_{sat}$ and $g_m = g_m^{int}/(1 + R_S g_m^{int})$, an expected $g_m = 0.36$ S/mm is calculated, which matches relatively well with the experimentally measured value. The parameters used for this calculation include saturation velocity $v_{sat} = 10^7$ cm/s,[35] measured unoptimized dielectric constant $\varepsilon_{r,HfO_2} = 12$, $\varepsilon_{r,GaN} = 8.9$, and the source resistance $R_S = 0.78\ \Omega \cdot$ mm. If $R_C = 0.07\ \Omega \cdot$ mm and $\varepsilon_{r,HfO_2} = 17$ are achieved,[36,37] the expected $g_m$ will increase to 0.53 S/mm and $R_{on}$ will be reduced to 0.38 $\Omega \cdot$ mm for this device geometry.

Buffer leakage was evaluated using a test structure fabricated by removing the active region of some HEMTs on the same chip via BCl$_3$ ICP etch, as shown in Fig. 3(a). A homoepitaxial AlN film showed excellent electrical resistivity, resulting in a buffer leakage current as low as 13 nA/mm and 5 $\mu$m/mm at 200 V for 20 and 2 $\mu$m spacing between two ohmic contacts, respectively. The same measurement was also performed on a test structure consisting of a 500 nm Al-polar AlN buffer layer grown on SiC with regrown GaN contacts, similar to the heterostructure presented in Ref. 16. It was revealed that the leakage current through a homoepitaxial AlN buffer layer is approximately two orders of magnitude lower than that through an AlN buffer layer grown on SiC. This lower leakage is attributed to the lower dislocation density when grown on single-crystal AlN substrates, as deep level traps formed by dislocations can provide paths for leakage current.[38,39] Although an Al(Ga)N buffer layer can be rendered semi-insulating by incorporating Fe or C, degradation of crystalline quality and increased current collapse have been reported as a result.[40] On the contrary, utilizing a low dislocation density homoepitaxial AlN buffer layer helps to reduce buffer leakage current, thereby suppressing the short-channel effect, without any consequential adverse effect.

To evaluate the speed of the devices, bias-dependent scattering parameters were measured using a Keysight N5247B vector network analyzer in the frequency range of 100 MHz to 67 GHz. After de-embedding parasitics using on-wafer open and short probe pads, a forward current gain cutoff frequency $f_t = 68$ GHz and a maximum frequency of oscillation $f_{max} = 100$ GHz were extracted by extrapolating $|h_{21}|^2$ and a unilateral ($U$) gain, respectively, following the $-20$ dB/dec slope, as shown in Fig. 3(b). The main limitation of $f_t$ in this device is the high parasitic source resistance and low transconductance, which can be improved by reducing the contact resistance and improving the gate stack.[41] Another factor limiting the $f_t * L_G$ product may be the low average channel electron velocity, stemming from a
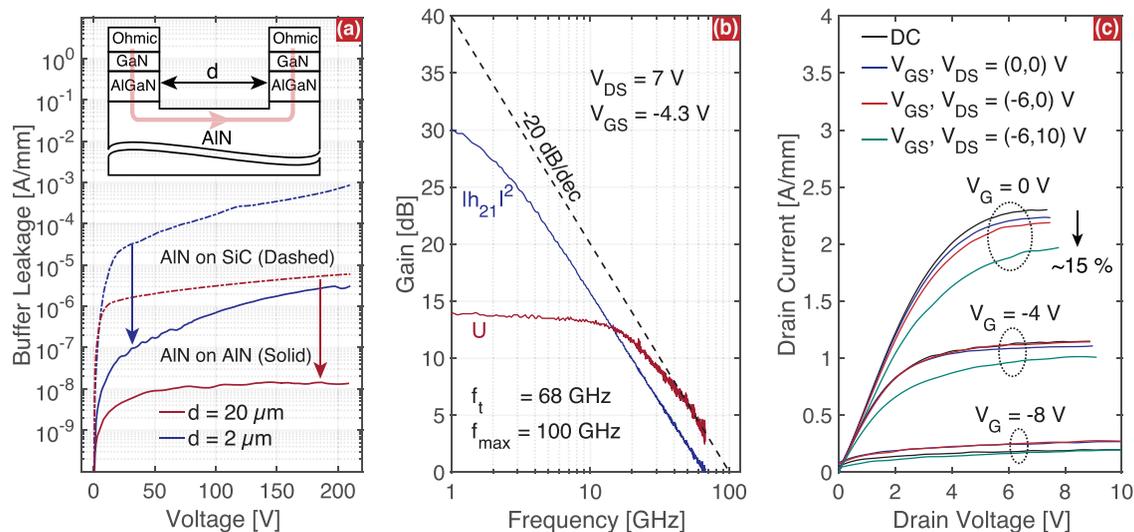


**FIG. 3.** (a) Buffer leakage current measured on a test structure fabricated by removing the active region of a HEMT. It is shown that a homoepitaxial AlN buffer layer exhibits excellent electrical resistivity, even lower than that through an AlN buffer layer grown on SiC substrates. (b) Small-signal characteristics for a HEMT with $L_G = 60$ nm and $L_{SD} = 800$ nm. (c) Pulsed $I_D V_D$ measurements for a 500 ns pulse with 0.05% duty cycle at a bias of $V_G = 0$, $-4$, and $-8$ V. A 15% dispersion is observed in the saturation region at 10 V drain lag conditions.

high 2DEG density of the HEMTs at the quiescent bias point. It has been reported that due to the strong electron-optical-phonon scattering and long lifetime of longitudinal optical phonon in GaN HEMTs, the electron velocity is locked by the optical-phonon emission, with the end result being the decreasing saturation velocity with increasing 2DEG density.[35,42] Therefore, the N-polar HEMTs presented in this study may benefit from the reduced 2DEG density under the gate and reduced gate leakage, by modifications of heterostructure design, such as lowering the Al composition in the $Al_{0.91}Ga_{0.09}N$ layer to decrease the polarization offset.

Pulsed $I_D V_D$ measurements were performed to investigate the dispersion control of the unpassivated HEMTs. As shown in Fig. 3(c), low current collapse was observed for the drain current drive pulsed from quiescent gate, drain bias of $-6, 0$ V, and the drain current drive pulsed from $-6, 10$ V showed maximum current collapse of 15% as well as a moderate knee walkout at a bias of $V_{GS} = 0$ V.

In summary, the previously unstudied N-polar HEMTs on freestanding AlN substrates were demonstrated, showing a high on-current of 2.6 A/mm, a high speed ($f_t/f_{max} = 68/100$ GHz), and very low buffer leakage. While there is large room for future improvement, such as reducing contact resistance and gate leakage suppression, these results mark important milestones toward highly reliable RF electronics with excellent thermal management based on N-polar AlN HEMTs.

## AUTHOR DECLARATIONS
### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

Eungkyun Kim and Zexuan Zhang contributed equally to this work.

**Eungkyun Kim:** Conceptualization (lead); Investigation (lead); Methodology (lead); Validation (lead); Writing – original draft (lead). **Debdeep Jena:** Conceptualization (lead); Funding acquisition (lead); Investigation (supporting); Methodology (supporting); Project administration (lead); Resources (lead); Supervision (lead); Validation (supporting); Writing – review & editing (lead). **Huili Grace Xing:** Conceptualization (lead); Funding acquisition (lead); Investigation (supporting); Methodology (supporting); Project administration (lead); Resources (lead); Supervision (lead); Validation (supporting); Writing – review & editing (lead). **Zexuan Zhang:** Conceptualization (lead); Investigation (lead); Methodology (lead); Validation (lead); Writing – original draft (supporting). **Jimy Encomendero:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Validation (supporting). **Jashan Singhal:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Validation (supporting). **Kazuki Nomoto:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Validation (supporting). **Austin Hickman:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Validation (supporting). **Cheng Wang:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Validation (supporting). **Patrick J. Fay:** Investigation (supporting); Methodology (supporting); Validation (supporting). **Masato Toita:** Funding acquisition (lead); Project administration (lead); Resources (lead).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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