Strain-balanced AlScN/GaN HEMTs with f_T/f_{MAX} of 173/321 GHz

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***Abstract*—We report the effect of scaling the gate length from 0.8 μm to 40 nm on the performance of novel strain-balanced AlScN/GaN high electron mobility transistors (HEMTs) on SiC substrates. A new strain-balanced heterostructure is introduced where the tensile strain of the AlN interlayer is balanced by the compressive strain in the AlScN barrier layer. MBE regrown source/drain ohmics with ultralow contact resistance of 0.09 Ω·mm allow a low HEMT on resistance of 0.83 Ω·mm. The shortest gate length AlScN/GaN HEMTs exhibit maximum drain currents of 2.8 A/mm, peak transconductance of 0.55 S/mm, and speed characterized by f_T/f_{MAX} of 173/321 GHz. The highest f_{MAX} obtained here is ∼2X higher than previous AlScN HEMTs.**

I. Introduction

GaN HEMTs benefit from the combination of large energy bandgaps, high breakdown electric field, and high conductivity polarization-induced two-dimensional electron gas (2DEG) channels to deliver state-of-the-art X- to W-band power amplifiers [1]. The AlGaN/GaN HEMTs employed in RF and power electronics applications today are hitting their performance limits. Fig. 1 (a) indicates that replacing the traditional AlGaN barrier with tensile-strained binary AlN, or lattice-matched ternary AlInN enhances scaling. Lattice-matched AlScN is seen to have a wider bandgap than lattice-matched AlInN. Fig. 1 (b) shows how scaling is enabled by boosting the 2DEG density for smaller barrier thicknesses than AlGaN using AlInN, AlScN, or AlN barriers. The ≤6 nm limitation imposed by tensile strain for AlN barrier thickness, and of $\leq 2 \times 10^{13}$/cm^2 2DEG charge in AlInN barrier HEMTs are overcome by novel AlScN barriers which also offer high-k [2] and ferroelectric [3] properties. In spite of their high on currents [4] and appreciable mm-wave output power [5], the benchmarking of GaN HEMT barriers in Fig. 1 (c) shows that AlScN barrier HEMTs lag in $f_{MAX} \leq 156$ GHz [4].

Because AlN interlayers between AlScN and GaN boost channel mobility, Fig. 1 (a) and (d) show that a combination of a tensile-strained AlN with a *compressively* strained AlScN is needed for strain balance. We have realized this strained balanced heterostructure in this work. Employing improved n$^+$GaN regrown source/drain Ohmic contacts and ultrascaled gate lengths down to 40 nm T-gates, the new strain-balanced AlScN barrier HEMTs exhibit $I_{max} \sim 2.8$ A/mm, and f_T/f_{MAX} of 173/321 GHz.

II. Epitaxial Design and Growth

AlScN lattice-matches to GaN at around 10% Sc mole fraction, as seen in Fig. 1 (a). To counter the tensile strain of a 1.5 nm AlN interlayer indicated in Fig. 1 (d), we chose 5 nm 13% Sc composition AlScN, followed by a 2 nm GaN cap as the gate barrier epi-stack. Fig. 2(a) shows an energy band diagram and channel carrier density profile of this strain-balanced gate stack evaluated by self-consistently solving Schrödinger and Poisson equations. The 2DEG wavefunction squared is prevented from spatial overlap with the $Al_{0.87}Sc_{0.13}N$ layer by the AlN interlayer to minimize alloy scattering [6].

We grew the designed strain-balanced heterostructure shown in Fig. 2 (c) by plasma-assisted molecular beam epitaxy (MBE) directly on semi-insulating 4H-SiC substrates. We first grew a 100 nm AlN nucleation layer, and a 600 nm unintentionally doped (UID) GaN layer, before inserting the new strain balanced gate stack. Fig. 2(b) shows the surface morphology after epitaxial growth. A root mean square roughness of 0.770 nm by AFM is measured for the strain-balanced heterostructure, comparable to previous AlScN/GaN HEMTs that do not use strain balanced barriers [4], [7].

III. Device design and fabrication

Fig. 2 (c) shows the device process flow that we used to fabricate scaled AlScN HEMTs from the epitaxial wafer, indicating the steps and a schematic cross-section of the resulting HEMT. We first defined the source/drain regions using a SiO_2/Cr hard mask. After ICP etching through the gate barrier into the UID GaN layer using the hard mask, we loaded the wafer back into the MBE chamber and regrew n$^+$GaN contact wells with heavy Si donor doping concentration $N_d \sim 10^{20}$/cm^3. After removal of the masked regions, we deposited Ti/Au source/drain metal stacks on the n$^+$GaN S/D regrown wells. No annealing was necessary. We deposited Ni/Au stack for the gate metal. We combined optical and electron beam lithography (EBL) processes to realize gate lengths ranging from 40 nm $\leq L_g \leq$ 800 nm. The SEM in Fig. 2 (d) shows the top view source, drain, and gate metal pads on the fabricated sample. The SEM inset shows a T-gate with $L_g = 40$ nm.

IV. Results and discussion

Fig. 3 (a) shows the effect of processing on the Hall effect transport properties of the 2DEG channel by comparing values before and after device fabrication. The as-grown sample exhibited 2DEG sheet carrier density $n_s \sim 2.5 \times 10^{13}$/cm^2, electron mobility $\mu \sim 755$ cm^2/V.s, and sheet resistance R_{sh} = 337 Ω/sq. After processing of the entire HEMT the Hall effect data measured across several wafer dies on processed van der Pauw patterns with n$^+$GaN contacts are seen to preserve similar transport properties, though with modestly higher sheet resistance, and some variations across the wafer.

Fig. 3 (b) shows the contact resistances between the metal - n$^+$GaN regrown layers, and the n$^+$GaN-2DEG channel extracted by the transfer length method (TLM). The regrown n$^+$GaN to 2DEG contact resistance R_c = 0.09 Ω·cm^2 obtained here is lower than the 0.1-0.3 Ω·cm^2 resistance reported for other high-speed AlScN/GaN HEMT devices [4], [8]–[10]. Fig. 3(c) shows the capacitance-voltage (C-V) profile measured on a 30 μm diameter circular diode in circles, and a Schrödinger-Poisson C-V simulation as a solid line. A dielectric constant k =10.8 is used in the simulation for $Al_{0.87}Sc_{0.13}N$, compared to k = 8.5 for AlN.

Fig. 4 (a) schematically shows the gate length L_g and the source drain distance L_{sd}, which we varied to study scaling. Fig. 4 (b) shows the measured $I_d - V_{ds}$ output characteristics for L_g = 800, 130, and 40 nm, with corresponding scaled L_{sd} for gate width $W = 50$ μm. The $I_{max} = 1.9$ A/mm and $R_{on} = 1.53$ Ω·mm for L_g/L_{sd}= 3000 nm/800 nm is seen to increase to $I_{max} = 2.6$ A/mm and $R_{on} = 0.94$ Ω·mm for L_g/L_{sd}= 130 nm/1000 nm, and further to $I_{max} = 2.8$ A/mm and $R_{on} = 0.83$ Ω·mm for L_g/L_{sd}= 40 nm/600 nm. We observe appreciable output conductance due to short channel effect for both L_g = 130 nm and 40 nm HEMTs. $R_{on} \sim 0.83$ Ω·mm is the lowest for AlScN/GaN HEMTs.

Figs. 5 (a), (b) and (c) show the transfer characteristics $I_d - V_{gs}$ in log scale, linear scale, and extrinsic transconductance $g_{m,ext}$ of a strain-balanced AlScN HEMT with L_g = 800 nm. A moderate on/off ratio of $> 2 \times 10^4$ was measured with off-state current limited by gate-source leakage current similar to previous reports [5], [8], [10]. No trap-related hysteresis was observed at this gate length. A saturation current I_{dss} = 1.7 A/mm at V_{ds} = 10 V and $g_{m,ext}$ = 367 mS/mm were measured for this (optical gate) device. Negligible drain-induced barrier lowering (DIBL) is seen in Fig. 5 (a) and negligible threshold voltage (V_{th}) shift is seen in Fig. 5 (b).

Figs. 5 (d), (e) and (f) show the corresponding $I_d - V_{gs}$ and $g_{m,ext}$ plots for L_g = 40 nm. A similar on/off ratio $\sim 1 \times 10^4$ was measured. The minimal current hysteresis suggests absence of trapping and ferroelectric gating effects compared to previous high-speed FerroHEMTs with 14% Sc AlScN barrier and L_g = 90 nm [4]. Fig. 5 (d) shows DIBL of 80 mV/V in the subthreshold regime. Fig. 5 (e) shows that V_{th} shifts from -4.7 V for V_{ds} = 0.1 V to -5.3 V for V_{ds} = 10 V. The 40 nm T-gate enables I_{dss} = 2.8 A/mm for V_{ds} = 10 V and $g_{m,ext} \sim 550$ mS/mm. Figs. 5 (g) and (h) summarize the dc scaling trends of the strain-balanced AlScN HEMTs.

Fig. 6(a) shows the small signal RF performance of a $L_g = 40$ nm strain-balanced AlScN HEMT. Using a -20 dB/dec extrapolation, we measure f_T/f_{MAX} = 173/321 GHz. These are the highest f_T and f_{MAX} among all AlScN barrier HEMTs reported to date. They exceed the highest values of f_T = 130 GHz [11] and f_{MAX} = 168 GHz [4] for L_g = 90 nm AlScN barrier HEMTs. In Fig. 6(b) we show the f_T and f_{MAX} we measured for various T-gate gate lengths L_g and various L_{sd}. A large number of strain-balanced HEMTs exhibit $f_{MAX} > 210$ GHz for $L_g \leq 130$ nm. Fig. 6(c) benchmarks the small signal RF cutoff frequencies in this work compared to previous reports, highlighting the significant improvement in speed enabled by 40 nm T-gate technology.

We established a small signal equivalent circuit model using circuit elements obtained using a standard extraction procedure [12]. Fig. 7(a) shows the comparison between measured and simulated S parameters of the HEMT in Fig. 6(a). Fig. 7(b) and (c) show the equivalent circuit model and the extracted circuit elements of the HEMT in Fig. 6(a). The extracted parameters are $g_{m,ext}$ = 0.4 S/mm (smaller value than dc), R_{ds} = 247 Ω and C_{gd} = 8 fF, which together result in the high f_T and f_{MAX}. The simulated f_T/f_{MAX} of 174/318 GHz are consistent with the measured values of f_T/f_{MAX} = 173/321 GHz of the strain-balanced AlScN HEMTs.

V. Conclusions and future work

This work shows the high potential of strain-balanced AlScN barrier GaN HEMT performance using highly scaled 40 nm T-gate technology. Achievable 2X improvement in electron mobility and transconductance, coupled with scaled T-gates, low resistance regrown contacts, and appropriate device passivation will enable AlScN/GaN transistors to take GaN HEMT technology to the next generation.

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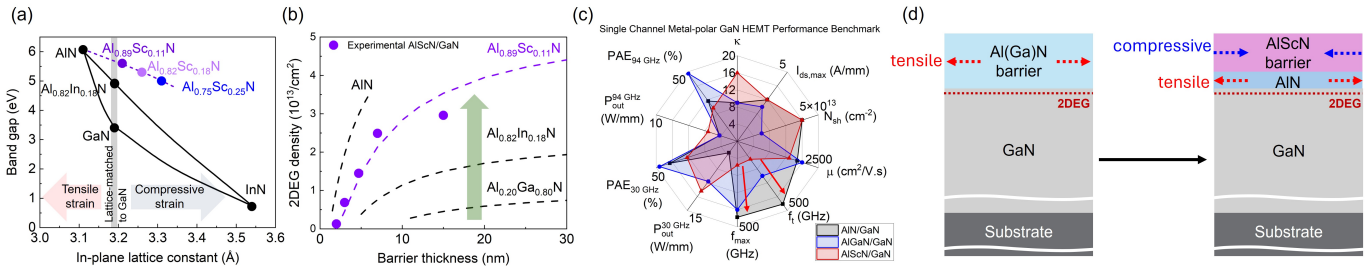


Fig. 1. AlScN is a promising barrier for GaN HEMTs because of (a) its wide bandgap and lattice-matching capability to GaN and (b) high polarizaiton-induced 2DEG density. (c) AlScN/GaN HEMTs benchmarked against state-of-the-art AlGaN/GaN and AlN/GaN single channel HEMTs. (d) Strain balance can be achieved in the barrier layer by countering the tensile strain of the AlN layer with a compressive strain in the AlScN.

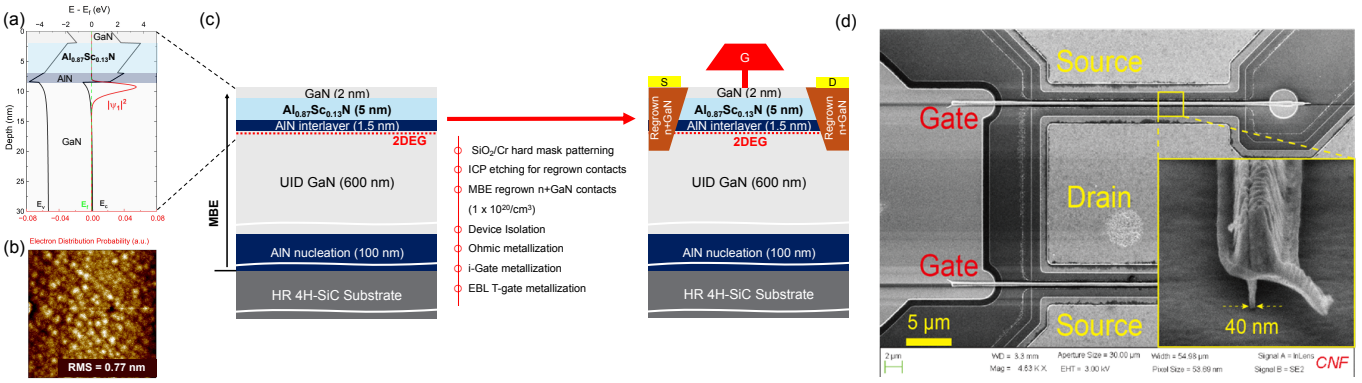


Fig. 2. (a) Energy band diagram of the AlScN/AlN/GaN HEMT heterostructure and (b) AFM micrograph showing as-grown surface morphology of the epitaxial AlScN/AlN/GaN HEMT structure grown by MBE. (c) The representative device process flow of AlScN/GaN HEMTs with MBE regrown n+GaN contacts. (d) The SEM image of a processed HEMT. The SEM inset shows an EBL T-gate with a gate width L_g = 40 nm.

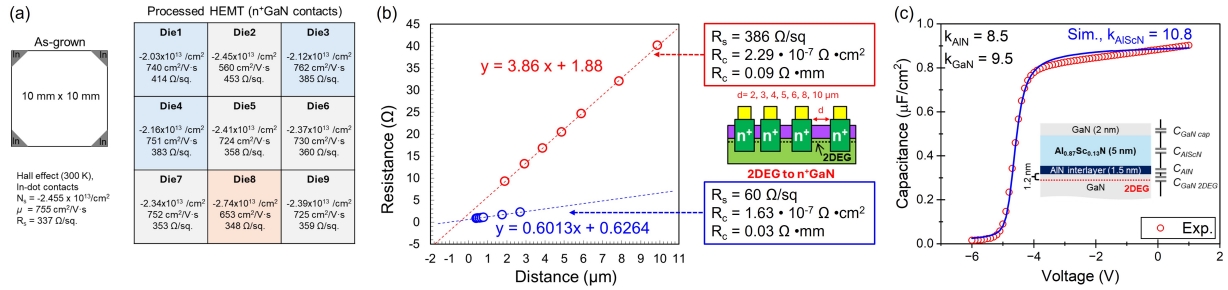


Fig. 3. (a) Hall effect measurements with Van der Pauw pattern showing the transport properties pre- and post-fabrication across device dies. (b) Ultra low contact resistances for the processed HEMT between the metal and the regrown n$^+$GaN regions and the n$^+$GaN regions and the 2DEG. (c) Capacitance-Voltage measurement of a circular gate diode in circles. Solid line is a model with dielectric constant $k_{AlScN} \sim 10.8$.

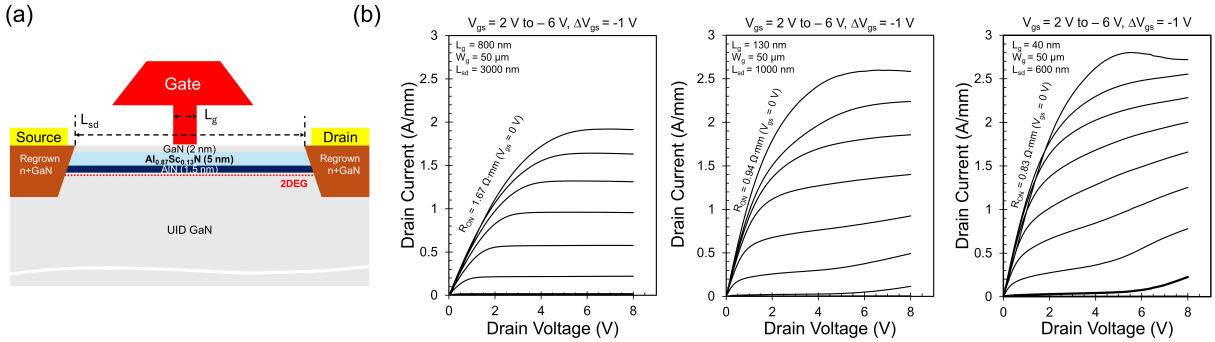


Fig. 4. (a) Strain-balanced AlScN HEMT device cross-section schematic. (b) DC output characteristics of the AlScN/GaN HEMTs with gate length scaling from L_g of 800 nm (optical gate) to 130 and 40 nm (EBL T-gate). Specific device dimensions and measurement conditions are listed in the plots.

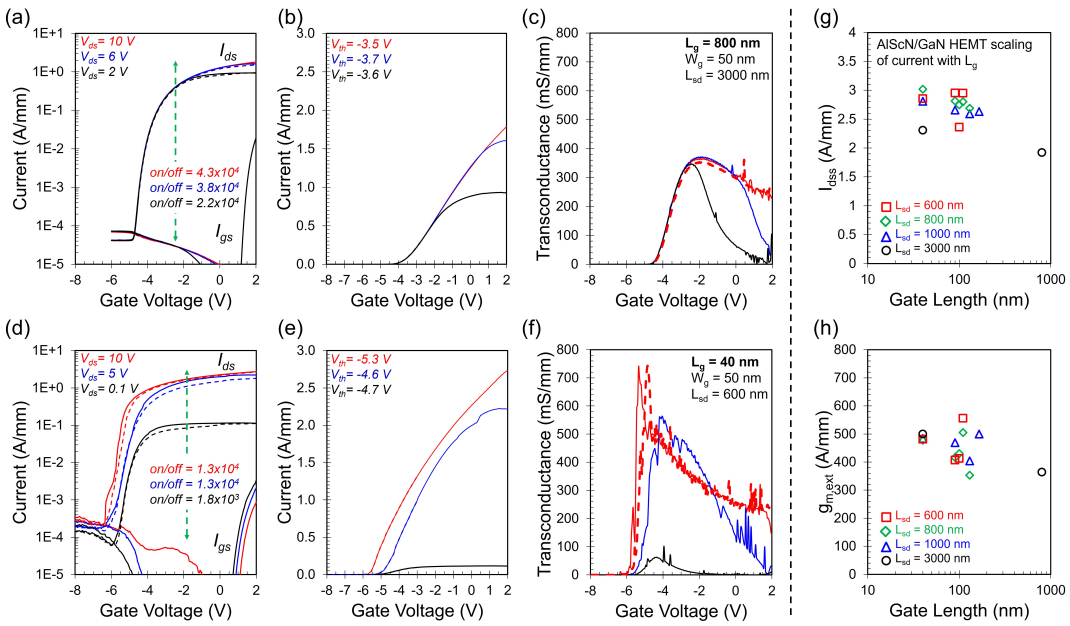


Fig. 5. Measured transfer characteristics of strain-balanced AlScN barrier GaN HEMTs in (a, d) log scale, (b, e) linear scale, and (c, f) transconductance vs. V_{gs} of a HEMT with L_g = 800 nm and with EBL T-gate L_g = 40 nm. Summary of (g) saturation current I_{dss} and (h) transconductance $g_{m,ext}$ as a function of gate length and source-drain distance. Higher saturation current I_{dss} was measured in highly scaled L_g = 40 nm devices.

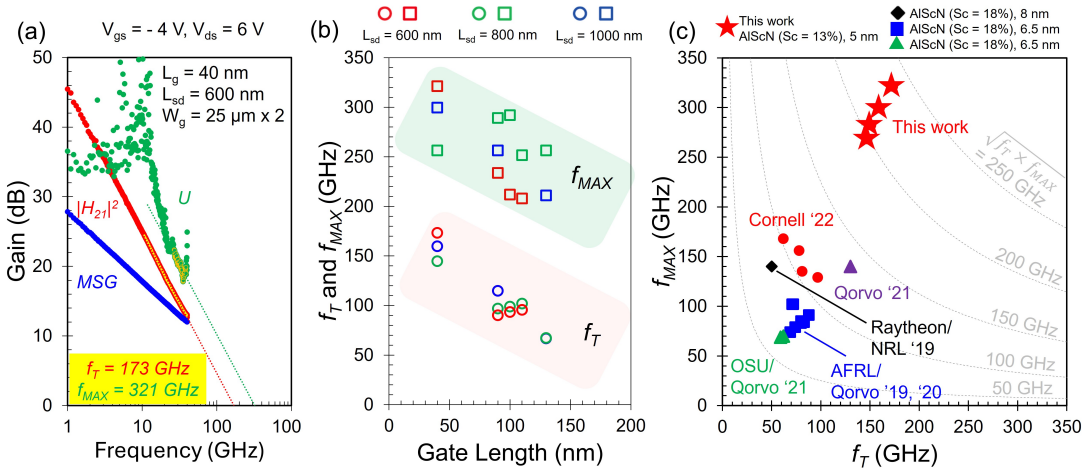
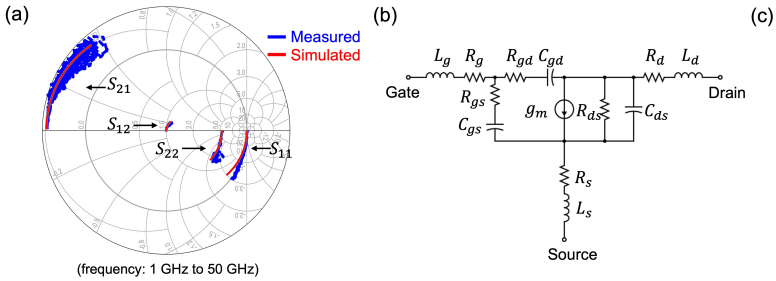


Fig. 6. (a) Measured cutoff frequencies at L_g = 40 nm of the AlScN/GaN HEMT in this work, showing highest f_T/f_{MAX} values of 173/321 GHz. (b) Scaling output of f_T and f_{MAX} with L_g, showing $f_T > 80$ GHz and $f_{MAX} > 210$ GHz for T-gate devices with $L_g \leq 130$ nm. (c) Speed benchmark of AlScN HEMTs with previous reports [4], [8], [9], [11], [13] showing a $\sim$ 2X increase in the f_{MAX} in ultrascaled strain-balanced AlScN HEMTs.



(c)

L_g	30 pH	R_g	1.9 Ω
L_d	3 pH	R_d	4.4 Ω
L_s	2 pH	R_s	3.6 Ω
R_{gd}	9 Ω	C_{gd}	8 fF
R_{gs}	9 Ω	C_{gs}	9 fF
R_{ds}	247 Ω	C_{ds}	2.6 fF
g_m	0.4 S/mm		
Simulated f_T 174 GHz		Simulated f_{MAX} 318 GHz	

Fig. 7. (a) Comparison between measured and simulated S parameters of the HEMT in Fig. 6(a). (b) Small signal equivalent circuit of a HEMT. (c) Small signal equivalent circuit elements of the HEMT in Fig. 6(a) under $V_{GS} = -4$ V and $V_{DS} = 6$ V.