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Low p-contact resistance InGaN-capped AlGaN-based DUV LEDs on bulk AlN substrates

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ABSTRACT

Better wall plug efficiency of deep-ultraviolet light emitting diodes (DUV-LEDs) requires simultaneous low resistivity p-type and n-type contacts, which is a challenging problem. In this study, the co-optimization of p-InGaN and n-AlGaN contacts for DUV LEDs is investigated. We find that using a thin $In_{0.07}Ga_{0.93}N$ cap is effective in achieving ohmic p-contacts with specific contact resistivity of 3.10×10^{-5} Ω cm^2. Upon monolithic integration of p- and n-contacts for DUV LEDs, we find that the high-temperature annealing of 800 °C required for the formation of low resistance contacts to n-AlGaN severely degrades the p-InGaN layer, thereby reducing the hole concentration and increasing the specific contact resistivity to 9.72×10^{-4} Ω cm^2. Depositing a SiO_2 cap by plasma-enhanced atomic layer deposition (PE-ALD) prior to high-temperature n-contact annealing restores the low p-contact resistivity, enabling simultaneous low-resistance p- and n-contacts. DUV-LEDs emitting at 268 nm fabricated with the SiO_2 capping technique exhibit a 3.5 V reduction in operating voltage at a current level of 400 A/cm^2 and a decrease in differential ON-resistance from 6.4 to 4.5 m Ω cm^2. This study highlights a scalable route to high-performance, high-Al-content bipolar AlGaN devices.

AlGaN-based light-emitting diodes (LEDs) in the UVC range (200–280 nm) are promising for applications in disinfection, sensing, and UV communications,[1,2] offering compact, mercury-free alternatives to traditional UV sources. However, their wall plug efficiency (WPE) remains below 15%,[2] far from the ∼30% required to compete with mercury lamps. A key limitation is the difficulty of forming low-resistance ohmic contacts to high-Al-content $Al_xGa_{1-x}N$ ($x > 0.7$),[3] where both n- and p-type contacts suffer from intrinsic material challenges. As the Al composition increases, the electron affinity of AlGaN decreases from 3.18 eV for GaN to 1.01 eV for AlN, and suitable low work function metals are limited, necessitating very high Si doping and annealing temperatures > 800 °C to achieve low-resistance n-contacts.[4–6] Similarly, p-contacts to $Al_xGa_{1-x}N$ ($x > 0.4$) suffer from large contact resistances due to the high ionization energy of Mg acceptors and the scarcity of large work function metals.[7,8]

Despite numerous efforts on achieving good ohmic contact on both p-GaN and n-AlGaN surfaces, the operating voltages of DUV LEDs and high Al composition AlGaN p-n diodes remain high.[9,10] One of the critical problems lies in the large difference between the annealing temperatures required for ohmic contact formation on p-GaN and n-AlGaN surfaces.[10] The challenge in maintaining simultaneous low contact resistance for both p-type and n-type contacts during the monolithic integration of DUV LEDs and laser diodes on a single wafer leads to elevated operating voltages, increased Joule heating, and degraded device performance, particularly at high current densities.[11]

In this study, we reduce the operating voltage of the DUV LED by first showing that employing a p-InGaN capping layer on p-GaN exhibits ohmic contact behavior and reduces the p-contact specific contact resistivity by approximately three orders of magnitude compared to p-GaN alone. We next observe that the >800 °C anneal

required for low-resistance n-contacts in LED fabrication severely degrades the p-InGaN layer, increasing the specific contact resistivity by over an order of magnitude. To address this, we introduce a thin SiO_2 cap on p-InGaN before n-contact annealing, preserving low p-contact resistance along with a low n-contact resistance as well. This work is helpful in reducing the operating voltage and series resistance of high-Al-content AlGaN-based bipolar devices.

Two structures were fabricated to evaluate the effect of lowering the p-type contact resistance using a p-InGaN capping layer. The samples used in this study were grown using a nitrogen plasma-assisted Veeco Gen10 molecular beam epitaxy (MBE) system on +c-plane single-crystal bulk AlN substrates. Sample A consisted of a 300 nm thick AlN buffer layer and a 28 nm thick Mg-doped GaN. Sample B had an identical structure, with the addition of a 7 nm thick Mg-doped $In_{0.07}Ga_{0.93}N$ cap. The sample schematics are shown in Fig. 1(a). The two samples first underwent standard solvent cleaning (acetone and isopropanol) followed by lithographic patterning using nLOF 2020 and exposure with a 200 DSW i-line wafer stepper. Native oxide removal was performed using HCl:DI and buffered oxide etch (BOE), each for 15 s, followed by nitrogen drying. Finally, p-type metal–semiconductor contacts were formed via electron-beam evaporation of Ni/Au (15/20 nm) and rapid thermal annealing (RTA) at 450 °C for 30 s in an O_2 atmosphere.

To study the effects of the p-InGaN capping layer, the specific contact resistivity and sheet resistance were characterized via the circular transmission line method (CTLM). The CTLM I–V measurements are shown in Fig. 1(b). The TLM patterns had an inner contact radius of 20 μm and spacings from 1 to 20 μm. The contact of sample A exhibits a nonlinear I–V characteristic, while that of sample B exhibits a linear I–V characteristic.

Figure 1(c) shows the specific contact resistivity vs current, extracted using $R = dV/dI$. At the current level of 0.1 mA, sample A exhibited a specific contact resistivity of $\rho_c = 1.15 \times 10^{-1}$ Ω cm^2 and sheet resistance of $R_{sheet} = 91.9$ kΩ/□. In contrast, sample B yielded a significantly lower specific contact resistivity of $\rho_c = 3.10 \times 10^{-5}$ Ω cm^2 and sheet resistance of $R_{sheet} = 24.2$ kΩ/□. The contact resistance of sample B is $R_c = 8.4$ Ω mm, comparable to the highest quality p-type InGaN contacts reported in the literature.[12–14] Notably, the specific contact resistivity of sample B is reduced by over three orders of magnitude relative to sample A.

This substantial ρ_c reduction can be explained by the simulated energy band diagrams. These diagrams for samples A and B were computed using the self-consistent Schrödinger–Poisson solver, 1D Poisson,[15] and are presented in Figs. 1(d) and 1(e), respectively. In the simulation, nickel was used as the Schottky contact metal, with the theoretical barrier height $q\phi_b$ calculated as

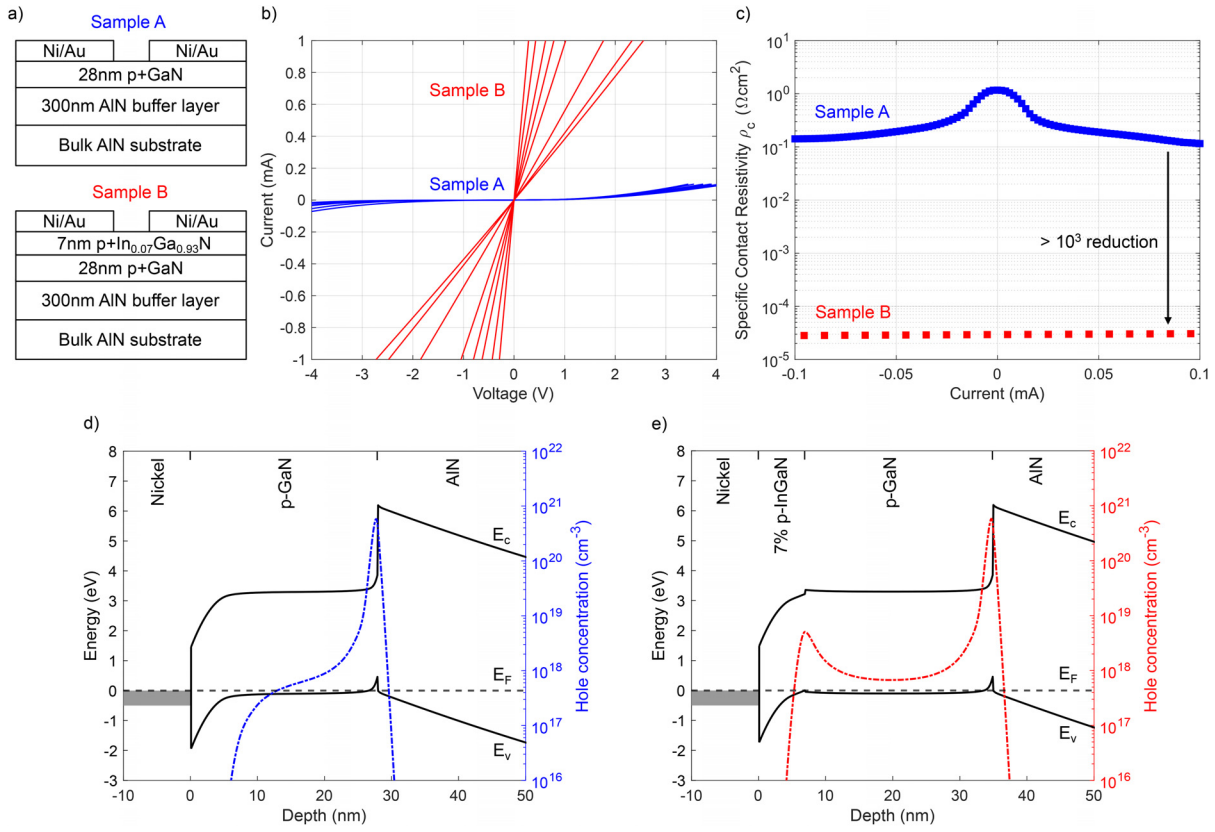

FIG. 1. (a) Schematic of the p-GaN contact samples without (sample A) and with (sample B) a p-InGaN cap. (b) CTLM I–V curves from the two samples. (c) Specific contact resistivity vs current level for the data shown in (b). The contact resistance of sample B is $R_c = 8.4$ Ω mm. (d)–(e) Energy band diagram simulations of sample A and sample B, respectively.

$$q\phi_b = E_g - q(\phi_m - \chi_s),$$

where the work function of Ni is $q\phi_m = 5.25$ eV,[8] the bandgaps are $E_g = 3.4$ eV for GaN[16] and 3.11 eV for $In_{0.07}Ga_{0.93}N$,[16] and the electron affinities are $\chi_s = 3.8$ eV[17] for GaN and $\chi_s = 3.86$ eV for $In_{0.07}Ga_{0.93}N$,[17] the latter obtained by linear interpolation using Vegard's law. For both samples, a uniform Mg doping concentration of $5 \times 10^{19}/cm^3$ was assumed in the p-GaN and p-InGaN layers. The activation energy of Mg acceptors was taken as ~180 meV for p-GaN[18] and ~140 meV for p-$In_{0.07}Ga_{0.93}N$.[18] Deep in the AlN buffer and bulk layer, E_C-E_F is pinned at 0.66 eV due to oxygen impurity,[19] where oxygen concentration levels of $\sim 3 \times 10^{17}/cm^3$ was previously observed in our MBE-grown samples.[20]

A comparison of the energy band diagrams shows that employing the p-InGaN cap lowers the Schottky barrier height by 0.23 eV, allowing for enhanced thermionic emission of holes through the barrier. According to the thermionic emission (TE) and thermionic field emission model (TFE),[21] lowering the Schottky barrier by 0.23 eV can provide three orders of reduction in the specific contact resistivity in p-GaN. Furthermore, the energy band diagrams show a narrowing of the tunneling barrier width in sample B. This is attributed to two key mechanisms: (1) the higher obtained hole concentration in the p-InGaN cap and (2) the strain-induced piezoelectric and spontaneous polarization fields that lead to band bending and result in a peak in the hole distribution at the p-InGaN/pGaN interface. Together, these mechanisms contribute to the significant reduction in ρ_c observed with the use of a p-InGaN cap.

The hole concentration within the p-type layers in samples A and B can be estimated from the measured sheet resistance using the relation $R_{sheet} = (qp\mu t)^{-1}$, where q is the elementary charge 1.6×10^{-19} C, p is the free hole concentration, μ is the hole mobility, and t is the effective thickness of the conducting layer. Using the measured sheet resistances of $R_{sheet} = 91.9$ and 24.2 kΩ/□ for samples A and B, respectively, layer thickness of $t_{pGaN} = 28$ nm for sample A and $t_{pInGaN/pGaN} = 7 + 28$ nm for sample B (accounting for parallel conduction through both layers), and assuming a hole mobility of $\mu = 10\ cm^2V^{-1}s^{-1}$,[22] the estimated hole concentrations are $p = 2.43 \times 10^{18}/cm^3$ for sample A and $7.38 \times 10^{18}/cm^3$ for sample B. These estimated hole concentrations are higher than those induced by Mg-doping alone, which can be potentially ascribed to the two-dimensional hole gas (2DHG) at the InGaN/GaN and the GaN/AlN interface as predicted by the energy band diagram simulations.[23,24]

From a materials perspective, achieving hole concentrations exceeding $10^{18}/cm^3$ is more feasible with p-InGaN than p-GaN.[25] First, Mg incorporation in the InGaN alloy is significantly higher than in GaN. Lee *et al.* in Ref. 26 reported that Mg-doped $In_{0.16}Ga_{0.84}N$ incorporates 30 × more Mg than GaN at the same growth temperature. Second, the high activation energy (~ 180 meV) of Mg acceptors in GaN strongly limits the free hole concentration at room temperature, with only 1%–5% of incorporated Mg contributing to free carriers.[22,27] Increasing the indium content in InGaN reduces this activation energy,[25] further boosting the hole concentration to above $10^{18}/cm^3$ and reducing ρ_c. It is worth noting that specific contact resistivities as low as $\rho_c \sim 10^{-4}$–10^{-5} Ω cm² have been reported for p-GaN contacts.[28–30] Achieving such low ρ_c in sample A would require optimizing the epitaxial growth and contact fabrication processes. In contrast, the incorporation of a p-InGaN capping layer offers a more direct and effective approach to reducing ρ_c.

We next investigate the monolithic integration of p-InGaN and n-AlGaN contacts in the DUV LED process. Specifically, we examine the impact of the high-temperature anneal required for low-resistance n-AlGaN contacts on the integrity and performance of the p-InGaN layer. Figure 2(a) shows the schematic of the DUV LED structure, which was grown on a 2-in. bulk AlN substrate by MBE. The heterostructure was grown along the [0001] crystal direction and consists of a 500 nm AlN nucleation layer, a 400 nm n-$Al_{0.76}Ga_{0.24}N$ with donor doping of [Si]~ $1 \times 10^{19}/cm^3$, a 50 nm $Al_{0.66}Ga_{0.34}N$ UID waveguiding layer, a 9 nm $Al_{0.53}Ga_{0.47}N$ single quantum well, a 70 nm $Al_{0.66}Ga_{0.34}N$ UID waveguiding layer, a 300 nm distributed polarization doped (DPD) AlGaN layer graded from AlN to $Al_{0.65}Ga_{0.35}N$ along the growth direction capable of providing $\sim 5.7 \times 10^{17}/cm^3$ mobile hole density without any impurity doping,[9] and a Mg-doped contact layer with 10 nm p-GaN and capped with a 7 nm p-$In_{0.05}Ga_{0.95}N$ layer. We prepared three samples of the size $1 \times 1\ cm^2$, all of which were diced from the same 2-in. wafer. The LED devices were fabricated by first exposing the n-cladding layer surface by inductively coupled plasma

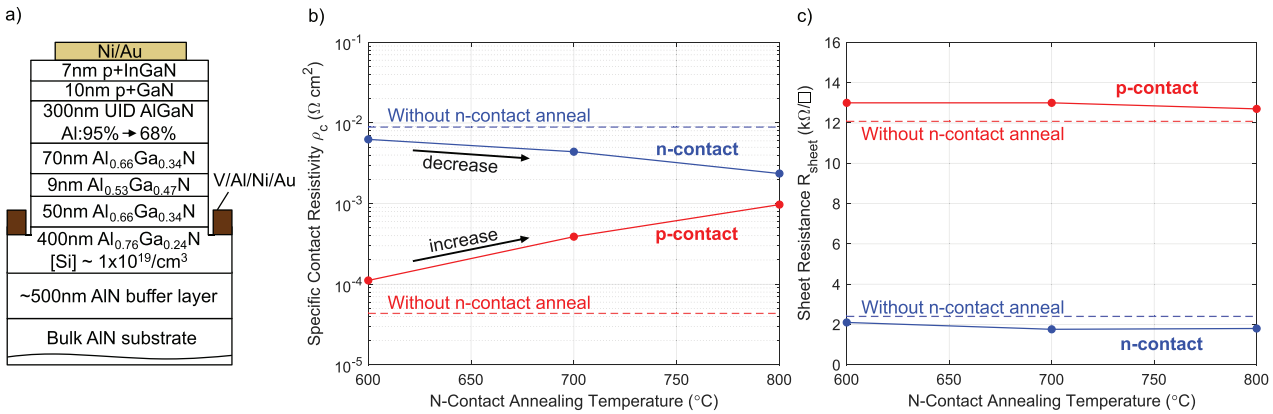

FIG. 2. (a) Heterostructure of the DUV LED samples used for this contact annealing-temperature-dependent study. (b) Specific contact resistivity of n- and p-contact vs n-contact annealing temperature. P-contacts were subsequently annealed at 450 °C. All resistance values were extracted at 1 mA from the CTLM I–V measurement. (c) Sheet resistance vs n-contact annealing temperature.

reactive ion etching (ICP-RIE) ~50 nm into the n$Al_{0.76}Ga_{0.24}N$ layer. Next, n-electrode metal stack V/Al/Ni/Au with thicknesses 20/80/40/100 nm was deposited using electron-beam evaporation. The three samples were annealed for 30 s in N_2 ambient at different temperatures: 600, 700, and 800 °C. Identical p-contact Ni/Au metal stack with 15/20 nm thicknesses were subsequently deposited on the three samples on the p-$In_{0.05}Ga_{0.95}N$ surface and annealed for 30 s at 450 °C in O_2 ambient.

CTLM structures were fabricated on the p-InGaN surface and the etched n-AlGaN surfaces of the three samples. The specific contact resistivity of both n- and p-type contacts as a function of n-contact annealing temperature is shown in Fig. 2(b), with all values extracted at the current level of 1 mA. Horizontal lines mark ρ_c without n-contact anneal.

For the n-contact, high annealing temperatures of 600–800 °C are required to lower ρ_c, consistent with reports for high-composition-Al n-AlGaN contacts.[4] Several studies in the literature have suggested that during the annealing of V/Al-based metal contacts with n-AlGaN, nitrogen is extracted from the semiconductor, forming a thin crystalline AlN at the metal–semiconductor interface from Al in the electrode stack.[31,32] Nitrogen vacancies act as donor states, increasing carrier concentration at the interface[4] and enhancing tunneling through the thin space charge region, thus reducing contact resistance. For high-Al composition AlGaN, studies have shown that higher annealing temperatures are required to drive the metal–nAlGaN reaction needed for low-resistance ohmic contacts,[4,31,33] which agrees with the trend in the contact resistance data presented in Fig. 2(b). The specific contact resistivity of our reported n-type contacts are higher than values reported in the literature, where $\rho_c \leq 5 \times 10^{-4}$ Ω cm^2 has been achieved for n$Al_xGa_{1-x}N$ ($x > 0.7$).[4,6] We attribute the elevated ρ_c in our devices to several possible factors: (1) surface damage and roughening caused by high-power RIE, and (2) the use of native AlN substrates rather than foreign sapphire substrates. While AlN substrates offer advantages such as lower threading dislocation and point defect densities,[34] this reduced defect density may limit the effectiveness of defect-assisted tunneling mechanisms that otherwise help reduce ρ_c in devices grown on sapphire.[35] Further reduction in ρ_c may be achieved by increasing the Si doping concentration from 1×10^{19}/cm^3 to 3×10^{19}/cm^3, which is predicted to lower ρ_c to the $\sim 10^{-5}$ Ω cm^2 range for $Al_{0.75}Ga_{0.25}N$ based on TFE model calculations. Additional strategies reported in the literature include surface treatment[36,37] and the incorporation of an intermediate interfacial layer.[6]

In contrast to the n-type contacts, the specific contact resistivity of the p-type contacts increases with higher n-contact annealing temperatures. The lowest p-contact $\rho_c = 4.37 \times 10^{-5}$ Ω cm^2 was observed in the sample that did not undergo n-contact annealing. As the n-contact annealing temperature increased from no anneal to 800 °C, the p-contact rose super-linearly to 9.72×10^{-4} Ω cm^2, as shown in Fig. 2(b). We attribute this degradation to thermal decomposition and nitrogen desorption from the p-InGaN surface—mechanisms previously reported for p-GaN contacts.[10] This process forms a high concentration of nitrogen vacancy defects near the sample surface that acts as compensating donors in the p-type layer,[38] thereby reducing the hole concentration and increasing ρ_c.

These findings highlight a critical trade-off in monolithic DUV LED integration: while high-temperature annealing improves the n-contact resistivity, it simultaneously degrades the p-contact. To maintain low p-contact resistivity, the n-contact annealing temperature should ideally remain below 800 °C; however, this constraint may limit the performance of the n-contact. Similar p-GaN degradation has been reported,[10,26] which the authors mitigated by separately optimizing p- and n-contact anneals to minimize series resistance.

Additional insight can be drawn from the sheet resistance trends shown in Fig. 2(c). While the p-contact sheet resistance increases from 12.17 kΩ/□ at no n-contact anneal to 13.1 kΩ/□ at 600 °C, it remains relatively constant up to 800 °C. This suggests that the temperature-induced degradation is localized primarily at the metal–semiconductor interface, rather than in the bulk of the p-InGaN layer. In contrast, the sheet resistance of the n-type contact decreases slightly with increasing annealing temperature, consistent with improved ohmic contact formation.

To mitigate thermal degradation and nitrogen evaporation of p-InGaN during high-temperature n-contact anneal, we deposited a 50 nm SiO_2 cap by PE-ALD, inspired by Ref. 39, which showed that SiO_2 suppresses Mg out-diffusion during RTA of Mg-doped GaN. The full LED fabrication sequence incorporating the SiO_2 cap is shown in Fig. 3. To evaluate the effectiveness of this technique, TLM measurements were performed on three p-contact samples: one without n-contact annealing, one with 800 °C n-contact annealing without the SiO_2 cap, and one with the SiO_2 cap during the anneal. The results,

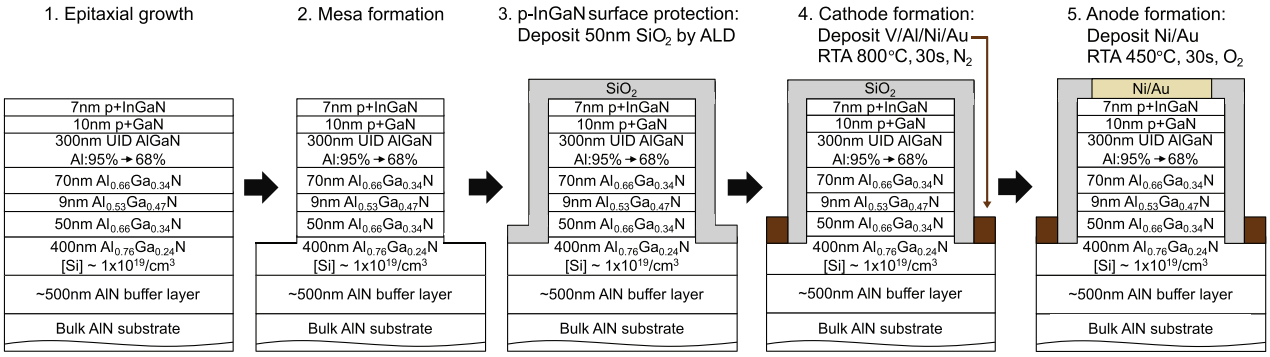

FIG. 3. Schematic diagram illustrating the fabrication process of an LED with the SiO_2 capping technique. (a) Epitaxial growth. (b) Mesa formation by ICP-RIE. (c) Deposition of SiO_2 by ALD. (d) Deposition and annealing of n-type metal contacts. (e) Deposition and annealing of p-type metal contacts.

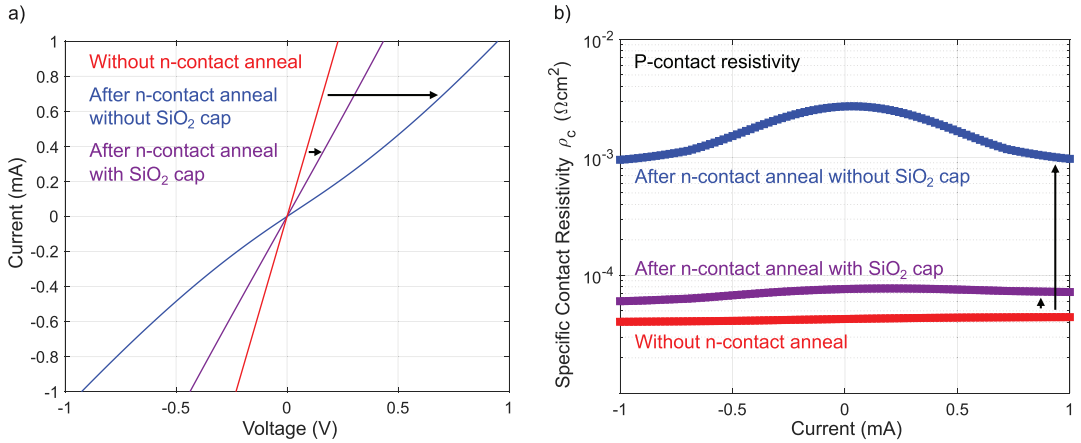

FIG. 4. (a) CTLM I–V curve comparison of p-contact without undergoing n-contact anneal, after undergoing n-contact anneal with SiO_2 cap, and after undergoing n-contact anneal without SiO_2 cap. IVs are plotted for 2 μm spacing. (b) Specific contact resistivity vs current level for the data shown in (a).

shown in Figs. 4(a) and 4(b), indicate that the specific contact resistivity of the p-contact was significantly reduced from 9.72×10^{-4} Ω cm^2 without the cap to 6.76×10^{-5} Ω cm^2 with the cap, nearly restoring it to the value of 4.37×10^{-5} Ω cm^2 observed in the un-annealed reference sample.

In addition to lowering the p-contact resistance, the SiO_2 capping technique exhibited spatial uniformity across the sample. A 1×1 cm^2 sample was partitioned into four regions, each containing a central CTLM structure. The average p-contact ρ_c across the four dies was 6.93×10^{-5} Ω cm^2 $\pm$ 0.38×10^{-5} Ω cm^2, indicating excellent uniformity and consistency. This method provides an effective strategy for mitigating thermal degradation of p-InGaN contacts. While academic journals seldom detail it explicitly, using dielectric (SiO_2, SiN_x) or epitaxial cap layers (GaN, AlN) to protect device epilayer prior to contact deposition is a standard but under-reported processing step.[40,41] However, there is currently no report of utilizing a dielectric capping layer to intentionally mitigate degradation of p-contacts in the DUV LED community.

Two DUV LED samples were fabricated from the same epitaxial wafer, with a heterostructure similar to that shown in Fig. 3. One sample used the SiO_2 capping technique and the other did not. Diodes were tested randomly from each sample, and Fig. 5(a) compares the room-temperature J–V characteristics of the best-performing diode from each group—selected based on the lowest ON-resistance at 10 V. At 400 A/cm^2, the SiO_2-capped diode showed reduced forward voltage to 15.2 V compared to 19.0 V for the uncapped diode, and lower ON-resistance of 4.5 vs 6.4 m Ω cm^2. Batch testing, as shown in Fig. 5(b), confirmed improved performance. SiO_2-capped diodes averaged $J_{10V} = 1.21 \pm 0.54$ A/cm^2, while uncapped devices averaged $J_{10V} = 0.34 \pm 0.22$ A/cm^2. The variation within each group is attributed to fabrication non-uniformities. Most devices showed leakage current between 10^{-7} and 10^{-5} A/cm^2 at –10 V.

Electroluminescence (EL) spectra, collected from the backside of an LED with SiO_2 capping at room temperature, is shown in Fig. 5(c). The spectra exhibit a DUV emission peak centered at 268 nm. The secondary peak centered at 247 nm likely originates from carrier recombination in the cladding layers. More investigation will be performed in the future. These results collectively demonstrate that SiO_2 capping enhances AlGaN DUV LED performance by lowering series resistance and operating voltage.

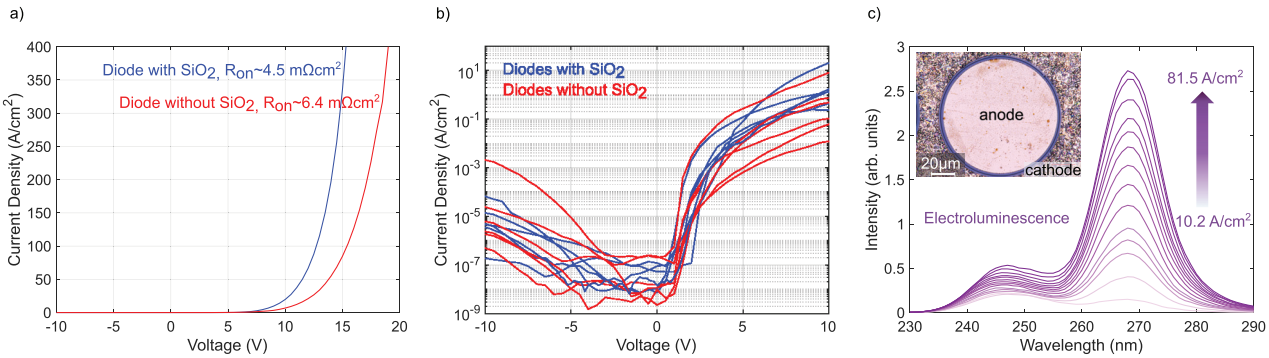

FIG. 5. (a) Room-temperature J–V characteristics of two LEDs, one with SiO_2 capping method and one without. The differential ON-resistance was extracted at 400 A/cm^2. (b) I–V from batch test of LEDs with and without SiO_2 capping. (c) Room-temperature electroluminescence of an LED with the SiO_2 capping method. Inset shows the microscopy image of a fabricated LED.

In this work, we demonstrated that a p-InGaN capping layer enables low-resistance p-type contacts for AlGaN-based DUV LEDs on bulk AlN, reducing the specific contact resistivity to 3.10×10^{-5} Ω cm^2—three orders lower than p-GaN alone—due to reduced Schottky barrier height, lower Mg activation energy, and polarization-induced band bending. However, high-temperature annealing for n-contacts degrades p-contact performance. Implementing a SiO_2 cap preserved the InGaN surface, recovering the specific contact resistivity to 6.76×10^{-5} Ω cm^2. LEDs fabricated with this method showed reduced operating voltage and ON-resistance, alongside DUV emission at 268 nm. This work offers a practical approach for optimizing the electrical performance of AlGaN-based DUV LEDs and provides insights into the co-optimization of p- and n-type contacts in device fabrication.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Hsin-Wei S. Huang and Shivali Agrawal contributed equally to this work.

Hsin-Wei S. Huang: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (equal); Methodology (equal); Software (equal); Visualization (lead); Writing – original draft (lead); Writing – review & editing (equal). **Shivali Agrawal:** Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (equal); Methodology (equal); Visualization (supporting); Writing – original draft (supporting); Writing – review & editing (supporting). **Debaditya Bhattacharya:** Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **Vladimir Protasenko:** Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **Huili Grace Xing:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **Debdeep Jena:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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