

Thermal Characterization and Design of AlN/GaN/AlN HEMTs on Foreign Substrates

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Abstract—AlN/GaN/AlN high electron mobility transistors (HEMTs) offer enhanced carrier confinement and higher breakdown voltage than conventional AlGaIn/GaN HEMTs. In this work, Raman thermometry was used to characterize the self-heating behavior of a single-finger AlN/GaN/AlN HEMT on 6H-SiC. A 3D finite element analysis model was created to optimize the thermal design of the device structure. Simulation results reveal that the optimal buffer layer thicknesses to minimize the channel temperature rise of AlN/GaN/AlN HEMTs on 6H-SiC and diamond substrates are $\sim 2 \mu\text{m}$ and $\sim 0.7 \mu\text{m}$, respectively. Moreover, diamond substrate integration further enhances the thermal performance, achieving a $\sim 45\%$ and $\sim 53\%$ reduction in the device thermal resistance as compared to those of an AlN/GaN/AlN HEMT on 6H-SiC and an AlGaIn/GaN HEMT on 4H-SiC, respectively.

Index Terms—Electrothermal effects, HEMTs, Raman spectroscopy, thermal management of electronics, thermoreflectance, wide bandgap semiconductor devices.

I. INTRODUCTION

GALLIUM NITRIDE (GaN)-based high electron mobility transistors (HEMTs) have attracted considerable attention in high-power/frequency 5G wireless communication and military radar applications [1]. However, conventional AlGaIn/GaN HEMTs are encountering challenges in maintaining optimal RF performance at high frequencies, particularly

Received 24 January 2025; accepted 3 March 2025. Date of publication 6 March 2025; date of current version 29 April 2025. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) Technologies for Heat Removal in Electronics at the Device Scale (THREADS) Program under Grant HR0011-23-C-0135 and in part by the Army Research Office under Award W911NF2220191. The review of this letter was arranged by Editor J. Joh. (*Corresponding author: Sukwon Choi.*)

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Digital Object Identifier 10.1109/LED.2025.3548853

in the millimeter-wave range (30–300 GHz). The degradation in RF performance is caused by short-channel effects that stem from inadequate confinement of electrons in the two-dimensional electron gas (2-DEG), leading to less effective gate modulation of the channel [2]. InGaN back barriers [3], AlGaIn back barriers [4], and N-polar HEMTs [5] have been implemented to address this challenge. However, limitations associated with the maximum output power and device self-heating remain due to the relatively low energy bandgap (E_g) and thermal conductivity (κ) of InGaN and AlGaIn, respectively [6].

A novel AlN/GaN/AlN HEMT platform has been proposed to address these challenges [7]. This platform employs a strained GaN quantum well sandwiched between AlN barrier and buffer layers, where the large E_g difference ($E_{g,\text{AlN}} \sim 6.2 \text{ eV}$ vs. $E_{g,\text{GaN}} \sim 3.4 \text{ eV}$) ensures effective electron confinement, while the larger polarization discontinuity induces a higher 2-DEG density near the AlN barrier/GaN channel interface [8]. In addition, the ultra-wide E_g of the AlN barrier and buffer layers improves the breakdown field [7] and reduces the leakage current [9], respectively.

Although extensive research has been conducted to demonstrate the improved electrical performance of AlN/GaN/AlN HEMTs [10], the improvement in thermal performance has yet to be investigated. Bulk AlN possesses a high κ of $\sim 320 \text{ W/(m}\cdot\text{K)}$ [11] at room temperature, while the κ of a $\sim 2 \mu\text{m}$ GaN buffer is reported to be $\sim 160 \text{ W/(m}\cdot\text{K)}$ [12]. This work compares the self-heating behavior of an AlN/GaN/AlN HEMT and a conventional AlGaIn/GaN HEMT using micro-Raman thermometry. Time-domain thermoreflectance (TDTR) was used to characterize the thermal properties of the AlN/GaN/AlN on 6H-SiC material stack. A device thermal model was created to identify critical design considerations that are necessary to maximize the thermal performance of AlN/GaN/AlN HEMTs on foreign substrates.

II. DEVICE DESCRIPTION

A single-finger AlN/GaN/AlN HEMT was fabricated on a 6H-SiC substrate as described in the cross-sectional schematic in Fig. 1(a). Plasma-assisted molecular beam epitaxy and migration enhanced epitaxy were used to grow the quantum well heterostructure. Details of the fabrication process can be

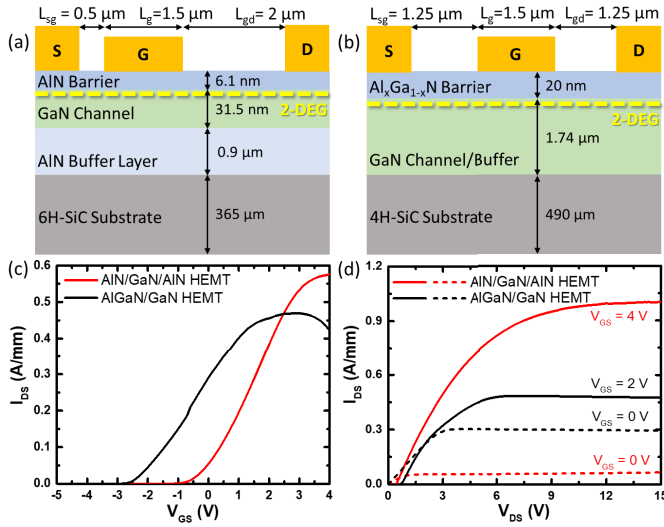


Fig. 1. Cross-sectional schematic of (a) the AIN/GaN/AIN HEMT and (b) AlGaIn/GaN HEMT. Both devices have a gate width of $50 \mu\text{m}$. (c) Electrical transfer and (d) output characteristics of both devices.

found in [13]. For comparison, a conventional AlGaIn/GaN HEMT was fabricated on a 4H-SiC substrate using a commercial epitaxial wafer, as depicted in Fig. 1(b). Fig. 1(c) and (d) show the electrical transfer (at $V_{\text{DS}} = 5 \text{ V}$) and output characteristics of both devices.

III. DEVICE THERMOGRAPHY

The device buffer layer and surface temperatures were measured using micro-Raman thermometry under power density conditions of 2–14 W/mm. A fully open channel condition that results in a relatively uniform Joule heat distribution across the channel, was analyzed for both devices. This means V_{GS} was kept at 4 V for the AIN/GaN/AIN HEMT and 2 V for the AlGaIn/GaN HEMT (refer to the transfer characteristics in Fig. 1(c)). The through-thickness temperature rise (ΔT) of the AIN and GaN buffer layers was determined based on the line broadening of the $E_2(\text{high})$ phonon mode of the AIN and GaN. Further details of the line width based Raman thermometry procedure are available in [14]. The device surface temperature above the drain-side corner of the gate was measured by monitoring the phonon frequency shift of anatase TiO_2 nanoparticles transferred onto the devices. Details of the nanoparticle-assisted Raman thermometry method can be found in [15]. As shown in Fig. 2(a), the through thickness average ΔT of the buffer layer of the AIN/GaN/AIN HEMT is marginally lower than that of the AlGaIn/GaN HEMT. On the other hand, as shown in Fig. 2(b), the surface temperature of the AIN/GaN/AIN HEMT is up to $\sim 12\%$ lower than that of the AlGaIn/GaN HEMT. It should be noted that the surface temperature results provide a reasonable estimation of the channel (2-DEG) temperatures [16] and [17].

IV. THERMAL PROPERTY MEASUREMENT AND MODELING

TDTR measurement results in Figs. 3(a) and (b) show that the in-plane (κ_{in} , across the c-plane) and cross-plane direction (κ_{out} , along the c-axis) κ of the $0.9 \mu\text{m}$ thick AIN buffer

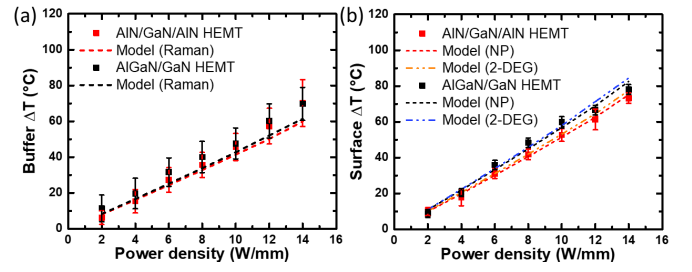


Fig. 2. Measured and simulated ΔT of (a) the buffer layer and (b) the surface (which represents the channel ΔT) of the AIN/GaN/AIN HEMT and AlGaIn/GaN HEMTs.

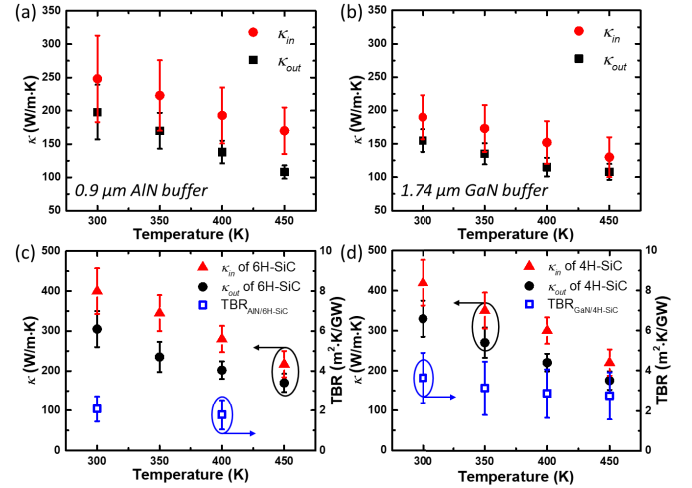


Fig. 3. The anisotropic κ of (a) the AIN and (b) GaN layers. (c) The anisotropic κ of the 6H-SiC substrate and the TBR at the AIN/6H-SiC interface. (d) The anisotropic κ of the 4H-SiC substrate and the TBR at the GaN/4H-SiC interface.

layer are higher than that of the $1.74 \mu\text{m}$ thick GaN buffer. This renders the AIN/GaN/AIN HEMT to possess a lower channel-to-substrate thermal resistance (R_{th}) than that of the AlGaIn/GaN HEMT despite the κ of the 6H-SiC substrate is slightly lower than that of 4H-SiC in both directions (Figs. 3(c) and (d)). The higher effective thermal boundary resistance (TBR) at the GaN/4H-SiC interface than that of the AIN/6H-SiC interface (Figs. 3(c) and (d)) contributes to the observations in Fig. 2 (i.e., similar average buffer temperatures but distinct surface temperatures). Details of the TDTR setup and measurement procedure can be found in [16] and [18]. The measured κ values show good agreement with data available in the literature [19], [20], [21], [22], [23].

A 3D finite element analysis (FEA) device thermal model that adopts the measured thermal properties was built using COMSOL Multiphysics to validate the experimental results and conduct thermal design optimization studies. The thermal conductivity of the 31.5 nm thick GaN channel layer was assumed to be 18.5 W/(m-K) [12]. The TBR at the GaN channel/AIN buffer interface ($\sim 2 \text{ m}^2\text{K/GW}$) was adopted from [18]. To mimic operation under a fully-open channel condition, a uniform heat generation profile across the channel was assumed [17]. A thermal interface material (Bergquist TGP 1500R) and wafer chuck below the device die were modeled to match the experimental setup. The bottom of the wafer chuck

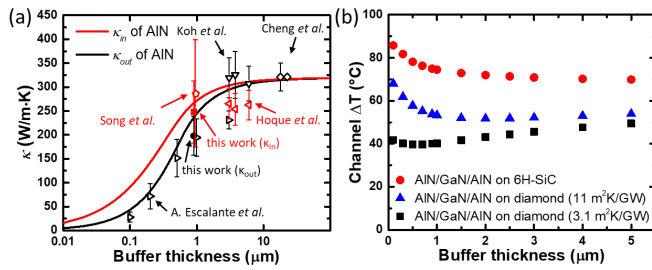


Fig. 4. (a) The calculated thickness-dependent anisotropic κ of AlN thin films compared to data reported in literature. Experimentally determined κ_{in} , and κ_{out} values were adopted from [11], [19], [23], [25], [26]. (b) The peak channel ΔT of AlN/GaN/AlN HEMTs on 6H-SiC and diamond substrates as a function the buffer layer thickness at a power density of 14 W/mm.

was set at room temperature (25 °C), while all other surfaces were subjected to natural convection ($h = 5 \text{ W}/(\text{m}^2\text{K})$). The temperatures measured by Raman thermometry were modeled via 3D average domain probes with a radius of 1 μm spanning through the GaN channel/buffer for the AlGaIn/GaN HEMT and AlN buffer layer for the AlN/GaN/AlN HEMT (Fig. 2(a)). Experimental and modeling results agree within error bar ranges.

V. THERMAL DESIGN

The results in Fig. 2 indicate that design optimization of the AlN/GaN/AlN HEMT structure is necessary to maximize its thermal performance. When the film thickness is below the mean free path (MFP) of acoustic phonons tasked for heat conduction, the κ is reduced by phonon-boundary scattering. An analytical solution for the thickness-dependent κ of thin films was derived using the phonon Boltzmann transport equation with a gray approximation [24]. Fig. 4(a) illustrates the calculated κ_{in} and κ_{out} of AlN using this model when adopting an effective MFP of $\sim 0.7 \mu\text{m}$, which contributes to 70% of the bulk κ of AlN [20]. The modeling results show good agreement with experimental data reported in Fig. 3(a) and in literature [11], [19], [23], [25], [26]. Based on this κ model, 3D FEA device thermal simulations presented in Fig. 4(b) indicate that increasing the AlN buffer thickness from 0.9 μm to $\sim 2 \mu\text{m}$ (on 6H-SiC) reduces the channel ΔT by $\sim 4\%$. Increasing the AlN buffer thickness from 2 to 5 μm results in a $\sim 2\%$ further improvement at 14 W/mm. For these simulations the temperature-dependence of the κ of AlN films of different thicknesses was not accounted for because no experimental data is available in literature.

To understand the impact of the substrate material on the device self-heating, models for AlN/GaN/AlN HEMTs on 4H-SiC (not shown in Fig. 4 (b)) and single crystal diamond (Fig. 4 (b)) were created. The substrate thicknesses were assumed to be identical to that of 6H-SiC (365 μm). An AlN/4H-SiC TBR of 2.1 m²K/GW (sample in [23] measured by TDTR) and AlN/diamond TBRs of 11 m²K/GW [27] and 3.1 m²K/GW [28] were adopted. Replacing the 6H-SiC substrate with 4H-SiC (assuming a 2 μm thick AlN buffer) results in a 5.6% reduction in the channel ΔT at 14 W/mm. As shown in Fig. 4(b), a high thermal conductivity [29] diamond substrate effectively reduces the channel temperature.

For example, the model exhibits a $\sim 45\%$ reduction in the channel ΔT compared to the AlN/GaN/AlN (2 μm) HEMT on 6H-SiC when the buffer layer thickness is 0.7 μm (optimal thickness for a TBR_{AlN/diamond} of 3.1 m²K/GW). Under this limiting case, the GaN channel, channel/buffer TBR, AlN buffer, buffer/substrate TBR, and diamond substrate contribute to 7.7%, 9.5%, 31.6%, 26.5%, and 24.7% of the R_{th} , respectively. As a final note, Fig. 4(b) shows that the optimal thickness of the AlN buffer layer depends on the underlying thermal resistance components.

VI. CONCLUSION

The thermal performance of an AlN/GaN/AlN HEMT on 6H-SiC was investigated using micro-Raman thermometry and a 3D FEA thermal model that adopts thermal properties measured by TDTR was created. Results demonstrate that, although AlN exhibits higher thermal conductivity than GaN, the cooling effectiveness can be limited if the AlN buffer layer thickness is not carefully designed. Increasing the thickness of the AlN buffer layer up to 2 μm (on a 6H-SiC substrate) effectively helps reducing the channel ΔT . Integration of an AlN/GaN/AlN (0.7 μm) HEMT with a single crystal diamond substrate results in a $\sim 45\%$ reduction in the channel ΔT compared to that of a device on a 6H-SiC substrate. The findings of this work will assist the electro-thermal co-design of next-generation AlN/GaN/AlN HEMTs that offer optimal RF performance under high power and frequency operation.

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