



# Dielectric assisted liftoff enabled simultaneous low n- and p- differential contact resistivities in ultrawide bandgap AlGa<sub>0.25</sub>N pn diodes on bulk AlN

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Ultrawide bandgap (UWBG) semiconductor pn junction diodes are desired for high voltage power electronics and UV optoelectronic devices. Making low-resistance contacts to the UWBG junction region is difficult due to low solubility of dopants in AlGa<sub>0.25</sub>N, nonavailability of readily available metals with suitable work functions, processing induced damage and the lack of dislocations in single-crystal bulk AlN substrates. We report dielectric assisted liftoff, a processing scheme to simultaneously achieve n- and p-contacts with low turn-on voltages ( $v_{on}$ ), and low specific differential contact resistances ( $\rho_c$ ) in heterostructure diodes on bulk AlN. We report  $\rho_c^n = 5\text{--}6 \times 10^{-5} \Omega\text{cm}^2$  and  $v_{on}^n \approx 0$  V to etched n-type Al<sub>0.75</sub>Ga<sub>0.25</sub>N for current densities between 0 and 5 kA cm<sup>-2</sup>. We also report  $\rho_c^p \approx 10^{-3}\text{--}10^{-5} \Omega\text{cm}^2$  and  $v_{on}^p \approx 0\text{--}0.01$  V to p-In<sub>0.07</sub>Ga<sub>0.93</sub>N contacts over the same current range. The key design principle in fabrication of the diodes is to avoid exposing the nitride semiconductor surfaces to photoresist by using a dielectric layer, which also simultaneously protects the p-InGa<sub>0.93</sub>N during the n-contact annealing step.

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## 1. Introduction

Technologically relevant ultrawide bandgap (UWBG) semiconductors with energy gaps of  $\sim 5\text{--}6$  eV are diamond,  $\alpha\text{-Ga}_2\text{O}_3$ , and high Al-content AlGa<sub>0.25</sub>N and AlN<sup>1</sup>. Al(Ga)N is the only one among these three with a direct bandgap and unique polarization fields for n- and p-doping<sup>2</sup> which enables both unipolar and bipolar epitaxial heterostructure devices. This unique advantage for AlGa<sub>0.25</sub>N enables the development of ultrawide bandgap pn junctions. AlN today is electrically too insulating to allow for low resistance n-type or p-type contacts. n-type conductivity is achieved in Al<sub>0.7</sub>Ga<sub>0.3</sub>N, by Si donor doping.<sup>3</sup> However, acceptor doping of this high Al concentration AlGa<sub>0.25</sub>N has not yielded high p-type conductivity yet.

At a sharp GaN/AlN heterojunction, a 2D hole gas (2DHG) forms without acceptor dopants due to polarization.<sup>4</sup> Compositionally graded junctions spread this 2DHG into a 3D hole gas,<sup>2</sup> a technique referred to as distributed polarization doping (DPD). In a p-up heterostructure, the 3D hole gas creates the bridge for vertical injection of holes into the UWBG junction region at the bottom, sourced from the low-resistance metal/p-InGa<sub>0.93</sub>N/GaN layer on the top. The DPD injection layer thus enables low-resistance contacts to holes in the valence band of the UWBG AlGa<sub>0.25</sub>N (or AlN) junction active region of the pn junction diode.

DPD has been successfully employed in metal-organic chemical vapor deposition<sup>5,6</sup> and molecular beam epitaxy (MBE)<sup>7,8</sup> pn diodes realized on bulk AlN substrates. For power electronics<sup>9</sup>, ultraviolet (UV) lasers<sup>10</sup> and light emitting diodes (LEDs),<sup>7,8</sup> lowering of n- and p-type contact resistivities result in lower undesired losses, thereby boosting desirable device metrics. Because the common substrates for UWBG AlGa<sub>0.25</sub>N—sapphire and bulk AlN—are electrically insulating, the n-type contact requires metal deposition on an etched surface and

high-temperature annealing.<sup>11–21</sup> Dislocations assist formation of low resistance contacts.<sup>22</sup> Because bulk AlN substrates have  $\sim 10^4$  cm<sup>-2</sup> dislocations compared to AlN templates on sapphire that have  $\sim 10^9$  cm<sup>-2</sup>, contacts on bulk AlN substrates is problematic. Simultaneously achieving low n-type and p-type contact resistivities in a repeatable fashion has proven problematic due to limited chemical control of surfaces which are exacerbated by high temperature annealing.<sup>23</sup> Further, a study of metal-first processing for UWBG  $\beta\text{-Ga}_2\text{O}_3$  diodes<sup>24,25</sup> and a study of metal-first contacts to n-AlGa<sub>0.25</sub>N<sup>26</sup> revealed that mitigating carbon contaminants introduced during photoresist processing enables low resistance and linear contacts.

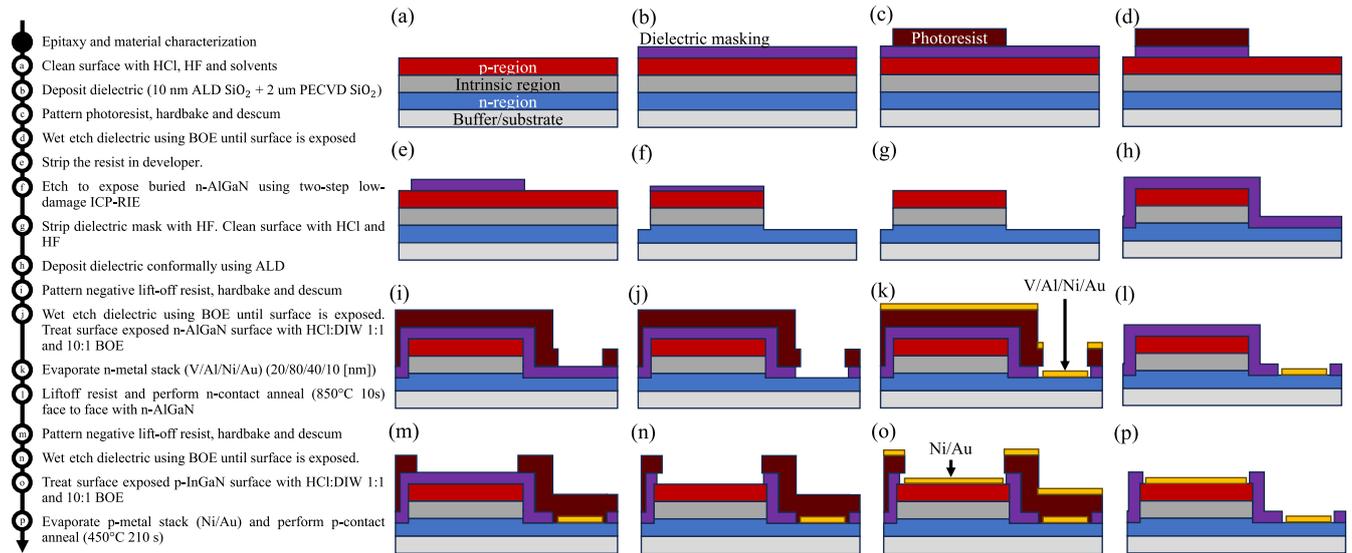
In this work we present dielectric assisted liftoff (DALi), a method using dielectric masking that eliminates these problems to enable simultaneous low-resistivity n- and p-type contacts.

## 2. Methods

### 2.1. Design and epitaxy

Plasma assisted MBE was used to grow an epitaxial diode structure on a 2 inch bulk AlN crystal wafer from Crystal IS using growth conditions reported elsewhere.<sup>7,8</sup> The n-region of the structure is a 400 nm thick buried n-type Al<sub>0.75</sub>Ga<sub>0.25</sub>N layer doped with  $8 \times 10^{19}$  cm<sup>-3</sup> Si as measured by secondary ion mass spectrometry (SIMS). The intrinsic region on top of the n-region was designed as an LED with a single 9 nm unintentionally doped (UID) Al<sub>0.55</sub>Ga<sub>0.45</sub>N quantum well embedded inside a 120 nm thick UID Al<sub>0.65</sub>Ga<sub>0.35</sub>N waveguiding layer. Hall measurements on a calibration sample with 84 nm of n-Al<sub>0.73</sub>Ga<sub>0.27</sub>N on bulk AlN yielded  $n_{3d} = 7.3 \times 10^{19}$  cm<sup>-3</sup>,  $\mu_n = 18.1$  cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and a sheet resistance of  $R_{sh} = 560 \Omega/\square$ . The p-type region consisted of a DPD injection layer graded linearly from AlN to Al<sub>0.65</sub>Ga<sub>0.35</sub>N over 300 nm, followed by 10 nm of p-GaN and 5 nm of p-In<sub>0.07</sub>Ga<sub>0.93</sub>N. The targeted Mg





**Fig. 1.** Process flow for the fabrication of the quasi-vertical structure based on the dielectric assisted liftoff (DALi) fabrication scheme. This scheme ensures that photoresist is never in contact with the semiconductor surface, both during the n-contact expose etch step, where the dielectric is used as the etch mask, and during the metallization steps.

concentration in the pGaN and the p-InGaIn film is  $\sim 5 \times 10^{19} \text{ cm}^{-3}$ . The 2 inch wafer was diced into square coupon sized pieces prior to fabrication.

**2.2. Nanofabrication and the dielectric assisted liftoff (DALi) process**

Figure 1 shows the detailed fabrication process which we now describe in steps. The sample was first dipped in HCl and HF for 1 min each, followed by an organic solvent clean to obtain a clean semiconductor surface as depicted in Fig. 1(a). Figure 1(b) shows the dielectric masking by plasma enhanced atomic layer deposition (PEALD) of a 10 nm protective SiO<sub>2</sub> layer on the top p-InGaIn surface followed by plasma enhanced chemical vapor deposition of 2 μm of SiO<sub>2</sub>. This SiO<sub>2</sub> was then patterned with positive photoresist which was subsequently hardbaked for 5 min at 115 °C. We then wet etch the SiO<sub>2</sub> in 10:1 buffered oxide etchant (BOE) to expose the surface as shown in Figs. 1(c) and 1(d).

The photoresist was then removed with organic solvents as shown in Fig. 1(e). The patterned SiO<sub>2</sub> was used as the hard mask during the next etch step to expose the n-AlGaIn as shown in Fig. 1(f). The etch was performed in a two step process. The first step etches 450 nm into the structure to expose the n-AlGaIn layer using a high power Cl<sub>2</sub>/BCl<sub>3</sub>/Ar based inductively coupled plasma reactive ion etching (ICP-RIE). Then 2 min of a BCl<sub>3</sub> based low-power ICP-RIE etch was used to further etch 10 nm of the exposed n-AlGaIn surface to remove surface damage. Post etching, we removed the remaining dielectric mask by using HF and then cleaned the etched surface with HCl and HF as shown in Fig. 1(g).

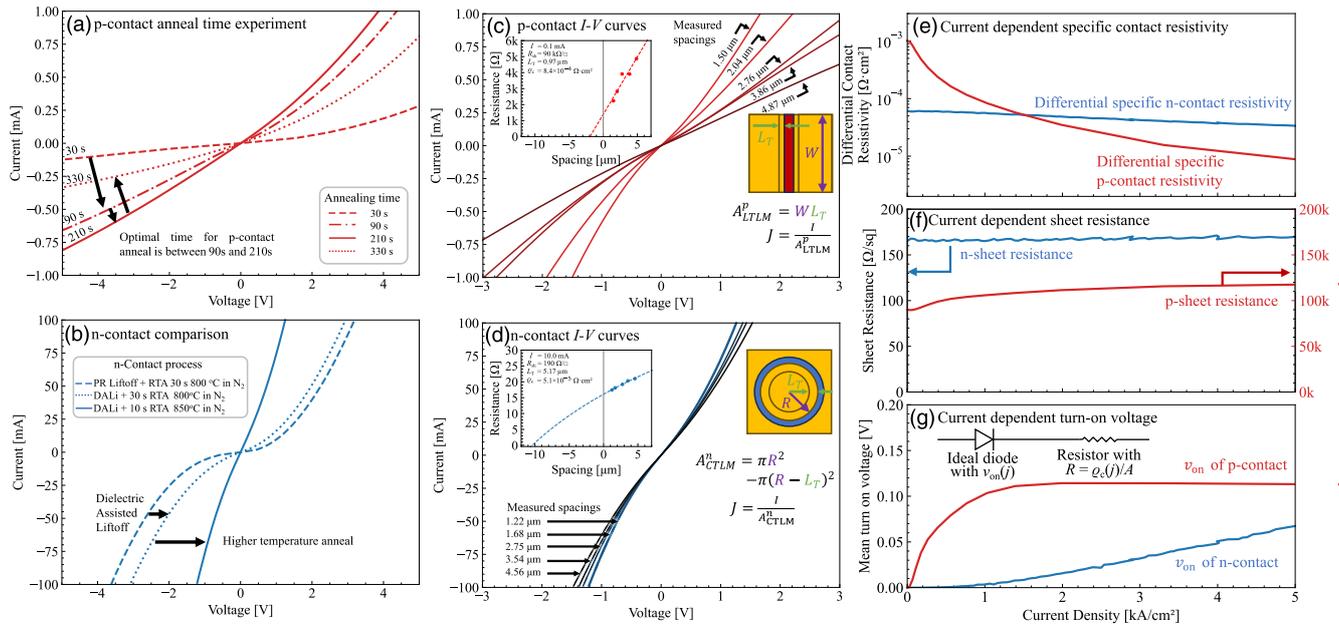
We now describe the DALi method. This is a pseudo metal-first process which allows us to perform lift-off metallization while preventing the semiconductor surface from being exposed to photoresist. PEALD is used to deposit 50 nm of SiO<sub>2</sub> conformally over the sample as seen in Fig. 1(h). We then pattern the n-electrode using negative lift-off resist which we hardbake for 5 min at 115 °C. Subsequently, we expose the semiconductor surface with a short BOE dip, followed by treating the exposed area with

1:1 HCl:DI water for 15 s, and then by another BOE dip to get rid of any oxides formed by the HCl treatment. This process is visualized in Figs. 1(i) and 1(j). Next, we proceed to deposit the n-contact stack V/Al/Ni/Au (20/80/40/10 nm) using e-beam evaporation and perform lift-off as seen in Figs. 1(k) and 1(l). This process flow ensures that the photoresist does not come in direct contact with the semiconductor surface, preventing contamination from the photoresist. Post lift-off we proceed to perform the n-contact rapid thermal anneal in an N<sub>2</sub> ambient at a temperature of 850 °C for 10 s. The remaining SiO<sub>2</sub> from the DALi process still covering the p-InGaIn protects the p-InGaIn during the high temperature n-anneal.<sup>23)</sup>

Following the n-contact anneal, we repeat the DALi method for the p-contact and then deposit the Ni/Au (15/20 nm) electrodes as visualized in Figs. 1(m), 1(n), 1(o) and 1(p). We perform a p-contact anneal in an O<sub>2</sub> ambient at 450 °C for 210 s. This concludes the fabrication of the electrodes.

The p-annealing condition described above was identified in a separate experiment which will now be described. A sample consisting of 10 nm of p-GaN and a 5 nm p-InGaIn cap was grown on bulk AlN. The sample underwent the DALi fabrication to deposit Ni/Au contacts. Post fabrication, the sample was diced into multiple pieces which underwent different durations of annealing at 450 °C. Figure 2(a) shows the I-V curves from 5 μm spacing circular transfer length method (TLM) pads. For 450 °C in O<sub>2</sub> ambient annealing, we observe that the current flowing through the contact increases for 30–210 s annealing times, and then decreases for 210–330 s annealing times. The optimal Ni/Au contacts are achieved for an annealing time of 210 s.

To understand the effectiveness of the DALi process, a separate control piece from the LED wafer was fabricated using the traditional lift-off technique with an n-contact anneal at 800 °C for 30 s. Figure 2(b) shows that the DALi process reduces the Schottky like behavior of the contacts on n-AlGaIn compared to traditional negative-lift-off procedure. By annealing at 850 °C,<sup>27)</sup> but for a shorter duration of 10 s, we are able to further reduce the n-contact resistance. The



**Fig. 2.** (a)  $I$ - $V$ s of 5  $\mu\text{m}$  spaced CTLM pads which helped us identify the best contact annealing duration for the p-contacts. (b)  $I$ - $V$ s of 5  $\mu\text{m}$  depicting the n-contact process comparing standard liftoff photolithography and DALi annealed at two different temperatures. (c)  $I$ - $V$ s and measured LTLM spacings for the p-contact on a fully fabricated pn junction diode sample as described by the procedure in Fig. 1. The inset figure shows an example LTLM fit at  $I = 0.1$  mA. The inset diagram shows a schematic of the LTLM pattern along with a calculation showing how the current density was calculated. (d)  $I$ - $V$ s and measured CTLM spacings for the n-contact from the same sample as part (c). The inset figure shows a schematic of the CTLM pattern along with a calculation showing how the current density was calculated. (e) The current dependent specific differential resistivity. (f) The extracted sheet resistance of the n-layer and p-layers. (g) A mean turn-on voltage of the contacts calculated by averaging the  $x$ -axis intercepts of the iso-current tangents to TLM  $I$ - $V$ s. For ideal linear ohmic contacts, the mean turn-on voltage of contacts is 0 V. The inset shows an equivalent circuit diagram of the contact which is modeled as an ideal diode and a resistor in series.

above experiments helped us identify improved process parameters for the DALi fabrication process.

### 2.3. Transfer length method analysis

To use the TLM for the contacts, the electrode spacings were measured with an optical microscope, and  $I$ - $V$  curves were measured in the Kelvin 4-probe configuration. Figures 2(c) and 2(d) show the measured  $I$ - $V$  curves for various TLM electrode spacings. For fitting the p-type linear TLM (LTLM) data, we use the relation

$$R_T = \frac{R_{sh}}{W}(d + 2L_T), \quad (1)$$

where  $R_T$  is the total resistance,  $R_{sh}$  is the sheet resistance,  $W$  is the width of the LTLM pad,  $d$  is the contact spacing and  $L_T$  is the transfer length. For fitting of the n-type circular TLM (CTLM) data, the relation

$$R_T = \frac{R_{sh}}{2\pi} \left[ \ln\left(\frac{r_o}{r_i}\right) + \frac{L_T}{r_i} \frac{I_0\left(\frac{r_i}{L_T}\right)}{I_1\left(\frac{r_i}{L_T}\right)} + \frac{L_T}{r_o} \frac{K_0\left(\frac{r_o}{L_T}\right)}{K_1\left(\frac{r_o}{L_T}\right)} \right] \quad (2)$$

was used.<sup>28)</sup> Here,  $R_{sh}$  is the sheet resistance of the material,  $r_i$  is the inner radius of the CTLM pad, where  $r_o = r_i + d$  is the outer radius of the TLM pad,  $L_T$  is the transfer length.  $I_0$  and  $I_1$  are the zeroth and first order Bessel functions of the first kind and  $K_0$  and  $K_1$  are the zeroth and first order Bessel functions of the second kind.

The standard TLM analysis<sup>28)</sup> for extracting specific contact resistivity  $\rho_c$  assumes linear  $I$ - $V$  curves, and that  $\rho_c$  is independent of the current  $I$ . The dynamic resistance of a device is often a metric of interest and proper knowledge of origins of this resistance is insightful for device engineers. For contacts with nonlinear  $I$ - $V$ s the standard extraction is

strictly only valid at  $I = 0$ . Therefore TLMs with nonlinear but repeatable  $I$ - $V$ s must account for a current dependent differential contact resistivity  $\rho_c(I)$  and a current dependent turn-on voltage  $v_{on}(I)$ . Here we introduce a different notation for differential specific contact resistivity,  $\rho_c$ , to distinguish it from the specific contact resistivity  $\rho_c$ . Because the contacts in Figs. 2(c) and 2(d) are nonlinear, we model each contact as an ideal diode with a current dependent turn-on voltage  $v_{on}(I)$  and a current dependent resistor  $\rho_c(I)/A$  (where  $A$  is the area of the contact) in series. Contacts with simultaneously low  $v_{on}(I)$  and  $\rho_c(I)$  are desired. We now describe the procedure to extract the differential contact resistivity  $\rho_c(I)$  and contact turn-on voltage  $v_{on}(I)$ .

Using Eqs. (1) and (2) with  $\mathcal{R}_T = dV(I)/dI$  from Figs. 2(c) and 2(d) for various TLM spacings at iso-currents, we extract  $R_{sh}$  and  $L_T$ . Here we introduce new notation  $\mathcal{R}_T$  to indicate differential resistance. Combining the two parameters we obtain the differential contact resistance as  $\rho_c = R_{sh}L_T^2$ .<sup>28)</sup> The inset figures of Figs. 2(c) and 2(d) are example iso-current fits of the p-LTLM and n-CTLMs at 0.1 mA and 10 mA respectively.

The tangent to a TLM  $I$ - $V$  curve has a slope of  $1/\mathcal{R}_T$  and the  $x$ -intercept of this tangent,  $V(I) - I \cdot dV(I)/dI$ , is the effective turn-on voltage. The mean turn-on voltage,

$$v_{on}(I) = \left\langle V(I) - I \frac{dV(I)}{dI} \right\rangle_{\text{TLMs}, d=0} \quad (3)$$

is taken as the mean value of the effective turn-on voltages across different TLM pads. This process is repeated at every current to obtain current dependent values of  $R_{sh}(I)$ ,  $L_T(I)$ ,  $\rho(I)$  and  $v_{on}(I)$ .

**Table I.** Summary of differential contact resistivity  $\rho_c(j_c)$ , sheet resistance  $R_{sh}(j_c)$  and mean turn-on voltage  $v_{on}(j_c)$  as extracted from the TLM analysis. A column of applications where the information about contact performance can be of importance is also included.

$j_c$ (A cm <sup>-2</sup> )	Type	$\rho_c(j)$ ( $\Omega$ cm <sup>2</sup> )	$R_{sh}$ ( $\Omega/\square$ )	$v_{on}$ (V)	Applications
0	n	$6.1 \times 10^{-5}$	165	0.000	Transistors below saturation or in sub-threshold
	p	$1.0 \times 10^{-3}$	90 k	0.000	
100	n	$6.0 \times 10^{-5}$	167	0.000	LEDs, power diodes, transistors in saturation
	p	$6.6 \times 10^{-4}$	91 k	0.022	
1000	n	$5.8 \times 10^{-5}$	166	0.001	Laser diodes, power diodes, power transistors
	p	$8.3 \times 10^{-5}$	106 k	0.103	

To estimate the current density at the contacts  $j_c(I) = I/A_{TLM}(I)$ , we used the relation  $A_{CTLM}^n(I) = \pi r_i^2 - \pi(r_i - L_T(I))^2$  for CTLMs and  $A_{LTLM}^p(I) = W \times L_T(I)$  for LTLMs. In Figs. 2(e), 2(f) and 2(g) we plot  $\rho_c(I)$ ,  $R_{sh}(I)$  and  $v_{on}(I)$  respectively against the current density  $j_c(I)$ .

By decoupling the turn-on behavior from the contact-resistance, we are able to model the contact as an ideal diode and resistor in series. In practice, this allows us to estimate the voltage drop across a contact as

$$V_c(j_c) = v_{on}(j_c) + j_c \rho_c(j_c) \quad (4)$$

and the power density across the contact as

$$P_c(j_c) = j_c V_c(j_c) = j_c v_{on}(j_c) + j_c^2 \rho_c(j_c), \quad (5)$$

allowing us to decouple contact performance from the diode.

### 3. Results and discussion

Table I summarizes the differential contact resistivity  $\rho_c(j_c)$ , sheet resistance  $R_{sh}(j_c)$  and mean turn-on voltage  $v_{on}(j_c)$  as extracted from the TLM analysis at some specific currents of interest. In particular we identify that the performance of the contacts near  $j_c = 0$  A cm<sup>-2</sup> is of importance for transistors operating in the sub-threshold region or below saturation. Moderate current densities of  $j_c \approx 100$  A cm<sup>-2</sup> is of interest to LED operation and transistors in their active state; whereas high current densities  $j_c > 1$  kA cm<sup>-2</sup> is relevant to lasers, and high power diodes and transistors. The full range of values can be read off Figs. 2(e), 2(f) and 2(g).

As seen in Fig. 2(e),  $\rho_c^p$  of the p-contact starts out high at  $\sim 10^{-3}$   $\Omega$  cm<sup>2</sup> at  $j = 0$  kA cm<sup>-2</sup> but it decreases to  $\sim 10^{-5}$   $\Omega$  cm<sup>2</sup> at  $j = 5$  kA cm<sup>-2</sup>. The specific differential contact resistance  $\rho_c^n$  of the n-contact is roughly constant at  $\sim 5\text{--}6 \times 10^{-5}$   $\Omega$  cm<sup>2</sup> over this current range.

A relatively constant sheet resistance is indicative of a good contact. Figure 2(f) shows the stability of the n-contact sheet resistance which roughly stays at  $R_{sh}^n \approx 167$   $\Omega/\square$  over a wide range of current densities. The sheet resistance of the p-contact is high, roughly staying in the range  $R_{sh}^p \approx 90\text{--}110$  k $\Omega/\square$ .

In Fig. 2(g) we plot the mean turn on voltage for the contacts. A low turn-on near 0 V is a sign of ohmic-like behavior of the contacts. Specifically, for our result, the n-contacts are almost linear between 0 kA cm<sup>-2</sup> and 1 kA cm<sup>-2</sup> because of the near zero turn-on voltage. The p-contact however shows significant turn-on behavior which saturates to  $v_{on}^p \approx 0.1$  V at higher current densities.

We benchmark and compare our n-contact against other reports of contacts to etched n-AlGaIn in Table II alongside variations in different fabrication techniques used. Contact

resistivities reported vary from  $6.6 \times 10^{-1}$   $\Omega$  cm<sup>2</sup> to  $2 \times 10^{-6}$   $\Omega$  cm<sup>2</sup> for compositions ranging from 50% to 95% Al composition in AlGaIn. It is important to note that there is variability in the TLM analysis method used across different papers which makes comparison challenging, particularly for the case of nonlinear  $I$ -Vs. Notably this work is one of the lowest reported n-contact differential resistivity to etched n-Al<sub>0.75</sub>Ga<sub>0.25</sub>N surface on bulk AlN substrates.

The observed low contact resistances are attributed to a combination of several factors. First, it is likely a result of high-quality material growth, which benefited from the incorporation of increased Si doping in the n-AlGaIn film.<sup>3</sup> Second, the use of a low-damage etching technique played a critical role in maintaining the integrity of the interface.<sup>13</sup> Third, the implementation of an adapted metal-first processing approach to prevent carbon contamination<sup>24,25</sup> further improved the contact performance. Fourth, surface treatment using HCl and HF/BOE effectively removed contaminants, creating a clean and well-prepared interface prior to metallization. Finally, co-development of both contacts, specifically the protection of the p-type layers during the high temperature n-contact anneal resulted in simultaneously low p-contact resistivities.

In Fig. 3(a) we show the measured log-scale  $I$ - $V$  characteristic of a diode fabricated with the DALi fabrication scheme. Figure 3(b) shows the  $I$ - $V$  characteristics in the linear scale. The diode shows low reverse leakage and an on-off ratio of 5 orders at  $\pm 7$  V. The linear plot indicates a diode turn-on voltage of  $\sim 4$  V. The inset of Fig. 3(b) shows the electroluminescence spectrum when the diode is biased at 4 A cm<sup>-2</sup> with a measured drop of 15 V, demonstrating that the device operates as a deep-UV LED with a peak emission wavelength of 258 nm ( $\sim 4.8$  eV). Despite the improved contacts, the diode's forward current density remains low. The origin of this discrepancy is speculated to be the high oxygen content of  $\sim 3 \times 10^{18}$  cm<sup>-3</sup> as measured by SIMS in the MBE grown DPD AlGaIn layers in these samples. Oxygen in the nitrogen sites ( $O_N$ ) is expected to be a deep level donor in high composition AlGaIn<sup>31</sup> which partially compensates the 3D hole gas in the p-DPD injection layer. This increases the p-DPD layer resistance, which prevents our diodes from achieving higher on currents, but does not impact the n-AlGaIn and the p-InGaIn contact resistances supported by Fig. 2. We believe this problem is addressable in the near future with modified growth conditions of the active region, while retaining the low resistance p- and n-type contacts obtained by the DALi process.

### 4. Conclusion

To conclude, we developed a fabrication process which includes a two-step etch, surface treatments, a novel pseudo

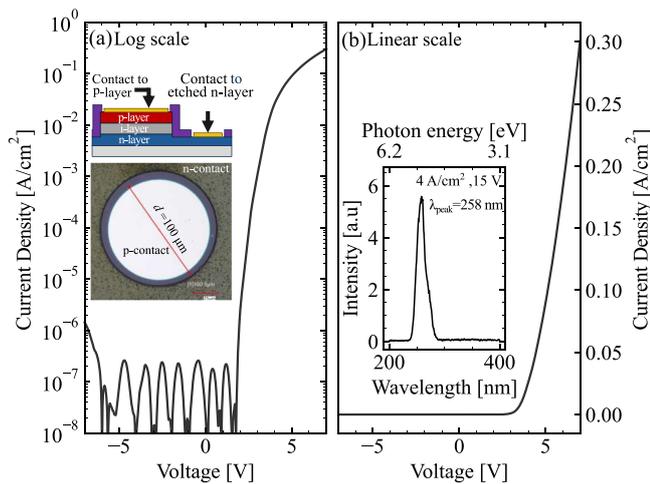
**Table II.** Literature survey of contacts to etched n-AlGaIn surfaces.<sup>5,12–19,29,30</sup> NR stands for not reported.

Institution	Year	Substrate	Growth method	Al comp [%]	[Si]/ $n$ [ $\text{cm}^{-3}$ ]	n-AlGaIn thickness [nm]	Etching method	Etch depth into AlGaIn [nm]	Surface treatment before metallization	Metal stack	Thicknesses [nm]	Contact method	Contact resistivity [ $\Omega \cdot \text{cm}^2$ ]	$R_{\text{sh}}$ [ $\Omega/\square$ ]	TLM analysis method
This work Cornell University	2025	AlN	MBE	75	[Si]: $8.0 \times 10^{19}$	400	ICP RIE: $\text{Cl}_2$ / $\text{BCl}_3/\text{Ar} + \text{BCl}_3$	50	DALi + HCl + BOE	V/Al/Ni/Au	20/80/40/10	DALi + RTA 850 °C 10 s	$5.8 \times 10^{-5}$	166	iso-current extraction at 1 kA $\text{cm}^{-2}$
Peking University	2025	Sapphire	MOCVD	70	$n$ : $1.5 \times 10^{19}$	1400	ICP RIE: $\text{Cl}_2/\text{BCl}_3/\text{Ar}$	200	HCl	V/Al/Ni/Au	15/90/20/40	Lift-off + RTA 850 °C	$1.2 \times 10^{-4}$	NR	NR
KAUST	2025	Sapphire	MOVPE	85	[Si]: $5.0 \times 10^{18}$	200	ALE: $\text{Cl}_2$	10	$\text{H}_2\text{SO}_4:\text{H}_3\text{PO}_4$ + BOE	Ti/Al/Ti	20/120/80	Lift-off + RTA 950 °C 90 s	$2.0 \times 10^{-5}$	421000	NR
Peking University	2024	Sapphire	MOCVD	60	$n$ : $1.5 \times 10^{19}$	1300	ICP RIE	200	HCl	V/Al/Ni/Cr/Au	15/90/20/20/40	Lift-off + RTA 850 °C 35 s	$5.3 \times 10^{-4}$	NR	NR
Nanjing University	2024	Sapphire	MOVPE	50	$n$ : $2.0 \times 10^{19}$	2000	ICP RIE: $\text{Cl}_2/\text{BCl}_3/\text{Ar}$	215	KOH/ $\text{SiN}_x$ sacrificial	V/Al/Ni/Au	15/140/30/60	Lift-off + RTA 900 °C 60 s	$9.3 \times 10^{-4}$	NR	NR
Nagoya University	2024	AlN	MOVPE	70	[Si]: $1.0 \times 10^{19}$	300	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	TMAH	V/Al/Ni/Au	NR	Lift-off + RTA 750 °C 120 s	$2.0 \times 10^{-6}$	470	iso-voltage extraction at 7.5 V
FBH Berlin	2023	Sapphire	MOVPE	87	NR	1200	ICP RIE: $\text{Cl}_2/\text{BCl}_3/\text{Ar}$	200	$\text{SF}_6$ Plasma	V/Al/Ni/Au	15/120/20/30	Lift-off + RTA 850 °C 30 s	$6.6 \times 10^{-1}$	NR	iso-current extraction at 1 mA
Cornell University	2022	AlN	MBE	90	[Si]: $6.0 \times 10^{19}$	750	ICP RIE: $\text{Cl}_2/\text{Ar}$	450	HCl + BOE	V/Al/Ni/Au	NR	Lift-off + RTA 850 °C 300 s	$2.6 \times 10^{-2}$	32000	iso-current extraction at 10 mA
Peking University	2021	Sapphire	MOCVD	50	$n$ : $2.5 \times 10^{18}$	1500	ICP RIE: $\text{Cl}_2/\text{BCl}_3/\text{Ar}$	200	Short PECVD $\text{SiN}_x$ deposition	Ti/Al/Ni/Au	30/180/50/100	Lift-off + RTA 850 °C 35 s	$1.3 \times 10^{-4}$	NR	NR
TU Berlin	2020	Sapphire	MOVPE	75	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 850 °C 30 s	$4.0 \times 10^{-4}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$
TU Berlin	2020	Sapphire	MOVPE	80	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 800 °C 30 s	$1.0 \times 10^{-3}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$

Continued on next page.

Table II. Continued.

Institution	Year	Substrate	Growth method	Al comp [%]	[Si]/ $n$ [ $\text{cm}^{-3}$ ]	n-AlGaIn thickness [nm]	Etching method	Etch depth into AlGaIn [nm]	Surface treatment before metallization	Metal stack	Thicknesses [nm]	Contact method	Contact resistivity [ $\Omega \cdot \text{cm}^2$ ]	$R_{\text{sh}}$ [ $\Omega/\square$ ]	TLM analysis method
TU Berlin	2020	Sapphire	MOVPE	85	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 800 °C 30 s	$2.0 \times 10^{-3}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$
TU Berlin	2020	Sapphire	MOVPE	87.5	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 800 °C 30 s	$1.0 \times 10^{-3}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$
TU Berlin	2020	Sapphire	MOVPE	90	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 800 °C 30 s	$2.0 \times 10^{-3}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$
TU Berlin	2020	Sapphire	MOVPE	95	[Si]: $\sim 10^{18}$	1200	ICP RIE: $\text{Cl}_2/\text{Ar}$	NR	NR	V/Al/Ni/Au	14/90/20/30	Lift-off + RTA 800 °C 30 s	$4.0 \times 10^{-3}$	NR	iso-current extraction at 0.1 kA $\text{cm}^{-2}$
TU Berlin	2020	Sapphire	MOVPE	65	NR	500	ICP RIE: 2 step $\text{Cl}_2/\text{Ar}$	NR	HCl	V/Al/Ni/Au	15/120/20/40	Lift-off + RTA 750 °C 30 s	$3.5 \times 10^{-4}$	NR	NR
University of South Carolina	2009	Sapphire	MOVPE	68	$n: 5.0 \times 10^{18}$	2000	ICP RIE: $\text{Cl}_2/\text{BCl}_3/\text{Ar}$	NR	NR	Ti/Al/Ni/Au	40/120/40/80	Lift-off + RTA 875 °C 15 s	$5.0 \times 10^{-4}$	NR	NR



**Fig. 3.** (a) Log scale  $I$ - $V$  curve from a 100  $\mu\text{m}$  device showing the diode characteristics. The inset shows a schematic of the diode and an optical microscope image of a diode. (b) Linear scale curve of the devices as (a). The inset shows electroluminescence from a diode biased at 4 A  $\text{cm}^{-2}$  with a measured voltage drop of 15 V. The peak electroluminescence wavelength is at 258 nm. No parasitic luminescence is observed in the 200–400 nm wavelength range.

metal-first process called DALi, and optimized annealing temperatures for high Al composition AlGa<sub>N</sub> pn junction diodes. This processing scheme allows us to achieve simultaneous n- and p-contacts with low turn-on voltages, and low specific differential contact resistances of  $\rho_c^n \approx 5\text{--}6 \times 10^{-5} \Omega \text{cm}^2$  and  $v_{\text{on}}^n \approx 0 \text{ V}$  to etched n-type Al<sub>0.75</sub>Ga<sub>0.25</sub>N expressed over a current range of 0–5 kA  $\text{cm}^{-2}$ . For the p-In<sub>0.07</sub>Ga<sub>0.93</sub>N contact, the extracted values range between  $\rho_c^p \approx 10^{-3}\text{--}10^{-5} \Omega \text{cm}^2$  and  $v_{\text{on}}^p \approx 0\text{--}0.01 \text{ V}$  over the same current range.

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- 1) J. Y. Tsao et al., *Adv. Electron. Mater.* **4**, 1600501 (2018).
- 2) J. Simon, V. Protasenko, C. Lian, H. Xing, and D. Jena, *Science* **327**, 60 (2010).
- 3) S. Bharadwaj, S. M. Islam, K. Nomoto, V. Protasenko, A. Chaney, H. G. Xing, and D. Jena, *Appl. Phys. Lett.* **114**, 113501 (2019).
- 4) R. Chaudhuri, S. J. Bader, Z. Chen, D. A. Muller, H. G. Xing, and D. Jena, *Science* **365**, 1454 (2019).
- 5) T. Kumabe, A. Yoshikawa, S. Kawasaki, M. Kushimoto, Y. Honda, M. Arai, J. Suda, and H. Amano, *IEEE Trans. Electron Devices* **71**, 3396 (2024).
- 6) T. Jamil, A. A. M. Mazumder, M. Ali, M. Rahman, K. Stephenson, G. Simin, and A. Khan, *Jpn. J. Appl. Phys.* **64**, 055507 (2025).
- 7) S. Agrawal, L. van Deurzen, J. Encomendero, J. E. Dill, H. Wei (Sheena) Huang, V. Protasenko, H. G. Xing, and D. Jena, *Appl. Phys. Lett.* **124**, 102109 (2024).
- 8) S. Agrawal, H. W. S. Huang, D. Bhattacharya, M. Ramesh, K. Szkudlarek, H. Turski, V. Protasenko, H. G. Xing, and D. Jena, (2025) "Edge emission from 265 nm UV-C LEDs grown by MBE on bulk AlN arXiv:2512.23896.
- 9) M. Ramesh, S. Agrawal, H. G. Xing, and D. Jena, *Phys. Status Solidi A* **2401023** (2025).
- 10) Z. Zhang, M. Kushimoto, T. Sakai, N. Sugiyama, L. J. Schowalter, C. Sasaoka, and H. Amano, *Appl. Phys. Express* **12**, 124003 (2019).
- 11) X. A. Cao, H. Piao, J. Li, J. Y. Lin, and H. X. Jiang, *Phys. Status Solidi A* **204**, 3410 (2007).
- 12) T. Liu, Z. Liu, H. Cao, M. Nong, X. Tang, Z. Jiang, G. I. M. Garcia, K. Ren, and X. Li, *Appl. Phys. Lett.* **126**, 152109 (2025).
- 13) X. Q. Guo et al., *Appl. Phys. Lett.* **126**, 082104 (2025).
- 14) S. Zhou et al., *Semicond. Sci. Technol.* **39**, 065001 (2024).
- 15) H. K. Cho, J. Rass, A. Mogilatenko, K. Kunkel, R. S. Unger, M. Schilling, T. Wernicke, and S. Einfeldt, *IEEE Photonics Technol. Lett.* **35**, 915 (2023).
- 16) N. Zhang et al., *Appl. Phys. Lett.* **118**, 222101 (2021).
- 17) H. K. Cho, J. H. Kang, L. Sulmoni, K. Kunkel, J. Rass, N. Susilo, T. Wernicke, S. Einfeldt, and M. Kneissl, *Semicond. Sci. Technol.* **35**, 095019 (2020).
- 18) X. Q. Guo et al., *Appl. Phys. Lett.* **124**, 232106 (2024).
- 19) L. Sulmoni, F. Mehnke, A. Mogilatenko, M. Guttman, T. Wernicke, and M. Kneissl, *Photonics Res.* **8**, 1381 (2020).
- 20) N. Nagata, T. Senga, M. Iwaya, T. Takeuchi, S. Kamiyama, and I. Akasaki, *Phys. Status Solidi C* **14**, 1600243 (2017).
- 21) M. Miller, B. Koo, K. Bogart, and S. Mohney, *J. Electron. Mater.* **37**, 564 (2008).
- 22) B. B. Haidet, I. Bryan, P. Reddy, Z. Bryan, R. Collazo, and Z. Sitar, *J. Appl. Phys.* **117**, 245702 (2015).
- 23) H. W. S. Huang, S. Agrawal, D. Bhattacharya, V. Protasenko, H. G. Xing, and D. Jena, *Appl. Phys. Lett.* **127**, 193305 (2025).
- 24) K. T. Smith, C. A. Gorsak, J. T. Buontempo, B. J. Cromer, T. Ikenoue, H. Gulupalli, M. O. Thompson, D. Jena, H. P. Nair, and H. G. Xing, *J. Appl. Phys.* **136**, 215302 (2024).
- 25) N. Pieczulewski et al., *APL Mater.* **13**, 061122 (2025).
- 26) J. E. Dill, X. Wei, C. Yu, A. Arvind, S. Agrawal, D. Bhattacharya, K. Shinohara, D. Jena, and H. G. Xing, (2025) arXiv:2512.08871.
- 27) H. K. Cho, A. Mogilatenko, N. Susilo, I. Ostermay, S. Seifert, T. Wernicke, M. Kneissl, and S. Einfeldt, *Semicond. Sci. Technol.* **37**, 105016 (2022).
- 28) "Chapter 4-test structures for ohmic contact characterization," *VLSI Electronics Microstructure Science*, S. S. Cohen and G. S. Gildenblat (ed.) (Elsevier, Amsterdam, 1986), Vol. 13, p. 87.
- 29) T. Maeda, R. Page, K. Nomoto, M. Toita, H. G. Xing, and D. Jena, *Appl. Phys. Express* **15**, 061007 (2022).
- 30) S. Srivastava, S. M. Hwang, M. Islam, K. Balakrishnan, V. Adivarahan, and A. Khan, *J. Electron. Mater.* **38**, 2348 (2009).
- 31) C. G. Van de Walle, C. Stampfl, J. Neugebauer, M. D. McCluskey, and N. M. Johnson, *MRS Internet J. Nitride Semicond. Res.* **4**, 890 (1999).