

Ultrathin CdSe Nanowire Field-Effect Transistors

ANUBHAV KHANDELWAL,^{1,3} DEBDEEP JENA,¹
JAMES W. GREBINSKI,² KATHERINE LEIGH HULL,² and
MASARU K. KUNO²

1.—Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556.
2.—Department of Chemistry & Biochemistry, University of Notre Dame. 3.—E-mail:
akhandel@nd.edu

We report the fabrication, and electrical and optical characterization, of solution-liquid-solid (SLS) grown CdSe nanowire field-effect transistors. Ultrathin nanowires (7–12 nm diameters) with lengths between 1 μm and 10 μm were grown by the SLS technique. Al-CdSe-Al junctions are then defined over oxidized Si substrate using photolithography. The nanowires, which were very resistive in the dark, showed pronounced photoconductivity even with a visible light source with resistance decreasing by a factor of 2–100 for different devices. Field-effect devices fabricated by a global backgating technique showed threshold voltages between -7.5 V and -2.5 V and on-to-off channel current ratios between 10^3 and 10^6 at room temperature. Channel current modulation with gate voltage is observed with the current turning off for negative gate bias, suggesting unintentional n-type doping. Further, optical illumination resulted in the loss of gate control over the channel current of the field-effect transistor.

Key words: CdSe, nanowire, field-effect transistor

Chemically synthesized semiconductor nanowires are attracting increasing attention as the building blocks for the bottom-up approach to the fabrication of nanoscale devices and sensors.^{1,2} Apart from the conventional electronic and photonic applications such as FETs and diodes, semiconductor nanowires are ideal for studying one-dimensional electron transport^{3,4} and explore quantum effect-based devices.⁵ Conventionally, nanowires are grown by the vapor-liquid-solid (VLS) technique, which is based on either molecular beam epitaxy or chemical vapor deposition. Other growth techniques such as electrochemical deposition and template growth^{6,7} have also been employed. Many room-temperature applications such as nanowire-based FETs, diodes, and logic gates, using both p-type and n-type nanowires, have been demonstrated.^{1,8,9} Optical properties of various nanowires have been studied as well.¹⁰ However, the diameters of nanowires reported so far are typically several tens of nanometers.^{11,12} Furthermore, conventional growth processes, particularly VLS, are expensive and time consuming, fac-

tors that can prove to be a potential hindrance for industrial applications of nanowires.

In this work, we demonstrate the device applications of CdSe nanowires, which are grown by a solution-liquid-solid (SLS) process. We briefly introduce the SLS growth technique; details are reported elsewhere.¹³ We then report electrical and optical characterization of FETs where these nanowires form the channel.

CdSe nanowires are synthesized in solution, leveraging advances in the SLS growth of semiconductor wires. In the solution-based approach, a low melting metallic catalyst particle (In, Sn, Bi, and Ga, among others) is first synthesized using colloidal chemistry. The choice of a low melting element enables catalytic activity at temperatures between 300°C and 400°C. For the particular case of CdSe, Bi nanoparticles with diameters between 1.5 nm and 3 nm are used to catalyze the wire growth. Both Bi particles and a common Se precursor (trioctylphosphine selenide (TOPSe)) are mixed in a glove box and are then rapidly introduced into a solution containing fatty acid-coordinated Cd ions. A rapid color change is observed, indicating a reaction between the Cd

(Received March 2, 2005; accepted July 25, 2005)

and Se ions. Nanowire growth is achieved by the presence of the metallic catalyst particle, which promotes crystallization exclusively along the $\langle 111 \rangle$ and $\langle 0001 \rangle$ directions of the zincblende and wurtzite phases of CdSe, respectively. This asymmetric crystallization, in turn, leads to the creation of CdSe nanowires with lengths between 1 μm and 10 μm . Wire diameters are loosely determined by the size of the Bi catalyst particle and range in size from 7 nm to 12 nm (Fig. 1). A typical growth run takes about an hour, making the SLS technique well suited for high-volume production.

These wires in solution are then drop cast over the surface of an oxidized p-Si wafer, on the back surface of which a 200-nm-thick Al/Au layer is deposited by e-beam evaporation to form the global back gate of the FET. The density of wires on the substrate can be controlled by varying the concentration of the nanowires in solution. The solution is then dried in air. Upon drying, wires are observed to stick to the substrate; this is believed to be due to van der Waals forces.¹⁴ Surfactants (or ligands) around the SLS-grown wires also help in adhesion to the surface. Photolithography is then carried out followed by e-beam evaporation to form source-drain metal pads (200-nm Al/Au). The nanowires are then coated with PMMA in order to avoid any possible surface reaction between air and the wires. Uncoated samples showed degradation of transport properties with time, while PMMA-coated samples were observed to give reproducible results.

Two terminal, room-temperature measurements were done using an electrical probe station and an Agilent 4155B semiconductor parameter analyzer. Many devices were tested and current conduction was observed only in those devices where source drain is shorted by wires, confirmed by scanning electron microscopy and atomic force microscopy imaging. The back-gated MOSFETs were used for two terminal transport measurements of wires by keeping the gate bias at 0 V.

Current conduction was observed in 15 devices out of which 11 showed ohmic behavior while 4 were rectifying. Since all metal contacts are similar (200-nm-thick Al/Au), the difference in the behavior may be attributed to the asymmetric contacts formed with the wires. In the dark, the wires were observed to be quite resistive (Fig. 2a), with typical current levels being a few nA for a few volts of applied bias. Such high resistivity can be attributed to the fact that the wires are nominally undoped, and any carriers are either thermally generated or are from a low density of unintentional dopant atoms incorporated during the growth process. Further, metal con-



Fig. 1. High-resolution transmission electron microscopy image of CdSe nanowire.

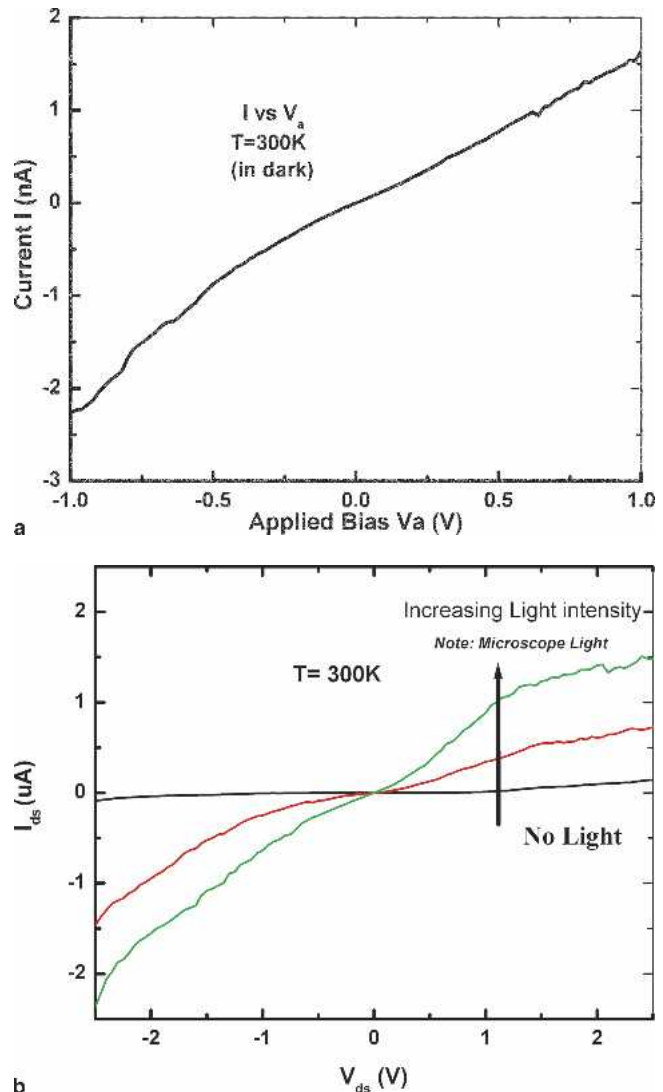


Fig. 2. (a) Current versus voltage curve for wires in the dark at room temperature. (b) Current versus voltage curves for wires with varying light intensity at room temperature.

tacts are not annealed in order to avoid charge injection into the channel from the source-drain metal contacts.^{11,15} Note that since the surface-to-volume ratio of a thin nanowire is rather large, the relatively large density of surface states, if electrically active, can drastically affect the transport properties of the nanowire. However, in the presence of optical excitation with visible microscope lamp light, pronounced photoconductivity is observed (Fig. 2b), which shows that the transport is not dominated by surface states. For devices with ohmic contacts, a decrease in nanowire resistance in the presence of light varied over a large range (between 2 and 100). This variation is primarily because of the different number of wires between the pads. In a few cases, resistance decreased from tens of M Ω s to a few M Ω s. The increase in current was nearly symmetrical for both positive and negative applied biases for all devices, irrespective of ohmic or rectifying contacts, consistent with the increase in the number of carriers in light. Please note that CdSe is a direct band-

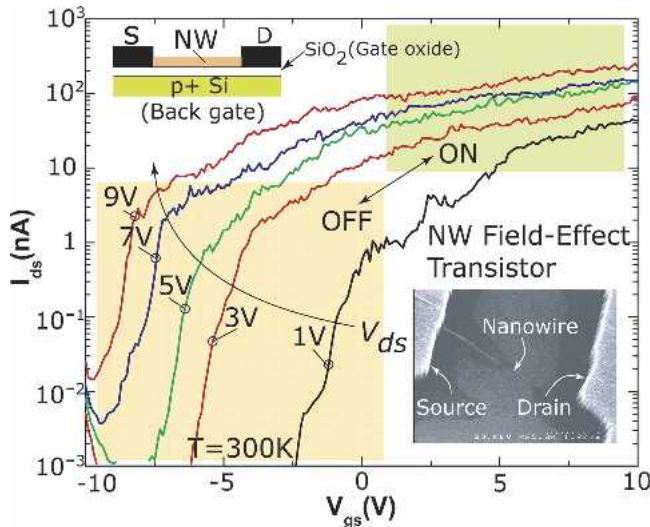


Fig. 3. I_{ds} - V_{gs} plot for varying V_{ds} shown by the back-gated MOSFETs, where wires form the channel. Measurements were done at room temperature. The inset figure shows the CdSe nanowire between the source-drain metal pads, 3 μm apart.

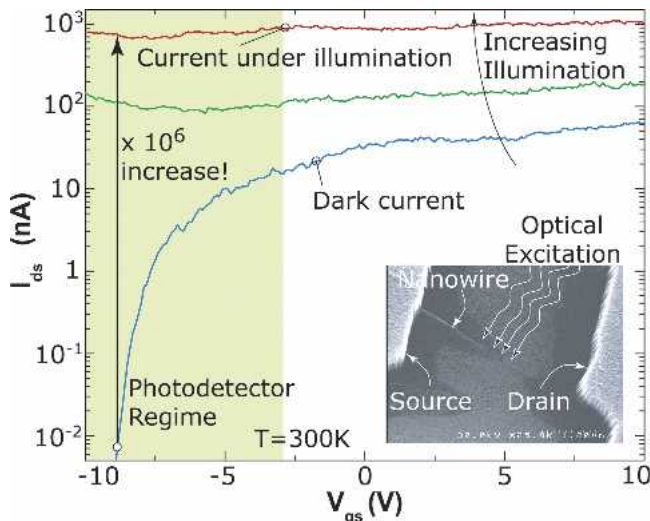


Fig. 4. I_{ds} - V_{gs} plot for varying light intensity. The V_{ds} is fixed at 4V and the measurement is at room temperature under visible (lamp) light.

gap semiconductor ($E_g = 1.75$ eV, $\lambda_{\text{cutoff}} \sim 700$ nm) and is expected to show strong photoconductivity at visible wavelengths.

We now present the results of electrical characterization of the NWFETs. Measurements done in the dark show modulation of channel current I_{ds} with varying gate voltage V_{gs} . Figure 3 shows I_{ds} versus V_{gs} at varying drain source voltage V_{ds} . The I_{ds} - V_{gs} characteristics shown are typical of an n-channel device with device current turning off for a negative gate bias, suggesting n-type unintentionally doping. The NWFETs show typical on-off current ratios between 10^3 and 10^6 , threshold voltages between -7.5 V and -2.5 V and subthreshold slopes between 300

mV/dec and 700 mV/dec. The high values of threshold voltages and subthreshold slopes are due to the thick oxide layer ($t_{\text{ox}} \sim 25$ nm) used for backgating. Under optical excitation, gate control over the channel current weakens (Fig. 4). A current increment by over 10^6 is observed for high negative gate bias, which makes the device suitable for optical sensing applications. Loss of gate control over channel current indicates the dominance of optically generated carriers in the wires over thermally generated ones.

In summary, the SLS technique is used to grow CdSe nanowires, with diameters between 7 nm and 12 nm. These nanowires showed pronounced photoconductivity at visible wavelengths with resistance decreasing from a factor of 2 to 100 for different devices. Back-gated MOSFETs were fabricated and field-effect characteristics demonstrated. Nanowires were found to be unintentionally n-type doped. Loss of gate control in the presence of light was observed. Having demonstrated conventional electronic device applications of CdSe nanowires, current work on characterizing transport in single wire CdSe nanowires with emphasis on quantum effect-based device applications is in progress. The strong optical response, coupled with the ability to fabricate CdSe NWFETs by an industrially attractive growth technique, holds much promise for applications in future electronic and optical devices.

REFERENCES

1. M.T. Bjork, B.J. Ohlsson, C. Thelander, A.I. Persson, K. Deppert, L.R. Wallenberg, and L. Samuelson, *APL* 81, 2 (2002).
2. X. Duan, Y. Huang, R. Agarwal, and C.M. Lieber, *Nature* 421, 241 (2003).
3. S. Michotte, S.M. Tempfli, and L. Piraux, *Physica C* 391, 15 (2003).
4. A.T. Tilke, F.C. Simmel, H. Lorenz, R.H. Blick, and J.P. Kotthaus, *Phys. Rev. B: Condens. Matter Mater. Phys.* 68, 075311 (2003).
5. K. Heike and M. Ulfward, *Phys. Rev. B: Condens. Matter Mater. Phys.* 62, 15 (2000).
6. D.J. Pena, K.N. Jeremiah, A.J. Carado, T.E. Mallouk, C.D. Keating, B. Razavi, and T.S. Mayer, *J. Phys. Chem. B* 106, 7458 (2002).
7. X. Liang, J.L. Li, X. Liu, J.-Z. Wang, H. Liu, Q. Xue, J. Jia, *Surf. Interface Analysis* 36, 100 (2004).
8. Z. Zhong, F. Qian, D. Wang, and C.M. Lieber, *Nano Lett.* 3, 343 (2003).
9. L.J. Lauhon, M.S. Gidiksen, D. Wang, and C.M. Lieber, *Nature* 420, 57 (2002).
10. K. Hiruma, M. Yazawa, T. Katsuyama, K. Ogawa, K. Haraguchi, M. Koguchi, and H. Kakabayashi, *J. Appl. Phys.* 77, 447 (1995).
11. J.Y. Yu, S.W. Chung, and J.R. Heath, *J. Phys. Chem. B* 104, 11864 (2000).
12. S. De Franceschia, J.A. van Dam, E.P.A.M. Bakkers, L.F. Feiner, L. Gurevich, and L.P. Kouwenhoven, *APL* 83, 14 (2003).
13. J.W. Grebinski, K.L. Richter, J. Zhang, T.H. Kosel, and M. Kuno, *J. Phys. Chem. B* 108, 9745 (2004).
14. R.A. Zingaro, W.C. Cooper, and V.N. Reinhold, eds., *Selenium* (1974), p. 123.
15. J. Guo, J. Wang, E. Polizzi, S. Dutta, and M. Lundstrom, *IEEE Trans. Nanotechnol.* 2, 329 (2003).