MBE-Grown Ultra-shallow AlN/GaN HFET Technology

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Due to large polarization effects, two-dimensional electron gas (2DEG) concentrations higher than $1x10^{13}$ cm^{-2} can be produced at the AlN/GaN heterojunction with AlN barriers as thin as 2 nm. This ultra-shallow channel together with the wide bandgap of AlN (6.2 eV) makes AlN/GaN heterojunction field effect transistors (HFET) extremely attractive for high frequency (>100 GHz) high power applications. At Notre Dame, these structures have been grown using molecular beam epitaxy and the record transport properties among III-V nitrides are achieved: a sheet resistance of ~ 170 ohm/square for a single heterostructure at room temperature. HFETs have been fabricated with optical lithographically defined gates. At present the device dc characteristics show a maximum drain current of 800 mA/mm and transconductance of 180 mS/mm for 3 μm long gate. This clearly demonstrates its value toward high speed devices. The development as well as challenges of this technology will be discussed here.

Introduction

AlGaN/GaN heterojunction field effect transistor (HFET) technology is rapidly advancing into the 100-200 GHz operation regime with the scaling of gate length, and the reduction of parasitic elements. Scaling of vertical heterostructure dimensions is needed to support further improvements in HFET performance. Therefore, ultra-thin barrier layers under the gate have been of increasing interest, formed either by gate recess or by direct epitaxy [1, 2]. The large bandgap of AlN (6.2 eV) allows efficient carrier confinement and lowers gate leakage current, and the absence of alloy disorder (compared to AlGaN barriers) results in improvement of both low- and high-field carrier transport. A handful of variations on AlN/GaN HFETs have been reported with notable success [2, 3, 4, 5]. However, in the early years, AlN was exploited as an insulating layer for a doped GaN channel, i.e. metal-insulator-semiconductor field effect transistors. Therefore, the epitaxial quality of the AlN layer deposited was largely unknown; neither was reported the existence and transport properties of the two-dimensional electron gas (2DEG), which can be produced at the AlN/GaN heterojunction due to the large polarization effect similar to that in the AlGaN/GaN heterostructures. In 2000, Smorchkova et al. for the first time reported [6] the critical thickness of AlN grown on GaN and resultant 2DEG channel properties. No devices were demonstrated until recently Higashiwaki et al. [2] reported a f_t of 107 GHz utilizing a SiN/AlN/GaN structure. In his device structure the AlN was 2.5 nm thick, however, there was no detectable 2DEG in the channel until a thin layer SiN of 2-3 nm was deposited. In our lab, we have recently developed high quality as-grown AlN/GaN structures by molecular beam epitaxy (MBE) [7]. A 2DEG concentration (n_s) of ~1.2 x 10^{13} cm^{-2} with mobility

(μ) of ~ 1200 cm^2/Vs is achieved in the 2.5 nm AlN heterostructure and the 2DEG concentration increases to ~ 6 x 10^{13} cm^{-2} with a 7 nm AlN, which is its critical thickness on GaN. Toward this end, we have explored AlN/GaN HFETs employing an ultrathin 2-5 nm AlN barrier layers.

Device structures

Growth and characterization

All growths of the AlN/GaN heterojunctions studied here were performed by MBE in a Veeco Gen 930 system on semi-insulating GaN templates on sapphire. All growth were performed under metal rich conditions, with the Ga flux ~ 10^{-7} torr for the GaN layers, and the Al flux ~ 4 x 10^{-8} torr for the AlN layers. The Ga shutter was kept open during the growth of AlN layers to enhance the diffusivity of Al adatoms on the surface. Both the GaN buffer layers and the AlN layers were grown at 800 ^oC. Active N_2 was supplied through a Veeco RF source, with a plasma power of 150 - 300 W. The structures comprised of a 100 - 200 nm-thick undoped GaN buffer layer, followed by an ultra thin AlN cap, the thickness of which was varied between 2.3 and 5.0 nm. The growth rate was measured to be 86.4 nm/hr at 150 W - it was calibrated by a high-resolution X-ray diffraction (XRD) measurement for a 9-period 4.6 nm/56.0 nm AlN/ GaN multiple quantum well (MQW) calibration structure. The thicknesses and the growth rate were calibrated by fitting the measured data to a simulation. A typical atomic force microscopy (AFM) scan of the as-grown AlN surface is shown in Figure 1. Also shown is the cross section transmission electron microscopy (TEM) image of the AlN/GaN MQW calibration sample.

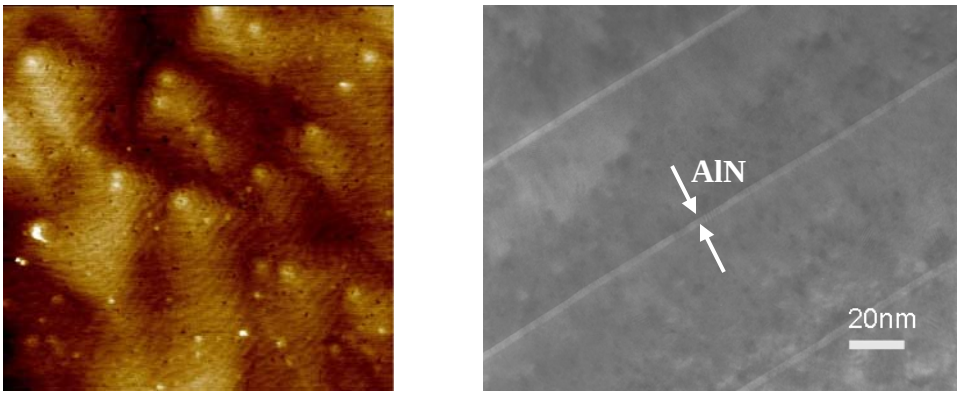

Figure 1. 2 μm x 2 μm AFM scan of as-grown AlN surfaces below critical thickness (left). Cross section TEM image of the AlN/GaN MQW calibration sample (right).

The mobility and charge concentration of the 2DEG were measured by Hall Effect measurements. Within the AlN thickness investigated here, the typical concentration and mobility after growth optimization are 1.2 x 10^{13} cm^{-2} with ~ 1200 cm^2/Vs and 4 x 10^{13} with ~ 900 cm^2/Vs, which results in a record low sheet resistance of ~ 170 Ω/square in a single III-V nitride heterostructure. This charge density is close to the expected value as a result of polarization charges at the AlN/GaN interface, and the study of its transport properties along with details of growth and charge analysis can be found in Ref. [7].

Fabrication

HFETs were fabricated using chlorine-based reactive-ion etching for mesa isolation. Ti/Al/Ni/Au source and drain contacts were then deposited by electron-beam evaporation. Rapid thermal annealing was used to obtain alloyed ohmic contacts. Finally, a gate stack of Al_2O_3/Ni/Au was deposited by e-beam evaporation. The Al_2O_3 layer was used to mitigate the gate leakage owing to its high dielectric constant (~ 10) and large bandgap.

Device performance

First generation

The first generation of HFETs were fabricated on un-optimized AlN/GaN heterostructures with a 3 nm AlN cap. In the as-grown structure, μ and n_s were found to be 300 cm^2/Vs and 3.03 x 10^{13} cm^{-2} at 295K, and 460 cm^2/Vs and 2.8 x 10^{13} cm^{-2} at 77K. What is worth noting is that the as-deposited contacts were found to be ohmic, and a contact resistance of 2.7 Ωmm was determined from the transmission line method (TLM) measurement. A subsequent anneal at 860 ^oC was able to improve the ohmic contact resistance to 0.36 Ωmm. However, the ohmic behavior of the as-deposited ohmic metals indicates existence of a strong tunneling/leakage path. Therefore, 10 nm Al_20_3 was then deposited by e-beam evaporation over the entire sample surface as a gate dielectric, followed by deposition of Ni/Au as the gate metal. Hall Effect measurements were repeated after the completion of device fabrication to determine the impact of the Al_2O_3 oxide layer. Mobility and sheet density were found to be 157 cm^2/Vs and 1 x 10^{13} cm^{-2}, respectively. The TLM measurements in Figure 2 show that annealing improved the contact resistance, but the Al_2O_3 deposition resulted in a more resistive channel, which is consistent with the Hall measurement. In the later generation of devices fabricated on heterostructures with high carrier mobilities, it was found that the as-deposited ohmic metals behave more like leaky Schottky diodes instead of ohmic contacts. Thus, we speculate that it is likely the surface roughness (exceeding 0.7 nm on this sample) that allows as-deposited Ti/Al/Ni/Au metal contacts to be ohmic, which also explains the observed low mobility.

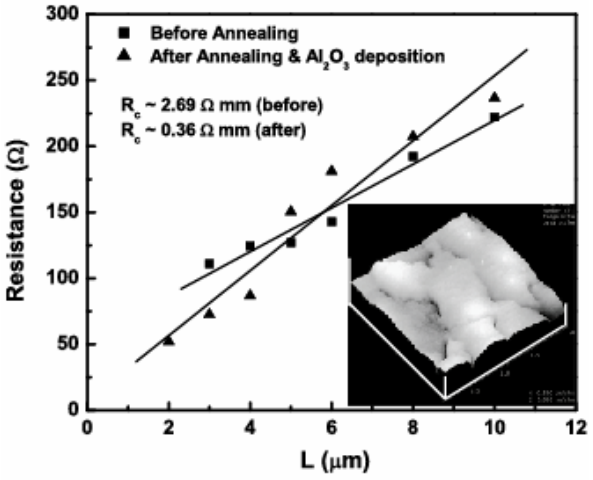

Figure 2. TLM measurements before and after annealing and Al_2O_3 deposition. Inset shows 2 μm x 2 μm AFM image of AlN surface roughness with a vertical scale of 5 nm.

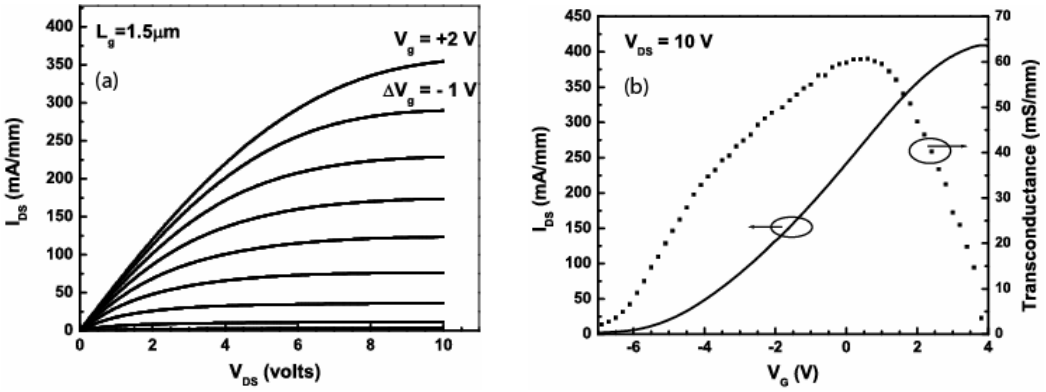

Figure 3. Family I-V (a) and transconductance (b) of first generation HFET.

Capacitance-voltage measurements on the gate diodes clearly show a 2DEG in the device structure, with a sheet carrier concentration of 1 x 10^{13} cm^{-2} at zero bias. The centroid of the 2DEG is calculated to be ~ 2 nm below the AlN/GaN interface, using a self-consistent Schrodinger-Poisson solver. The Al_2O_3 dielectric constant was also extracted from C-V characteristics to be ~ 7.5. HFET DC current-voltage characteristics at room temperature are shown in Figure 3. The source-gate and gate-drain distances are both 2 μm, and the gate length and width are 1.5 μm and 75 μm, respectively. A pinchoff voltage of V_g = -6 V is observed. The output current reached its maximum, ~ 400 mA/mm, at V_g = 4 V, and the transconductance g_m peaked at 60 mS/mm at V_g = 0.43 V. The observed low I_{DS} compared to current state of the art GaN-based HFETs can be attributed to the low mobility in this structure.

Second generation

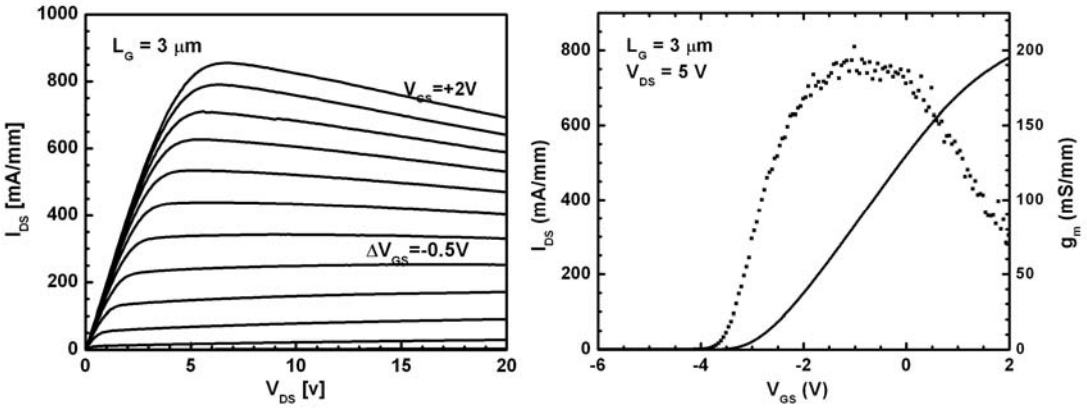

Figure 4. Family I-V (a) and transconductance (b) of second generation HFET.

Upon growth optimization [7], the surface roughness was decreased to ~ 0.3 nm, thus leading to improved carrier mobilities, higher than 800 cm^2/Vs. Figure 4 shows the typical device performance fabricated on such high mobility AlN/GaN heterostructures.

For this particular sample, the AlN thickness is 5 nm, n_s = 3.97 x 10^{13} cm^{-2} and μ = 880 cm^2/Vs. 10 nm thick Al_2O_3 was deposited only under the gate metal to prevent increase of the access resistance since it was found that the channel charge concentration decreases after Al_2O_3 deposition. The maximum current is found to be > 800 mA/mm and transconductance > 180 mS/mm. Taking into account the high contact resistance, ~ 3 Ωmm, the intrinsic g_m can be calculated to be ~ 400 mS/mm, which is close to the expected value.

Discussions

The devices above show comparable dc performance to that of devices based on the conventional AlGaN/GaN heterostructures. This clearly demonstrates the potential of ultra-shallow AlN/GaN heterostructures toward the high speed high power applications. However, there are several aspects yet to be developed/improved: (1) ohmic contacts, (2) gate leakage, (3) passivation and (4) ac performance. The maximum current is still below the expected value (assuming n_s = 2 x 10^{13} cm^{-2} and an effective carrier velocity v_{eff} = 1 x 10^7 cm/s, I_{DSmax} = 3.2 A/mm). This is believed to be due to the high contact resistance currently present in these devices similar to the conventional AlGaN/GaN heterostructures. The high access resistance also decreases the extrinsic g_m, and thus the device speed. At present, e-beam deposited Al_2O_3 is used to mitigate the gate leakage, which is generally high in the MBE grown III-V nitrides owing to both the metal-rich growth conditions and the high dislocation density. The preliminary results indicate there is a fairly high density of interface states at the Al_2O_3/AlN interface, besides, the addition of Al_2O_3 decreases the gate capacitance. An alternative gate leakage reduction scheme is necessary to fully explore advantages offered by the ultra-shallow AlN barrier. Finally, the ac performance of these devices still needs to be characterized. Surface passivation is essential for high efficiency large signal power applications. These investigations are currently underway.

Acknowledgments

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