Graphene Nanoribbon Tunnel Transistors

Qin Zhang, Tian Fang, Huili Xing, Alan Seabaugh, and Debdeep Jena

***Abstract*—A graphene nanoribbon (GNR) tunnel field-effect transistor (TFET) is proposed and modeled analytically. Ribbon widths between 3 and 10 nm are considered, corresponding to energy bandgaps in the range of 0.46 to 0.14 eV. It is shown that a 5-nm ribbon width TFET can switch from on to off with only 0.1-V gate swing. The transistor achieves 800 μA/μm ON-state current and 26 pA/μm OFF-state current, with an effective subthreshold swing of 0.19 mV/dec. Compared to a projected 2009 nMOSFET, the GNR TFET can provide 5$\times$ higher speed, 20$\times$ lower dynamic power, and 280 000$\times$ lower OFF-state power dissipation. The high performance of GNR TFETs results from their narrow bandgaps and their 1-D nature.**

***Index Terms*—Graphene, subthreshold swing, tunnel transistor, 1-D.**

I. Introduction

THE TUNNELING field-effect transistor (TFET) is attracting attention because of its low subthreshold swing and low OFF-state leakage [1]–[7]. Choi *et al.* [4] have experimentally demonstrated a Si n-channel TFET with a 52.8 mV/dec subthreshold swing. However, the ON-state current density in this device is two orders of magnitude lower than a high-performance MOSFET. To enhance the ON-state tunneling current, narrower bandgap materials with smaller effective masses are being considered [6], [7]; Knoch *et al.* [1], [2] show by simulation that 1-D TFETs are preferred to bulk FETs because of the superior gate control and a reduction of transverse energy component in the 1-D tunneling transport. Graphene nanoribbons (GNRs) have a width-tunable narrow bandgap [8]–[13], which is particularly favorable for TFET applications, and more amenable to planar processing and large-scale integration than carbon nanotubes (CNTs). In this letter, the GNR TFET is analyzed. It is shown that TFETs based on GNRs are capable of higher drive currents than III–V or group IV channel TFETs with lower subthreshold swing, higher speed, and orders of magnitude lower power dissipation.

II. Device Structure and Operation

Similar to a CNT TFET [1], [2], the schematic of a p-channel GNR TFET is shown in Fig. 1. The source is heavily doped to be n^+, and the drain is p^+. The channel is also designed to be p^+, but is fully depleted at zero gate bias.

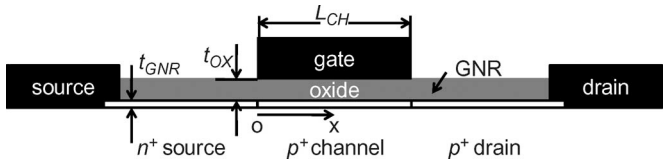

Fig. 1. Schematic cross section of an interband p-channel GNR TFET, where the GNR is heavily doped or electrostatically doped to form a p^+n^+ tunnel junction, and the gate is placed over the fully depleted p-side.

Heavy doping concentrations are generated either by dopants or electrostatically engineered [1]. Due to the strong C–C bonds in GNRs (and CNTs), chemical doping is challenging, but rapid progress is being made in that direction [13]. On the other hand, electrostatic doping has successfully been demonstrated for achieving tunnel junctions in CNT FETs [3], and the same can be achieved for GNRs. The electrostatics of this quasi-1-D geometry is solved by a surface potential method, where the GNR surface potential, $\Phi_F(x)$, is given by the 1-D Poisson equation [14]

$$\frac{d^2\Phi_F(x)}{dx^2} - \frac{\Phi_F(x) - \Phi_G - \Phi_{\rm BI}}{\lambda^2} = -\frac{q(\pm N)}{\varepsilon_{\rm GNR}}. \quad (1)$$

Here, Φ_G is the gate potential, $q\Phi_{\rm BI} = E_G/2 - qV_T\ln(N/n_i)$ is the built-in potential, $E_G = 2\pi\hbar v_F/3w_{\rm GNR}$ [9], [10] is the GNR's bandgap, $v_F \sim 10^8$ cm/s is the Fermi velocity of carriers in graphene [15], $w_{\rm GNR}$ is the ribbon width, V_T is the thermal voltage, n_i is the intrinsic carrier concentration, N is the doping concentration; the "+" sign is for donors, and the "−" sign is for acceptors. The parameter $\lambda = \sqrt{(\varepsilon_{\rm GNR}/\varepsilon_{\rm OX})t_{\rm GNR}t_{\rm OX}}$ is the relevant length scale for potential variations; $\varepsilon_{\rm GNR}$ and $\varepsilon_{\rm OX}$are the GNR and oxide dielectric constants, respectively, and $t_{\rm GNR} = 0.35$ nm [16] is the thickness of the GNR. Lastly, $t_{\rm OX}$ is the gate oxide thickness. Equation (1) is applied in all three regions: n^+ source, p^+ channel, and p^+ drain. The boundary conditions are the following: 1) zero electric field at $x = \pm\infty$; 2) continuous electric field and potential at the source/channel and drain/channel junction; 3) $E_F - E_C = qV_T$ at the n^+ source, and $E_V - E_F = qV_T$ at the p^+ drain; and 4) the valence band along the channel is aligned with the Fermi level at the source, at zero gate bias. This guarantees low OFF-state current at zero gate bias and a small turn-on voltage. For this analysis, the supply voltage is limited to half the GNR's band gap where ambipolar effects can be ignored. The computed band diagrams for a GNR pTFET with a supply voltage of 0.1 V are shown in Fig. 2(a) for the OFF-state at $V_{\rm GS} = 0$ and in Fig. 2(b) for the ON-state at $V_{\rm GS} = -0.1$ V, for a ribbon width $w_{\rm GNR} = 5$ nm, gate length $L_{\rm CH} = 20$ nm, and $t_{\rm OX} = 1$ nm.

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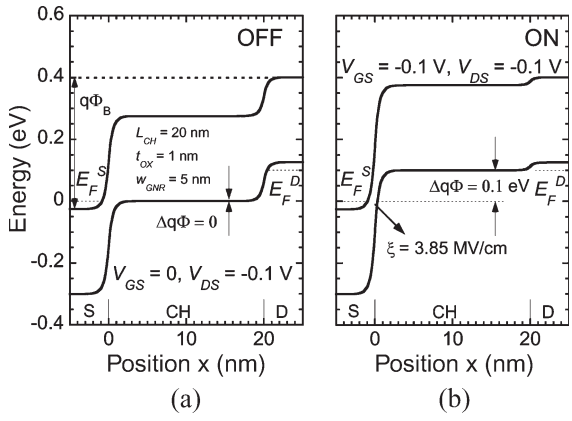

Fig. 2. Energy band diagrams for a GNR p-TFET at (a) OFF-state and (b) ON-state with a supply voltage of 0.1 V. The calculated gate oxide thickness is 1 nm, the GNR width is 5 nm, and the gate length is 20 nm.

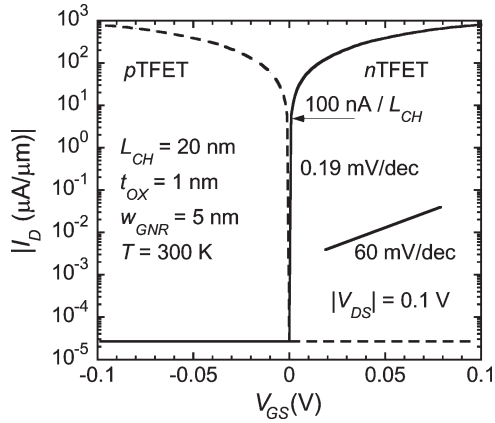

Fig. 3. Calculated transfer characteristics of (solid line) GNR n- and (dashed line) p-TFETs at room temperature using the same geometry as Fig. 2.

At the ON-state, the 1-D Zener tunneling current is obtained by integrating the product of charge flux and the tunneling probability within the energy window $\Delta q\Phi$

$$\begin{aligned} I_D &= \int qv_g\rho_{\rm GNR}(k) \\ &\quad \times \left[f\left(E-E_F^D\right)-f\left(E-E_F^S\right)\right]T_{\rm WKB}dk \\ &= \int_0^{\Delta\Phi} \frac{q}{\pi\hbar}\left[f\left(E-E_F^D\right)-f\left(E-E_F^S\right)\right]T_{\rm WKB}dE \\ &= \frac{q^2}{\pi\hbar}T_{\rm WKB}V_T \\ &\quad \times \Big[\ln\left(\exp\left(\left(\Delta\Phi-E_F^S\right)/qV_T\right)+1\right) \\ &\qquad -\ln\left(\exp\left(-E_F^S/qV_T\right)+1\right) \\ &\qquad +\ln\left(\exp(-V_{\rm DS}/V_T)+1\right) \\ &\qquad -\ln\left(\exp\left((\Delta\Phi-qV_{\rm DS})/qV_T\right)+1\right)\Big] \end{aligned} \tag{2}$$

where $v_g = 1/\hbar\ dE/dk$, $\rho_{\rm GNR}({\rm k}) = 1/\pi$ is the 1-D density of states, and $T_{\rm WKB}$ is the tunneling probability, calculated by applying the WKB approximation to a triangular potential with a barrier height of E_G [17]

$$T_{\rm WKB} = \exp\left(-\frac{\pi}{4}\frac{E_G^2}{\hbar v_F q\xi}\right) \tag{3}$$

is dependent on the bandgap E_G, and the electric field ξ across the tunnel junction. Using (2) and (3), taking $\Delta q\Phi$ and ξ from the band diagram calculations in Fig. 2(b), the drain–current density at room temperature is calculated as a function of the gate-to-source voltage and shown in Fig. 3, dashed line. Here, the effect of carrier injection into the channel on the channel electrostatics is neglected. The OFF-state leakage is assumed to arise from thermal emission over the barrier $q\Phi_B$ between source and the drain (see Fig. 2). The resulting leakage current for the 1-D case is given by $I_{\rm OFF} = q^2V_T/\hbar\pi\exp(-\Phi_B/qV_T)$ [18], which is 0.13 pA, somewhat lower than 1 pA observed in the GNR FET OFF-state [12]; this might be anticipated from the higher barrier $q\Phi_B$ of TFET versus the FET.

The complementary nTFET with symmetric geometry is also shown in Fig. 3, solid line. From this calculation, a 0.1-V swing can turn the transistor from on at 800 μA/μm to off at 26 pA/μm, with an on-to-off ratio of more than seven orders of magnitude. The subthreshold swing is 0.19 mV/dec, using a current per unit width of 100 nA/$L_{\rm CH}$ [19] to define the threshold voltage, indicated in Fig. 3. Comparison of the 20-nm gate length GNR TFET to the 2009 nMOSFET target from the 2007 Edition of the International Technology Roadmap for Semiconductors (ITRS) Roadmap [20] is given in Table I. It is shown that the intrinsic switching speed of the GNR TFET is more than five times that of the nMOSFET target. The OFF-state channel leakage of the GNR TFET is more than four orders of magnitude lower, and the supply voltage is one order of magnitude lower, which makes the off-leakage power more than five orders of magnitude lower and the dynamic power also more than one order of magnitude lower than the high-performance nMOSFET. Certainly, these predictions represent upper bounds on the expected performance, as the gate oxide leakage, interface charge, and parasitic resistances will all act to degrade this projection.

III. ON-State Current Density of Tunnel Transistors

Recently, GNR FETs of sub-10-nm width have shown ON-state current density as high as 2000 μA/μm [12]. From the Zener tunneling current density expression by Sze [18], it is not surprising that the GNR TFET can have an ON-state current density as high as 800 μA/μm (Fig. 3), while the Si TFET shows 12.1 μA/μm for $V_{\rm DS} = 1$ V, and only 0.4 μA/μm for the comparable $V_{\rm DS} = 0.1$ V and $V_{\rm GS} - V_{\rm TH} = 0.1$ V [4]

$$J_t = \frac{\sqrt{2m^*}q^3\xi V}{4\pi^2\hbar^2E_G^{1/2}}\exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\xi\hbar}\right) \tag{4}$$

where V is the reverse bias. The ON-state current density of a bulk tunnel transistor is the product of J_t and channel thickness, where V is the supply voltage $V_{\rm DD}$. Fig. 4(a) shows the calculated ON-state tunneling current density versus electric field and channel material at a supply voltage of 0.1 V. The solid line shows the current per unit gate width for bulk TFETs, assuming the channel thickness is 5 nm. The dashed line shows the current per ribbon width of GNR TFETs for the width of 3,

TABLE I
SPEED AND POWER ESTIMATES COMPARING 2009 nMOSFETs TARGETS FROM THE 2007 EDITION ITRS ROADMAP [20] WITH GNR TFETs USING THE GEOMETRY OF FIG. 1

	2009 *n*MOSFET	GNR TFET	unit
Equivalent oxide thickness *EOT*	0.75	1	nm
Supply voltage V_{DD}	1	0.1	V
Drive current I_D	1639	800	μA/μm
Off-state leakage current I_{OFF}	0.70	0.000025	μA/μm
Intrinsic speed ~ I_D / $C_{ox} V_{DD}$	1961	11000	GHz
Off-leakage power ~ I_{OFF} V_{DD}	0.70	0.0000025	μW/μm
Dynamic power ~ 1/2 I_D V_{DD}	820	40	μW/μm
	ITRS 2007 Edition		

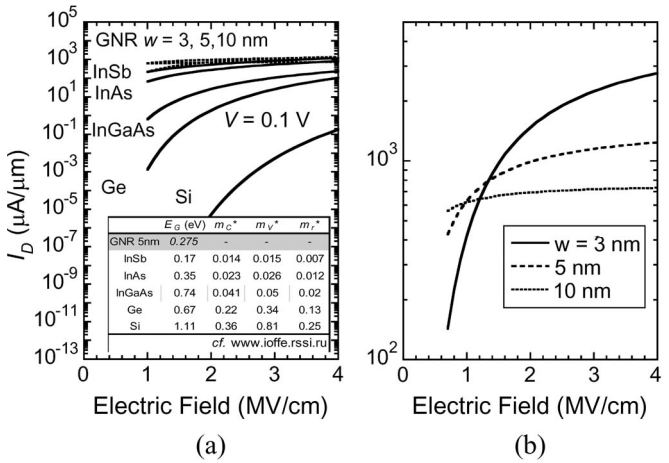

Fig. 4. (a) Calculated ON-state tunneling current density versus electric field and channel material at a supply voltage of 0.1 V. The solid line shows the current per gate width of bulk TFETs, assuming the channel thickness is 5 nm. The dashed line shows the current per ribbon width of GNR TFETs for the width of 3, 5, and 10 nm, respectively. The inset gives the materials parameters used in (2)–(4). (b) zooms in on the GNR part in (a).

5, and 10 nm, respectively, using (2) and (3). Fig. 4(b) expands the GNR data of Fig. 4(a). Although thinner GNRs with larger bandgaps have lower tunneling current, their current density can be higher beyond some point of the electric field, because of the smaller ribbon widths [see the crossover in Fig. 4(b)]. There is an optimum ribbon width for each certain electric field to achieve the maximum current density [17]. GNRs show higher tunneling current density than the widely explored low-mass semiconductors listed in the inset of Fig. 4(a), even higher than InSb which has smaller bandgap.

IV. CONCLUSION

The 1-D GNR is extremely well-suited for high-performance tunnel transistors. The GNR TFET derives its benefit from the material's properties and the tunneling mechanism, and can simultaneously achieve a high speed and low power dissipation.

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