

Formation of ohmic contacts to ultra-thin channel AlN/GaN HEMTs

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AlN/GaN-based high electron mobility transistors with ultra-thin AlN barriers of 2.3 - 5 nm are attractive candidates for very high speed applications owing to the aggressive scalability such structures afford. We report the first study on formation of ohmic contacts to these high quality ultra-thin channel heterostructures ($n_s > 1 \times 10^{13} \text{ cm}^{-2}$ and $\mu > 900 \text{ cm}^2/\text{Vs}$) with systematically varying barrier thicknesses. While the conventional ohmic contacts to AlGaIn/GaN structures generally re-

quire high temperature annealing, these ohmic contacts were found to behave ohmic or near ohmic as-deposited. Annealing (400-860 °C) improves the contact resistance to a range of 0.8 - 2 ohm-mm but the annealing conditions strongly depend on the AlN thickness as well as the heterostructure quality (μ). All alloyed contacts show smooth morphology, making them suitable for e-beam lithographically defined gate patterning.

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1 Introduction

AlGaIn/GaN high electron mobility transistor (HEMT) technology is rapidly advancing into the 100-200 GHz operation regime with the scaling of gate length, and the reduction of parasitic elements. Scaling of vertical heterostructure dimensions is needed to support further improvements in HEMT performance. Therefore, ultra-thin barrier layers under the gate have been of increasing interest, formed either by gate recess or by direct epitaxy [1, 2]. The large bandgap of AlN (6.2 eV) allows efficient carrier confinement and lowers gate leakage current, and the absence of alloy disorder (compared to AlGaIn barriers) results in improvement of both low- and high-field carrier transport.

A handful of variations on AlN/GaN HEMTs have been reported with notable success [2-5]. However, in the early years, AlN was exploited as an insulating layer for a doped GaN channel, i.e. metal-insulator-semiconductor field effect transistors. Therefore, the epitaxial quality of the AlN layer deposited was largely unknown; neither was reported the existence and transport properties of the two-dimensional electron gas (2DEG), which can be produced at the AlN/GaN heterojunction due to the large polarization effect similar to that in the AlGaIn/GaN heterostructures. Recently Higashiwaki et al. [2] reported a f_t of 107

GHz utilizing a SiN/AlN/GaN structure. In his device structure the AlN was 2.5 nm thick, however, there was no detectable 2DEG in the channel until a thin layer SiN of 2-3 nm was deposited using catalytic chemical vapor deposition (CAT-CVD). The resulting carrier mobility is low, $\sim 330 \text{ cm}^2/\text{Vs}$, indicating an un-optimized growth. It was also found that ohmic contacts formed onto SiN/AlN/GaN exhibited lower contact resistance than those onto AlN/GaN followed by SiN deposition.

In our lab, we have recently developed high quality as-grown AlN/GaN structures by molecular beam epitaxy (MBE) [6] and explored the ultra-thin channel HEMT technology [7]. A 2DEG concentration (n_s) of $\sim 1.2 \times 10^{13} \text{ cm}^{-2}$ with mobility (μ) of $\sim 1200 \text{ cm}^2/\text{Vs}$ is achieved in the 2.3 nm AlN heterostructure and the 2DEG concentration increases to $\sim 6 \times 10^{13} \text{ cm}^{-2}$ with a 7 nm AlN, which is its critical thickness on GaN. Employing these heterostructures, we have demonstrated very high DC maximum I_{DS} of $> 2 \text{ A/mm}$ with a gate length of 250 nm at room temperature on sapphire substrate. [8] Since the access resistance plays an important role on $I_{DS\text{max}}$, g_m and f_t , we have investigated ohmic contact formation on AlN/GaN structures with a barrier thickness of 2.3 - 5 nm. A very strong dependence on the AlN barrier thickness and quality of the heterostructure (described by n_s and μ) was observed.

2 Experimental

All growths of the AlN/GaN heterojunctions in this study were performed by MBE in a Veeco Gen 930 system on semi-insulating GaN templates on sapphire. All growths were performed under metal rich conditions, with the Ga flux $\sim 10^{-7}$ torr for the GaN layers, and the Al flux $\sim 4 \times 10^{-8}$ torr for the AlN layers. The Ga shutter was kept open during the growth of AlN layers to enhance the diffusivity of Al adatoms on the surface. Both the GaN buffer layers and the AlN layers were grown at 800 °C. Active N₂ was supplied through a Veeco RF source, with a plasma power of 150 - 300 W. The structures comprised of a 100 - 200 nm-thick undoped GaN buffer layer, followed by an ultra thin AlN cap, the thickness of which was varied between 2.3 and 5.0 nm. The mobility and charge concentration of the 2DEG were measured by Hall Effect measurements. Within the AlN thickness investigated here, the typical concentration and mobility after growth optimization are $1.2 \times 10^{13} \text{ cm}^{-2}$ with $\sim 1200 \text{ cm}^2/\text{Vs}$ (2.3 nm) and 4×10^{13} with $\sim 900 \text{ cm}^2/\text{Vs}$ (5 nm), which results in a record low sheet resistance of $\sim 170 \text{ } \Omega/\text{square}$ in a single III-V nitride heterostructure. This charge density is close to the expected value as a result of polarization charges at the AlN/GaN interface, and the study of its transport properties along with details of growth and charge analysis can be found in Ref. [6]. Except the samples presented in Figure 3, with the same AlN barrier thickness thus n_s , but various mobilities, all other results presented in this letter are on high mobility heterostructures ($\mu > 900 \text{ cm}^2/\text{Vs}$).

TLM (transmission line method) patterns were fabricated using chlorine-based reactive-ion etching for mesa isolation. Ti/Al/Ni/Au source and drain contacts were finally deposited by electron-beam evaporation. Rapid thermal annealing was used to obtain alloyed ohmic contacts. The I-V characteristics were tested on TLMs using an Agilent 4156C semiconductor parameter analyzer.

3 Results and discussion

Shown in Figure 1 are the I-Vs taken across two TLM pads separated by 3 μm with as-deposited metal stacks for 2.3, 3, 3.5 and 5 nm AlN barrier samples. For samples with very thin barriers of 2.3 nm, the as-deposited contacts behave ohmic owing to the strong tunnelling current as well as the large number of leakage paths (dislocations) under the large area contacts. With increasing AlN thickness, the as-deposited contacts become more Schottky-like, this is because of the suppressed tunnelling current in the thicker barrier structures. Similar effects have been observed in conventional AlGaIn/GaN HEMT structures [9], where the AlGaIn barrier was systematically thinned for improving ohmic contacts.

Upon annealing, ohmic contacts were obtained on all AlN thickness samples and contact resistance is in the range of 0.8 - 2 ohm-mm. The I-V behaviour measured across TLM pads after annealing at various temperatures is shown in Fig. 2, taking 3 nm AlN/GaN as an example. The

open channel current increases with increasing annealing temperature, reaches a maximum around 400 °C and then degrades with higher annealing temperatures. A separate annealing study revealed that it were indeed the contacts that degraded while the channel resistances remained unchanged for all the AlN thicknesses studied here. This optimal temperature was determined for a range of AlN barrier thicknesses and is plotted in the inset of Figure 2. It almost linearly increases from 400 °C to 860 °C while the AlN thickness increases from 3 nm to 5 nm.

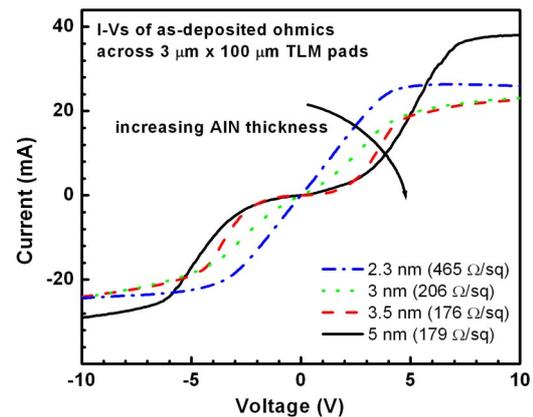


Figure 1 I-Vs of as-deposited ohmic contacts measured across TLM pads, indicating a strong tunnelling transport in thin AlN barrier samples.

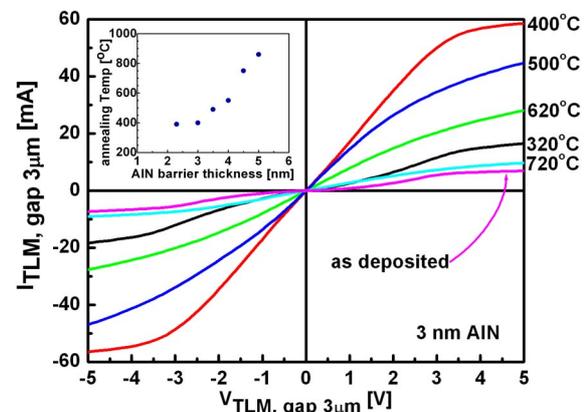


Figure 2 I-Vs of annealed contacts under different temperatures for a 3.0 nm AlN/GaN HEMT structure. The same trend was observed for 2.3, 3.5, 4.5 and 5 nm AlN structures as well and the optimal annealing temperature for each thickness is plotted in the inset: decreasing with decreasing AlN thickness.

Interestingly, it was observed there exists a strong dependence of the annealing temperature window as well as the resultant contact resistance on the quality of the heterostructure, indicated by its carrier mobility. For samples

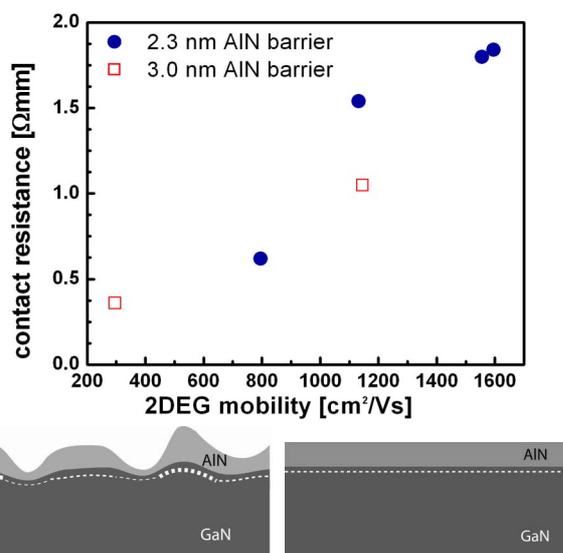


Figure 3 (Upper) The dependence of contact resistances on the AlN/GaN heterostructure quality (an AlN barrier thickness results in rather consistent 2DEG densities in the channel independent of μ). Ohmic contacts are increasingly more challenging to obtain on higher quality AlN/GaN heterostructures. (Lower) Schematic of low and high mobility AlN/GaN structure cross-sections.

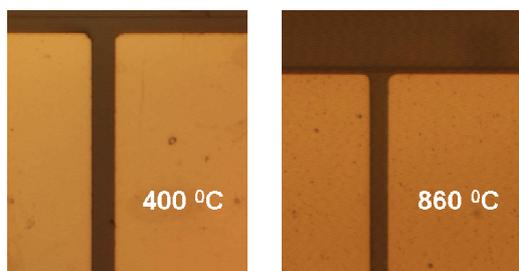


Figure 4 Optical images of annealed contacts at 400 °C (2.3 nm) and 860 °C (5 nm).

with low mobilities ($\mu < 600 \text{ cm}^2/\text{Vs}$), a wide range of annealing temperatures was found to result in comparable contact resistances, $\sim 0.3 - 0.6 \text{ ohm}\cdot\text{mm}$. For example, a contact resistance of $0.36 \text{ ohm}\cdot\text{mm}$ was obtained on a 3 nm AlN/GaN sample with mobility of $300 \text{ cm}^2/\text{Vs}$ at an annealing temperature as high as $860 \text{ }^\circ\text{C}$ [7]. On the other hand, an annealing at $860 \text{ }^\circ\text{C}$ of a 3 nm AlN/GaN sample with mobility of $1000 \text{ cm}^2/\text{Vs}$ resulted in an open circuit. Using the optimal annealing temperature shown in Figure 2, the contact resistance was observed to increase with increasing carrier mobilities. This trend is presented in Figure 3 (upper), suggesting it is challenging to realize low contact resistances on high quality AlN/GaN heterostructures. We postulate this is largely due to the fact the 2DEG density in an AlN/GaN heterostructure is highly sensitive to the AlN thickness thus sensitive to the reaction between the metals and the AlN barrier during annealing. For an AlN/GaN heterostructure with the same nominal barrier thickness but low mobility, it is very possible that thin AlN

and thick AlN areas are interlaced on nanometer scale, as illustrated in Fig. 3 (lower). The thin AlN areas allow metals to penetrate easily during annealing and contact with the 2DEG existing underneath the neighbouring thick AlN areas. Further investigations are ongoing to understand the underlying ohmic contact formation mechanisms, thus improving the contact resistance to be $< 0.5 \text{ ohm}\cdot\text{mm}$.

Shown in Fig. 4 are the optical images of the annealed contacts. Smooth morphologies, comparable to the as-deposited contacts, were observed up to an annealing temperature of $\sim 860 \text{ }^\circ\text{C}$. The contacts annealed at higher temperatures are rougher, sometimes comparable to the conventional annealed contacts to AlGaIn/GaN HEMTs. The smooth surface obtained can be attributed to the low annealing temperatures or the short annealing time ($< 5 \text{ seconds}$) at relatively higher temperatures. This should alleviate concerns during e-beam lithographical definition of submicron gates, which are normally associated with the rough contacts formed onto conventional AlGaIn/GaN HEMTs. [10]

4 Conclusion

The formation of ohmic contacts to high quality ultra-thin AlN barrier AlN/GaN HEMT structures was investigated. A strong dependence of ohmic contact annealing conditions on the heterostructure quality and barrier thickness was observed: the annealing temperature decreases with decreasing barrier thickness and the higher the carrier mobility, the narrower the annealing window.

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References

- [1] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. DenBaars, and U. Mishra, *IEEE Electron Device Lett.* **27**, 13 (2006).
- [2] M. Higashiwaki, T. Mimura, and T. Matsui, *IEEE Device Lett.* **27**(9), 719 (2006).
- [3] E. Alekseev, A. Eisenbach, and D. Pavlidis, *IEE Electron. Lett.* **35**(24), 2145 (1999).
- [4] H. Kawai, M. Nakamura, and S. Imanaga, *IEE Electron. Lett.* **34**(6), 592 (1998).
- [5] S. Imanaga and H. Kawai, *Jpn. J. Appl. Phys.* **39**, 1678 (2000).
- [6] C. Yu and D. Jena, *Appl. Phys. Lett.* **90**, 182112 (2007).
- [7] H. Xing, D. Deen, Y. Cao, T. Zimmermann, P. Fay, and D. Jena, *ECS Transaction* **11** (2007).
- [8] T. Zimmermann, D. Deen, Y. Cao, J. Simon, N. Su, J. Zhang, J. Bean, P. Fay, D. Jena, and H. Xing, *ICNS 2007*, late news, Las Vegas.
- [9] D. Buttari, A. Chini, G. Meneghesso, E. Zanoni, S. Heikman, N. Zhang, L. Shen, R. Coffie, S.P. DenBaars, and U.K. Mishra, *IEEE Electron Device Lett.* **23**(2), 76 (2002).
- [10] A. Basu, F.M. Mohammed, S. Guo, B. Peres, and I. Adesida, *J. Vac. Sci. Technol. B* **24**(2), L16 (2006).