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# 4-NM AlN BARRIER ALL BINARY HFET WITH $SiN_x$ GATE DIELECTRIC

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Undoped AlN/GaN heterostructures, grown on sapphire by molecular beam epitaxy, exhibit very low sheet resistances, ~ 150 Ohm/sq, resulting from the 2-dimensional electron gas situated underneath a 4 nm thin AlN barrier. This extraordinarily low sheet resistance is a result of high carrier mobility and concentration (~ 1200 $cm^2$/Vs and ~ $3.5x10^{13}$ $cm^{-2}$ at room temperature), which is ~ 3 x smaller than that of the conventional AlGaN/GaN heterojunction field effect transistor (HFET) structures. Using a 5 nm $SiN_x$ deposited by plasma enhanced chemical vapor deposition as gate-dielectric, HFETs were fabricated using these all binary AlN/GaN heterostructures and the gate tunneling current was found to be efficiently suppressed. Output current densities of 1.7 A/mm and 2.1 A/mm, intrinsic transconductance of 455 mS/mm and 785 mS/mm, were achieved for 2 μm and 250 nm gate-length devices, respectively. Current gain cut-off frequency $f_T$ of 3.5 GHz and 60 GHz were measured on 2 μm and 250 nm gate-length devices, limited by the high ohmic contact resistance as well as the relatively long gate length in comparison to the electron mean free path under high electric fields.

## 1. Introduction

Aggressive downscaling of gate-lengths into the deep sub-micrometer range for high-frequency power-devices demands very thin barrier heterojunction field effect transistors (HFET) structures with a high 2-dimensional electron gas (2DEG) density.[1] To this end, we have explored all binary AlN/GaN heterostructures with a 2.3 nm - 4.0 nm thin AlN barrier grown by plasma-assisted molecular beam epitaxy (PAMBE).[2,3,4] Due to the strong polarization effects in the III-V nitride material system,[5] a 2DEG forms near the AlN/GaN interface with a sheet carrier density as high as $3.5x10^{13}$ $cm^{-2}$ and mobility as high as 1200 $cm^2$/Vs.[6] The resultant sheet-resistance is as low as 150 Ω/sq, among the lowest ever reported and ~ 3X smaller than that of the conventional AlGaN/GaN HFETs. Recently we have demonstrated the highest reported output current density of 2.3 A/mm and the highest intrinsic transconductance of 1 S/mm simultaneously,[7] based on similar AlN/GaN all binary heterostructures with, however, a rather poor $Al_2O_3$ gate dielectric deposited by electron beam evaporation. In this work we have employed a 5.0 nm thin $SiN_x$ as the gate dielectric (Fig. 1) deposited by plasma-enhanced chemical vapor

deposition (PECVD). This $SiN_x$ film was found to be uniform and dense thus gate leakage in these HFETs is successfully suppressed.

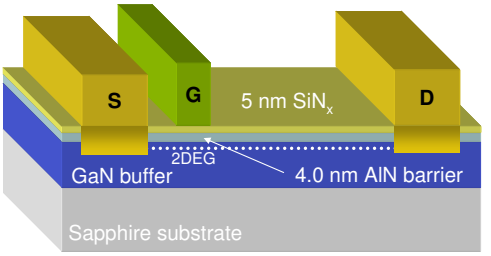


Fig. 1. Schematic cross-section of an AlN/GaN HFET with a 5.0 nm thin $SiN_x$ gate-dielectric on top of a 4.0 nm thin AlN barrier.

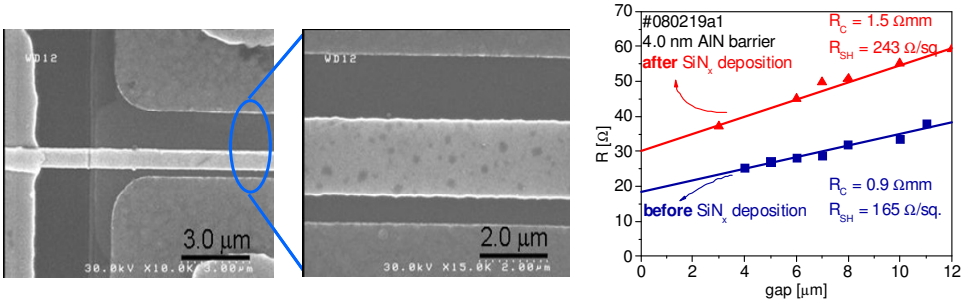


Fig. 2. (Left) SEM images showing smooth annealed ohmic contacts. Gate is the middle line. (Right) TLM measurements showing that the annealed ohmic contact resistance increased to 1.5 ohm-mm after $SiN_x$ deposition.

## 2. Experiments

The AlN/GaN heterostructures, consisting of a 4.0 nm undoped AlN barrier and a ~ 200 nm thick unintentionally doped (UID) GaN buffer layer, were grown on semi-insulating GaN-on-sapphire substrate in a Veeco 930 PAMBE system. The Hall effect measurements showed a 2DEG density of $3.5 \times 10^{13}$ $cm^{-2}$ with an electron mobility of 1185 $cm^2/Vs$ at room temperature. As a result, a very low sheet resistance of about 150 Ω/square was achieved, among the lowest ever reported for a single heterostructure. The details of the material growth and transport study have been reported elsewhere.[8] The device mesa (~ 110 nm) was first formed by a $Cl_2/BCl_3$ based reactive ion etch (RIE). The Ti/Al-based ohmic metal stack was then deposited by electron beam evaporation, followed by a rapid thermal annealing at 570°C resulting in contact resistances of 0.9 Ωmm. The more detailed study on ohmic contact formation to the ultrathin AlN/GaN structures can be found elsewhere.[9] Subsequently a 5 nm thin PECVD-$SiN_x$ layer was deposited and smooth surface morphology and complete coverage of $SiN_x$ was confirmed by atomic force microscopy with a rms-roughness of 0.446 nm. After a second deep mesa

etch (~ 250 nm) and a field-oxide deposition, Ni/Au gate metals were deposited on top of the $SiN_x$/AlN/GaN structure. Finally Ti/Au pads were deposited. Secondary electron microscopy (SEM) images (Fig. 2) show the ultrasmooth ohmic contacts, which in turn allows us to place the gate as close as possible to the source contacts. The transmission line method (TLM) measurements after the device completion showed an increase of contact resistances to be ~ 1.5 Ωmm (Fig. 2), which is currently ascribed to the plasma damage to the 2DEG during $SiN_x$ deposition.

## 3. Results and Discussion

A good rectifying behavior of the $SiN_x$-insulated gate-diode for all measured gate-lengths was observed and the current levels were in the range of μA/mm at an applied voltage in excess of 15 V. Thus, the gate-tunnel-current due to the thin AlN barrier was effectively suppressed by introducing the 5 nm $SiN_x$ layer. Fig. 3 shows the transfer curve of the drain output current and gate leakage current measured simultaneously on a 2 μm long device. A subthreshold slope of ~ 0.65 V/dec was also extracted (Fig. 3 inset), which is clearly limited by the relatively high buffer leakage current. The carrier concentration profile was extracted by C-V measurements, shown in the right of Fig. 3. A 2DEG is clearly observed at the AlN/GaN interface and a rather large number of charges can also be seen near the GaN regrowth interface, confirming the source of the high buffer leakage current observed in these devices.

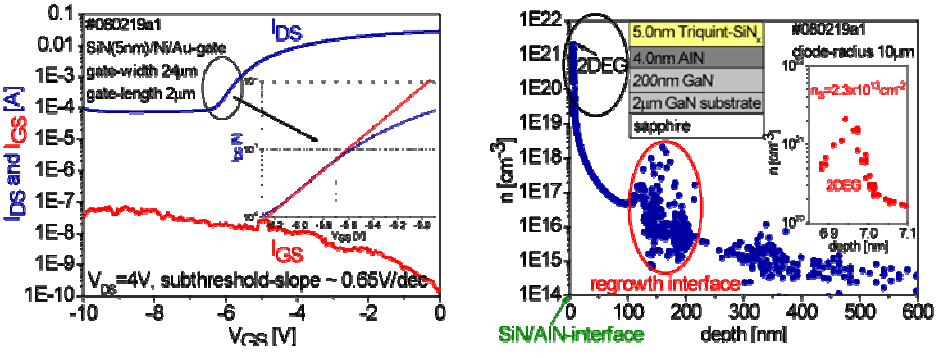


Fig. 3. (Left) Logarithmic plot of drain-output current and gate-leakage current vs. the gate-source voltage of a 2 μm gate-length FET device indicates the pinch-off current level is not limited by gate-leakage current. A high subthreshold slope of 0.65 V/dec and the low gate-leakage current point toward some parasitic contribution by the buffer (inset). (Right) Carrier concentration versus depth determined by CV measurements. A rather large number of charge was observed near the GaN regrowth interface.

Owing to the finite parallel conduction at the regrowth interface, a deep mesa etch was introduced to fully isolate devices from each other. Fig. 4 shows the family I-Vs of the 2 μm long gate HFET and the gate leakage current simultaneously measured. A maximum DC output current density of 1.7 A/mm was achieved. The contribution of the gate leakage current to the output current density is negligible since it is about three

orders of magnitude smaller than the output current. Furthermore, it can be seen from Fig. 3 that the contribution from the buffer leakage to the output current is about 100X smaller than the contribution from the 2DEG. Therefore, we can conclude that the output current of these devices indeed stem from the 2DEG at the AlN/GaN heterojunctions.

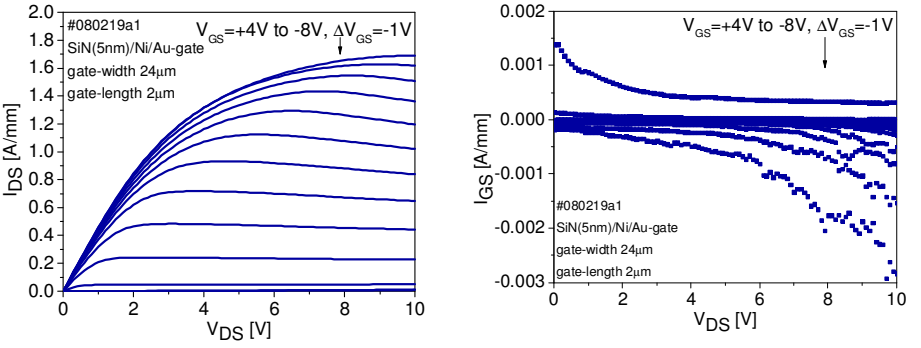


Fig. 4. (Left) DC output characteristics of a 2 µm gate-length HFET with a maximum output current density of 1.7 A/mm. (Right) The measured gate current leakage is three orders of magnitude smaller than the output current and does not contribute substantially to the output current level.

The same 2 µm gate-length device shows an extrinsic transconductance $g_{m,ext}$ of 270 mS/mm at $V_{DS}$=4V and the transfer-curve indicates a threshold voltage of -5.5 V (Fig. 5). Since the ohmic contact resistance $R_c$ is high in these devices, it is interesting to extract the intrinsic transconductance thus understanding the potential of these devices when the ohmic contact resistance can be sufficiently low. Using $R_c$=1.5 ohm-mm, $g_{m,int}$ of 455 mS/mm is extracted, which is among the highest reported in AlGaN/GaN based HFETs with 2 µm gate length.

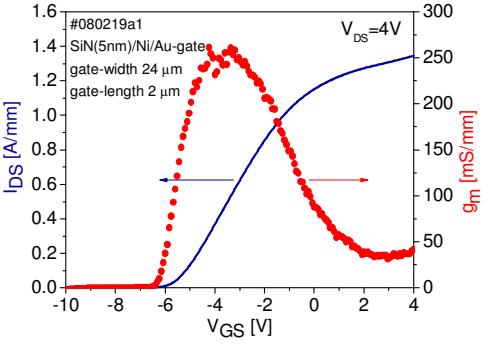


Fig. 5. Transfer-characteristic and transconductance of a 2 µm gate-length HFET showing a maximum $g_{m,ext}$ of 270 mS/mm (corresponding to $g_{m,int}$ of 455 mS/mm).

HFETs with gate-length of 250 nm were also characterized, showing a DC output current of ~ 2.1 A/mm and an extrinsic transconductance of ~ 360 mS/mm (corresponding to $g_{m,int}$ = 785 mS/mm), comparable to what we have reported previously [Ref.7]. Shown in Fig.6 are the small signal characteristics of 250 nm gate devices, measured using an Agilent 8722D network analyzer. A maximal current cutoff frequency $f_T$ of 46 GHz and a power cutoff frequency $f_{max(MAG)}$ of 50 GHz were determined. After de-embedding to remove the influence of the parasitic pad capacitances, a marginal increase in the cutoff frequency was observed, e.g. $f_T$ increased to 60 GHz.

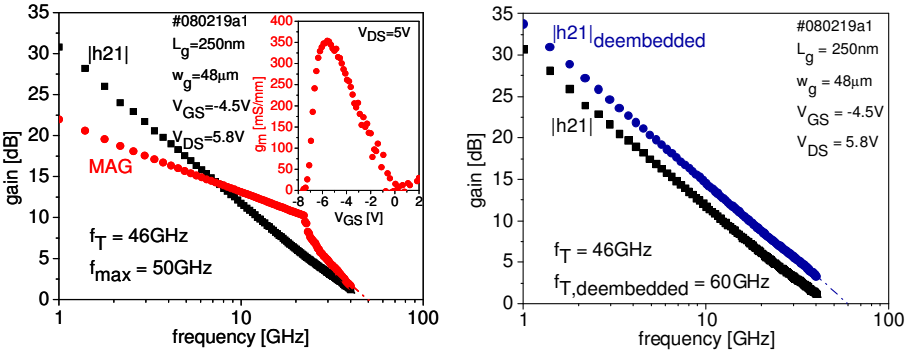


Fig. 6. (Left) Current cutoff frequency $f_T$ of 46 GHz and power cutoff frequency $f_{max}$ of 50 GHz were measured for a 250 nm gate-length FFET with $g_m$ of 360 mS/mm. (Right) After de-embedding $f_T$ of 60 GHz was extracted.

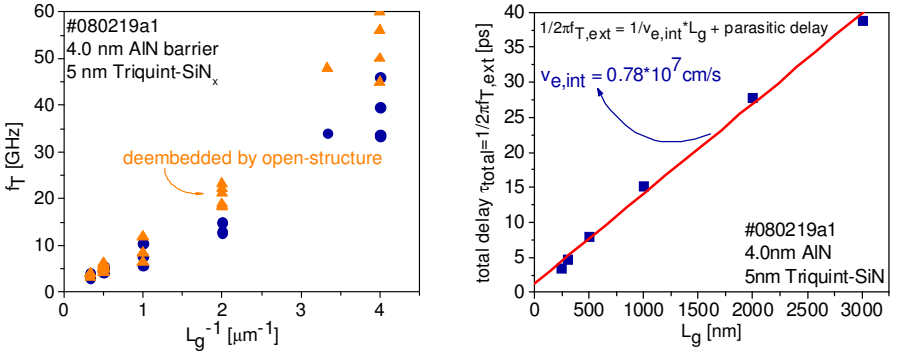


Fig. 7. (Left) As-measured and de-embedded values of $f_T$ versus HFET gate-length (250 nm – 3 µm). (Right) An average electron velocity of ~ 0.78 x $10^7$ cm/s extracted from the deembedded $f_T$ values assuming the parasitic delay is the same for all devices.

The as-measured and de-embedded current cutoff frequency values are summarized in Fig. 7 with respect to the gate length. Assuming the contribution of parasitic elements to the total time delay is the same for all HFETs with various gate lengths, it is found that

the average electron velocity is ~ 0.78 x $10^7$ cm/s. This assumption is a reasonable one since all $f_T$'s were measured under a similar bias condition. Jessen[10] et al. analyzed a variety of AlGaN/GaN HEMTs without back barriers and proposed a minimal aspect ratio $L_g/t_{bar}$ of 15 to mitigate the short channel effects, with $L_g$ being the metallurgical gate length and $t_{bar}$ the barrier thickness. For the devices investigated in this study, this aspect ratio value ranges from 27 to 222. Since it is much larger than 15, short channel effects are not considered here. The relatively low average electron velocity stems from the same roots why it is low in majority of the GaN-based HFETs. The high ohmic contact resistances in these devices substantially lowered the current gain, resulting in low cutoff frequencies. It has been long argued that the optical phonon emission rate is very high in GaN, e.g. ~ 10X higher than that in GaAs, while the optical phonon decay time or lifetime is comparable in GaN and GaAs.[11] As a result, it is very difficult to achieve the velocity overshoot in GaN that is commonly observed in GaAs or InP based devices. For instance, the simulation results have indicated that a gate length of ~ 25 nm is necessary to obtain velocity overshoot in GaN.[12] In order to take the full advantage of the ultrathin AlN barrier HFETs, it is necessary to fabricate devices with gate length < 50 nm with access resistance < 0.5 ohm-mm. Furthermore, a recent study[13] on $SiN_x$ gate dielectric in AlGaN/GaN HFETs showed that $SiN_x$ deposited by catalytic CVD resulted in the lowest gate leakage in comparison to that deposited by metalorganic CVD as well as PECVD, thanks for the low substrate temperature with no plasma employed in catalytic CVD technique; and that a thin layer of $SiN_x$ deposited by all techniques show the similar amount of surface barrier lowering. Atomic layer deposition $HfO_2$ has also been reported to be promising as gate dielectric in GaN-based FETs. The future ultrascaled FETs critically depend on the development of robust gate stack, short-channel effect minimization and surface passivation schemes, so do GaN-based ones.

## 4. Conclusion

HFETs based on undoped AlN/GaN heterostructures with a 4 nm thin AlN barrier were fabricated using a 5 nm $SiN_x$ deposited by PECVD as gate dielectric. The extraordinarily high concentration and mobility of the 2-dimensional electron gas led to record low sheet resistances. As a result, output current densities of 1.7 A/mm and 2.1 A/mm, intrinsic transconductance of 455 mS/mm and 785 mS/mm, were achieved for 2 μm and 250 nm gate-length devices, respectively. Current gain cut-off frequency $f_T$ of 3.5 GHz and 60 GHz were measured on 2 μm and 250 nm gate-length devices, limited by the high ohmic contact resistance as well as the relatively long gate length in comparison to the electron mean free path under high electric fields.

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## References

[1] H. Xing, T. Zimmermann, D. Deen, Y. Cao, D. Jena and P. Fay. "*Ultrathin AlN/GaN heterostructure based HEMTs*". International Conference on Compound Semiconductor Manufacturing Technology (CS ManTech), Chicago, (April 2008)

[2] H. Xing, D. Deen, Y. Cao, T. Zimmermann, P. Fay and D. Jena. "*MBE-grown ultra-shallow AlN/GaN HFET technology*". ECS Transactions, Vol. 11, 2007.

[3] David Deen, Tom Zimmermann, Yu Cao, Debdeep Jena and Huili Grace Xing. *"2.3 nm AlN/GaN high electron mobility transistors with insulated gates"*. Phys. Solid. Stat. (c), 5(6), 2047 (2008)

[4] Tom Zimmermann, David Deen, Yu Cao, Debdeep Jena and Huili Grace Xing. *"Formation of ohmic contacts to ultra-thin channel AlN/GaN HEMTs"*. Phys. Solid. Stat. (c), 5(6), 2030 (2008)

[5] C. Wood and D. Jena. Polarization Effects in Semiconductors: From Ab Initio Theory to Device Application. Berlin, Germany: Springer-Verlag, 2007, p.522.

[6] Yu Cao, Alexei Orlov, Huili Grace Xing, and Debdeep Jena. "Very low sheet resistance and Shubnikov-de-Haas oscillations in two dimensional electron gas at ultrathin binary AlN/GaN heterojunctions". Appl. Phys. Lett. 92(15), 152112 (2008)

[7] Tom Zimmermann, David Deen, Yu Cao, John Simon, Patrick Fay, Debdeep Jena and Huili Grace Xing. *"AlN/GaN insulated gate HEMTs with 2.3 A/mm output current and 480 mS/mm transconductance"*. IEEE EDL 29(7), 661, 2008.

[8] Yu Cao and Debdeep Jena. "High-mobility window for two-dimensional electron gases at ultrathin AlN/GaN heterojunctions". Appl. Phys. Lett., 90(18), 182112 (2007).

[9] Tom Zimmermann, David Deen, Yu Cao, Debdeep Jena and Huili Grace Xing. *"Ohmic contacts to thin AlN barrier all-binary heterostructures"*. Submitted to J. Electron. Mat., 2008

[10] Gregg H. Jessen, Robert C. Fitch Jr., James K. Gillespie, Glen Via, Antonio Crespo, Derrick Langley, Daniel J. Denninghoff, Manuel Trejo Jr. and Eric R. Heller. "*Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices*". IEEE Trans. Electr. Dev. 2589, 2007.

[11] Kejia Wang, John Simon, Niti Goel and Debdeep Jena. *"Optical study of hot-electron transport in GaN: Signatures of the hot-phonon effect"*. Appl. Phys. Lett., 88, 022103, 2006.

[12] B. E. Foutz, S. K. O'Leary, M. S. Shur and L. F. Eastman. *"Transient electron transport in wurtzite GaN, InN and AlN"*. J. Appl. Phys., 85, 7727 (1999).

[13] Masataka Higashiwaki, Zhen Chen, Yi Pei, Rongming Chu, Stacia Keller, Nobumitsu Hirose, Takashi Mimura, Toshiaki Matsui, and Umesh K. Mishra. *"A comparative study of SiN deposition methods for millimeter-wave AlGaN/GaN HFETs"*, IEEE Device Research Conference technical digest, p.207, Santa Barbara, June 2008