Gate-Recessed Enhancement-Mode InAlN/AlN/GaN HEMTs With 1.9-A/mm Drain Current Density and 800-mS/mm Transconductance

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***Abstract*—Having a drain current density of 1.9 A/mm, a peak extrinsic transconductance of 800 mS/mm (the highest reported in III–nitride transistors), $f_t/f_{\max}$ of 70/105 GHz, and $V_{\rm br}$ of 29 V, 150-nm-gate enhancement-mode InAlN/AlN/GaN high-electron-mobility transistors are demonstrated on SiC substrates using plasma-based gate-recess etch. The possible plasma-induced damage in the gate region was investigated using interface-trap states extracted from temperature-dependent subthreshold slopes.**

***Index Terms*—Enhancement mode (E-mode), HFET, high-electron-mobility transistor (HEMT), InAlN, interface state, subthreshold slope.**

I. Introduction

LATTICE-MATCHED InAlN-barrier GaN high-electron-mobility transistors (HEMTs) have attracted a lot of attention recently due to their demonstrated superior thermal stability [1] and high drain current density [2]. Similar to ultrathin barrier AlN/GaN (2–5 nm) heterostructures [3]–[6], very high 2-D electron gas (2DEG) densities can be induced in thin-barrier ($>$ 3 nm) InAlN/GaN heterostructures. With the insertion of an AlN interlayer (1–3 nm), high 2DEG mobility in InAlN heterostructures can be realized as well, exceeding 1000 $\rm cm^2/V\cdot s$, by reducing alloy scattering and interface roughness [7]. Alternatively, InAlN/AlN/GaN HEMTs can be viewed as AlN/GaN HEMTs with a thermally stable and lattice-matched cap that can be grown very thick, also providing a high 2DEG density in comparison with GaN/AlN/GaN heterostructures [8]. We have demonstrated that subcritical-thickness barrier AlN/GaN heterostructures can be utilized for enhancement-mode (E-mode) operation by selectively depositing 2DEG-inducing capping materials [9]. In this letter, we report E-mode operation of InAlN/AlN/GaN HEMTs with subcritical AlN barrier ($\sim$1 nm) selectively etching away InAlN in the gate region. The devices demonstrate a high drain current density of 1.9 A/mm and a record extrinsic transconductance of 800 mS/mm. Given the extremely thin AlN barrier underneath the gate, these structures are promising candidates for highly scaled HEMTs.

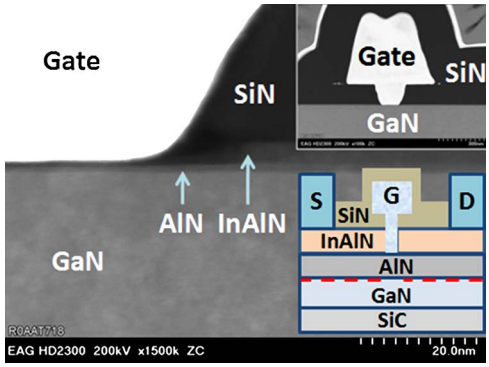

Fig. 1. TEM images of the recessed T-gate with SiN passivation, showing the gate recess stopped at AlN. Lower inset: Schematic of the gate-recessed E-mode InAlN/AlN/GaN HEMT structure.

II. Experiments

The InAlN/AlN/GaN HEMT structure (Fig. 1 inset) consists of a 4.8-nm InAlN barrier, a 1-nm AlN spacer, an unintentionally doped GaN channel, and a Fe-doped GaN semiinsulating buffer on SiC substrate, grown by metal–organic chemical vapor deposition at IQE RF LLC. The 2DEG concentration and mobility were measured to be $\sim 2\times 10^{13}$ $\rm cm^{-2}$ and $\sim$1160 $\rm cm^2/V\cdot s$, respectively, leading to a sheet resistance of $\sim$270 Ω/sq in the as-grown heterostructure. The devices were fabricated using standard processing for AlGaN/GaN HEMTs, except for the gate recess, at Triquint Semiconductor, Inc. The unoptimized Ti-based alloyed ohmic-contact scheme resulted in a contact resistance of $\sim 0.6\ \Omega\cdot$ mm, obtained from transmission-line measurement.

The gate recess was realized by a BCl_3-based reactive-ion-etching process after etching the top SiN passivation using F-based plasma. The transmission electron microscopy (TEM) images shown in Fig. 1 confirmed that the InAlN barrier was removed and the recess etch stopped at AlN. Electron-beam lithography was used to define 150-nm-long gates with varying gate widths, followed by the Pt/Au gate-metal

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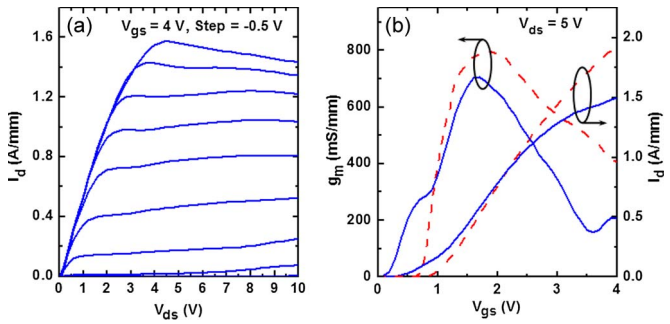

Fig. 2. (a) Representative dc family I–Vs and (b) transfer curve ($W_g = 2 \times 75$ μm, in solid blue) as well as a transfer curve ($W_g = 2 \times 50$ μm, in dashed red), showing the highest drain current density and extrinsic transconductance of gate-recessed E-mode InAlN HEMTs on the wafer.

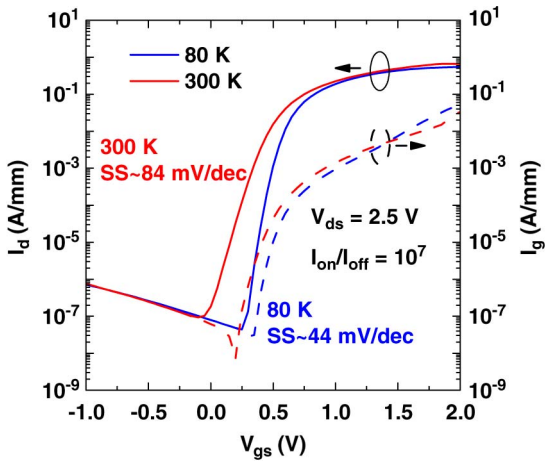

Fig. 3. Transfer curves of an InAlN E-mode HEMT at 80 and 300 K.

deposition. The barrier height of Pt/AlN is expected to be 3 eV or higher based on their work-function difference. The source–drain distance was 2 μm. The devices were passivated with 140-nm and 200-nm SiN prior to and after gate definition, respectively. Temperature-dependent field-effect measurements were performed over the range of 80–300 K on a Lakeshore cryogenic probe station using a Keithley 4200 semiconductor characterization system.

III. Results and Discussion

Representative dc family I–Vs and transfer curves of the InAlN/AlN/GaN HEMTs are shown in Fig. 2 (blue solid lines). Also shown is the device transfer curve showing a maximum drain current density of 1.9 A/mm with a peak extrinsic transconductance of 800 mS/mm (red dashed lines), the highest measured on this wafer. The conservative estimate of the intrinsic transconductance using $R_s = R_c = 0.6\ \Omega \cdot$ mm is therefore $\sim$1.5 S/mm; both the extrinsic and intrinsic tranconductances are the highest reported values for any GaN-based transistors, to the best of our knowledge. The pinchoff voltage $V_{\rm po}$ is in the range of 0.2–0.8 V from the linear extrapolation of g_m to zero or 0.4–1.0 V as extracted from the linear extrapolation of I_d, showing that these gate-recessed devices are E-mode. The variation observed in the device performance is attributed to nonuniformity in the epitaxial material and processing.

The drain-induced barrier lowering (DIBL) over a drain-bias range of 0.1 to 6 V was measured to be $\sim$100 mV/V, which is comparable with the reported value for AlGaN/GaN HEMTs with a 0.6-μm gate length [10]. The low DIBL value, along with the low output conductance, indicates that short-channel effect is minimal for these 150-nm-gate-length HEMTs owing to the very thin barrier ($\sim$1 nm) upon the gate recess. Small-signal RF measurements show that these devices have $f_t/f_{\rm max}$ in the range of $\sim$65–70 GHz/100–105 GHz (without deembedding), respectively. The three-terminal device breakdown voltage was measured to be 29 V at $I_d = 1$ mA/mm and $V_{\rm gs} = (V_{\rm po} - 1)$ V. The wider recess in InAlN as revealed in the TEM image (Fig. 1) may play a role in the device breakdown and f_t, which is under further investigation.

To understand the quality of the thin AlN barrier underneath the gate, both C–V and transfer I–V measurements were taken by sweeping from negative to positive $V_{\rm gs}$ and back, and no apparent hysteresis was observed. However, knee walkout was observed in pulsed I–V measurements, indicating the existence of traps, possibly both under the gate and near the gate toward the drain. The conductance method was then attempted to extract the interface-trap density $D_{\rm it}$. Unfortunately, no conductance peaks could be resolved over the frequency range of 10 kHz–1 MHz. The temperature dependence of the subthreshold slope (SS) was then employed to extract the $D_{\rm it}$ distribution in the bandgap. Furthermore, for switching applications, the subthreshold slope is an important parameter since low SS values represent excellent gate pinchoff ability and low power consumption at the OFF state.

Shown in Fig. 3 are the temperature-dependent transfer curves along with the gate current. In spite of the very thin barrier, a high $I_{\rm on}/I_{\rm off}$ ratio of 10^7 was measured over the bias range and temperature range in this letter. The SS values of 44 mV/dec at 80 K and 84 mV/dec at 300 K were extracted at the steepest point of the I_d–$V_{\rm gs}$ transfer curves at $V_{\rm ds} = 2.5$ V ($V_{\rm gs} = 0.35$ V for 80 K and 0.15 V for 300 K). The gate current was also found to be largely the same in the temperature range studied. This temperature independence suggests that the gate current is dominated by tunneling processes.

The subthreshold slope can be expressed in terms of the barrier capacitance C_b, the quantum capacitance C_q, and the interface-trap capacitance $C_{\rm it}$ as follows:

$$SS = \left(1 + \frac{C_q + C_{\rm it}}{C_b}\right) \frac{k_B T}{q} \ln 10. \quad (1)$$

In the deep subthreshold region, the quantum capacitance C_q, although finite at $T > 0$ K owing to the Fermi–Dirac distribution, is three to four orders of magnitude smaller than C_b, i.e., few electrons are present in the channel. As a result, one can extract $C_{\rm it}$ and the interface-trap density $D_{\rm it}$ by neglecting C_q. As shown in Fig. 4, the subthreshold slope shows linear temperature dependence from 80 to 300 K, which is consistently $\sim$25 mV/dec higher than the theoretical limit (60 mV/dec at 300 K). This linear dependence corresponds to an exponential decrease of the extracted $D_{\rm it}$ with increasing temperature, which, in turn, as shown next, corresponds to an exponential $D_{\rm it}$ distribution in the bandgap ($D_{\rm it}$ being higher closer to the

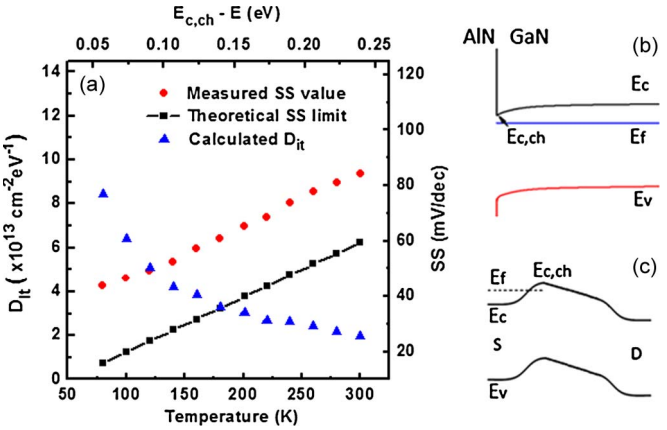

Fig. 4. (a) Temperature-dependent subthreshold slopes and the extracted interface-trap distribution; schematic band diagram in the subthreshold region (b) from the gate to GaN buffer, and (c) from the source to drain at $V_{\rm ds} = 2.5$ V.

conduction-band edge E_c). Similar $D_{\rm it}$ distributions have been commonly observed in other semiconductors [11].

Shown in Fig. 4(b) and (c) are the schematic band diagrams from the gate to GaN buffer and from the source to drain under the bias condition where $D_{\rm it}$ is extracted. Since the extracted $D_{\rm it}$ measures the local interface state density near the Fermi level E_f, one needs to relate the bias condition (I_d or $V_{\rm gs}$) to $E_c - E_f$. Assuming a Boltzmann distribution and single subband occupation in the channel, the effective barrier height between the Fermi level and the channel conduction-band edge $E_{c,\rm ch} - E_f$ can be written as a function of the channel carrier density N_s at the source side

$$E_{c,\rm ch} - E_f \approx -k_B T \cdot \ln\left[\exp\left(\frac{N_s \pi \hbar^2}{k_B T \cdot m^*}\right) - 1\right] \quad (2)$$

where m^* is the electron effective mass in GaN. In the subthreshold region, one can estimate the channel carrier density N_s using a diffusion-current model

$$I_d = qD_n \cdot \frac{dN_s}{dx} \approx k_B T \mu \frac{N_s}{L_g} \quad (3)$$

where D_n is the electron diffusion coefficient, μ is the electron mobility, and L_g is the gate length. Assuming a constant mobility of 1000 $\rm cm^2/V \cdot s$ based on a self-consistent model [12], the extracted N_s is $\sim 10^8$ $\rm cm^{-2}$, and $D_{\rm it}$ versus $E_{c,\rm ch} - E_f$ can be plotted in Fig. 4 following (2) and (3). At 80 K, $D_{\rm it}$ is estimated to be $\sim 8.4 \times 10^{13}$ $\rm cm^{-2}eV^{-1}$ near 55 meV below E_c; at 300 K, $D_{\rm it} \sim 1.9 \times 10^{13}$ $\rm cm^{-2}eV^{-1}$ near 240 meV below E_c.

The validity of the single-band-occupation assumption is also checked by the Poisson–Schrödinger self-consistent simulations: It is found that a confined energy state exists with N_s as low as $\sim 10^8$ $\rm cm^{-2}$. Therefore, it is reasonable to use the 2-D density-of-states in the aforementioned calculation. The extracted $D_{\rm it}$ at 300 K is ~2–10 times higher than the reported values in nonrecessed AlGaN HEMTs [10], indicating that the gate-recess process has most likely increased $D_{\rm it}$. The SS value can also be adversely affected by the gate leakage, thus leading to an artificially high extracted $D_{\rm it}$ [13]. In this letter, even though the $I_{\rm on}/I_{\rm off}$ ratio is among the highest reported values, $D_{\rm it}$ may still be overestimated. More systematic studies are currently underway to understand the nature of the gate-recess selectivity, resultant gate diodes, and $D_{\rm it}$.

IV. Conclusion

Gate-recessed E-mode InAlN/AlN/GaN HEMTs with subcritical AlN barrier (~1 nm) have been demonstrated with record high transconductance and drain current density. The interface-state density and its distribution are extracted from the temperature-dependent subthreshold slope. The relatively high $D_{\rm it}$ suggests that the gate recess has likely introduced damage, but despite this, the overall device performance is extremely promising for ultrascaled GaN transistors and integrated E-/D-mode circuits.

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