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Si-Containing Recessed Ohmic Contacts and 210 GHz Quaternary Barrier InAlGaN High-Electron-Mobility Transistors

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The effects of recess etch in alloyed ohmic contacts have been studied on InAl(Ga)N/AlN/GaN high-electron-mobility transistors (HEMTs) using a Si-containing ohmic metal stack. The optimized contact resistance is as low as 0.23 Ω mm. With decent ohmic contacts, an $In_{0.13}Al_{0.83}Ga_{0.04}N$ barrier HEMT with a 66-nm long gate and dielectric-free passivation followed by a 5 nm Al_2O_3 deposition, shows a maximum drain current density $I_{d,max}$ of 2.3 A/mm, a peak extrinsic transconductance $g_{m,ext}$ of 560 mS/mm and a current gain cut-off frequency f_T of 210 GHz, which are among the highest reported values in quaternary InAlGaN/AlN/GaN HEMTs. © 2011 The Japan Society of Applied Physics

GaN-based high-electron-mobility transistors (HEMTs) have shown excellent performance in high-power and high-temperature applications operating at microwave frequencies. Both AlN/GaN and InAl(Ga)N/AlN/GaN heterostructures have been employed for high-speed HEMTs since they offer ultrathin barriers and high channel charges simultaneously.[1–9] However, it is challenging to obtain alloyed ohmics with low contact resistance R_c on wide-bandgap semiconductors, particularly AlN with a bandgap of 6.2 eV.[10] Though ohmic regrowth by molecular beam epitaxy has been demonstrated to produce $R_c < 0.1\,\Omega$ mm,[2] it is more practical to develop an alloyed ohmic process with reasonably low contact resistance. Both ohmic recess etch[11] and Si-containing ohmic stacks[12] were previously reported to effectively minimize the alloyed ohmic contact resistance in AlGaN/GaN HEMTs. In this work, effects of ohmic recess etch using a Si-containing ohmic metal stack have been investigated on $In_{0.17}Al_{0.83}N$ and $In_{0.13}Al_{0.83}Ga_{0.04}N$ HEMTs with an AlN barrier interlayer of 1 nm thick; high-speed InAlGaN HEMTs with $f_T > 200$ GHz were then demonstrated with a low contact resistance.

The $In_{0.17}Al_{0.83}N$ (4.7 nm)/AlN (1 nm)/GaN (lattice-matched, Wafer A) and $In_{0.13}Al_{0.83}Ga_{0.04}N$ (10.3 nm)/AlN (1 nm)/GaN (slightly tensile strained, Wafer B) heterostructures were grown on SiC by metal organic chemical vapor deposition (MOCVD) at IQE RF LLC and Kopin Corporation, respectively. The ohmic stack was Si/Ti/Al/Ni/Au (2/20/100/40/50 nm) deposited by electron-beam (e-beam) evaporation and annealed in N_2 for 0–30 s. The ohmic recess was achieved using a chlorine-based reactive ion etching with a rate of ~5 nm/min. R_c is extracted using the transmission line method (TLM). The InAlGaN HEMT device has an e-beam-lithography-defined rectangular gate, with a gate length L_g of 66 nm, a gate width W_g of 2×50 µm, a source drain distance L_{sd} of 1.6 µm, and a source gate distance L_{sg} of 300 nm. After gate definition, the device was first treated with a dielectric-free passivation (DFP) scheme, which is an O_2-containing plasma treatment in the access region,[7,8] followed by another 5 nm Al_2O_3 using atomic layer deposition (ALD).

Presented in Fig. 1 is R_c obtained using systematically varied ohmic recess etch depths and annealing temperatures. For thin InAlN samples (Wafer A, ~6 nm barrier thickness in total), the ohmic recess depths are 0, 3, 7, and 15 nm for A-1 to A-4, respectively. For thicker InAlGaN samples (Wafer B, ~11 nm barrier thickness in total), the ohmic recess depths are 0 and 6 nm in B-1 and B-2, respectively. The annealing temperature was varied for each structure with a constant annealing time: 15 s for Wafer A samples and 18 s for Wafer B samples. For all the samples, R_c shows a minimal value with respect to the annealing temperature. For Wafer A samples, no clear trend that the ohmic recess may result in a lower R_c is observed; when the entire barrier was etched away (A-4), R_c became higher than those obtained in A-1 to A-3. This suggests that the alloyed sidewall contact is not as good as that with a partially recessed barrier. For Wafer B samples, it is observed that the recessed devices have a 30% lower R_c than non-recessed ones, indicating that the ohmic recess is able to improve R_c in heterostructures with thick barriers.

Figure 1(b) shows the linearly fitted R_c and R_{sh} from TLM of InAlGaN HEMTs annealed at 860 °C for 18 s, before and after a 20 nm SiN passivation by plasma enhanced CVD (PECVD). After passivation, R_{sh} drops from 220 to 190 Ω/sq, consistent with the Hall effect measurement results: $R_{sh} = 227\,\Omega/\text{sq}$, $n_s = 1.5 \times 10^{13}\,\text{cm}^{-2}$, and $\mu = 1900\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ before passivation; $R_{sh} = 190\,\Omega/\text{sq}$, $n_s = 1.8 \times 10^{13}\,\text{cm}^{-2}$, and $\mu = 1790\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ after passivation.[8] The surface barrier height lowering by SiN is currently ascribed to the increase in n_s, explained using a surface donor model.[13,14] R_c is also found to increase from 0.17 to 0.23 Ω mm after SiN passivation, which is, nevertheless, among the lowest reported value of alloyed ohmics in GaN-based HEMTs. The increase of R_c might be due to a reduced contact transfer length as a result of increased n_s near the metal contact and channel interface. Since high-performance GaN-based HEMTs are generally passivated and an important signature of surface state passivation is the associated increase of n_s, all R_c values shown in Fig. 1(a) were obtained after SiN passivation.

Cross-sectional scanning transmission electron microscopy (STEM) images and electron dispersion spectroscopy (EDS) scans were taken to study the microstructures in Sample B-2, as shown in Fig. 2(a). No apparent metal penetration into the GaN buffer was observed even though a ~6 nm InAlGaN barrier was recessed away, thus leaving a

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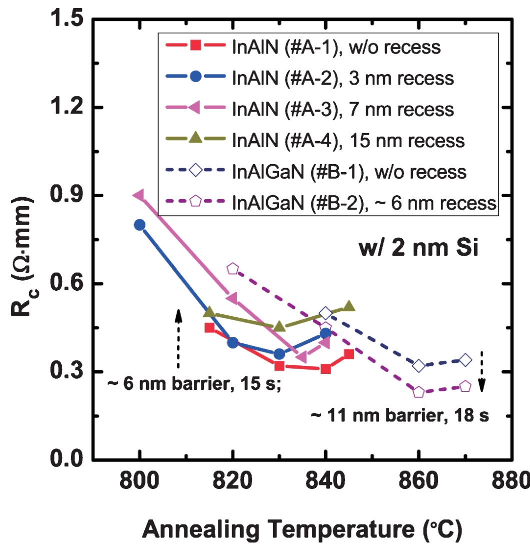
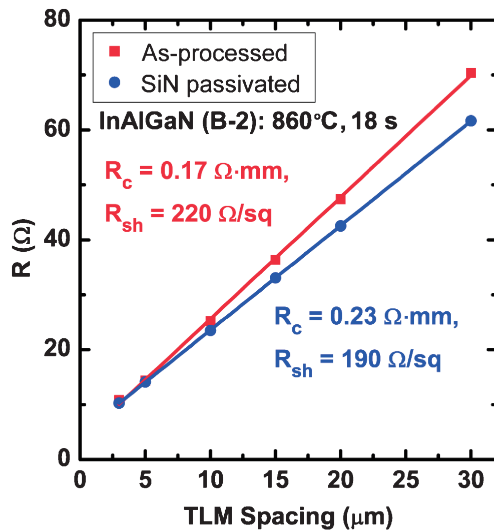
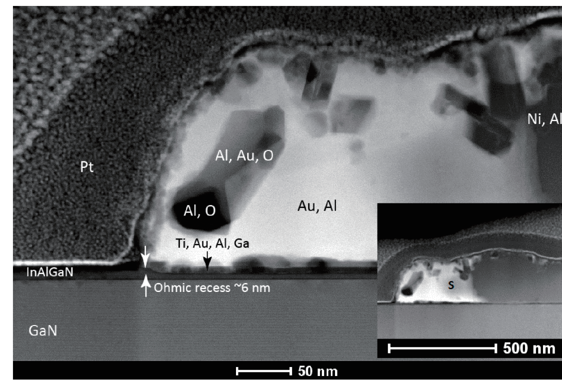


(a)

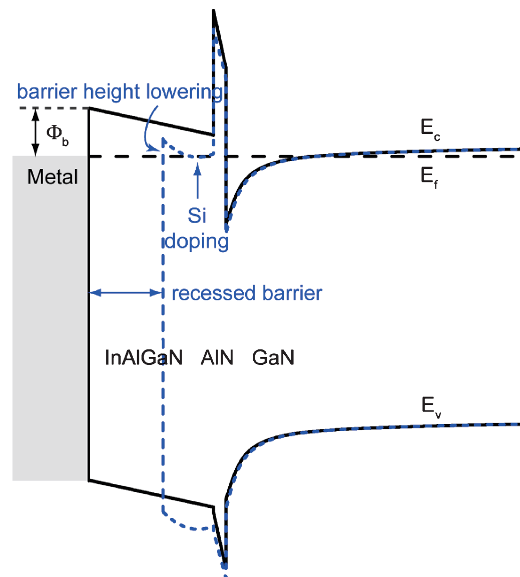


(b)

Fig. 1. (a) R_c as a function of the annealing temperature and recess etch depth in InAl(Ga)N HEMTs (b) TLM results of InAlGaN HEMTs (Sample B-2) showing the effect of passivation on R_c extraction.



(a)



(b)

Fig. 2. (a) Cross-sectional STEM image of alloyed ohmics with recess etch in InAlGaN HEMTs ($R_c = 0.23\,\Omega$ mm), in which Pt was deposited during the STEM sample preparation; element distribution within the alloyed metal stack was determined by EDS; inset: zoomed-out view. (b) A possible band diagram of the alloyed Si-containing ohmic contact with recess etch.

total barrier of ~5 nm. EDS analysis of the alloyed microstructures indicates that both Au and Ni diffused to form alloys with Al, and Ti stayed on the bottom; a small amount of O may be incorporated during the metal evaporation and alloying. The ohmic contact to the channel is thus speculated via tunneling through the remaining barrier with a possible band diagram shown in Fig. 2(b). The high tunneling probability is facilitated by a favorably small barrier between the low work-function Ti–Al–N or silicide alloys[12] and InAlGaN and/or defect-assisted tunneling. Si, which could not be discerned in TEM, may diffuse in as donors in III–nitrides during the high-temperature annealing, and a diffusion depth of 3–4 nm is expected at 860 °C for 18 s;[15] moreover, silicide formation[12] and the surface barrier height lowering by Si on GaN-based HEMTs[13,14] may also contribute to the observed low ohmic resistance. The ultimate tunneling probability should be limited by the 1 nm AlN in the HEMT structure. This observation is different from the commonly reported metal spiking through dislocations to form ohmic contacts in AlGaN HEMTs.[12] Nonetheless, a few other groups have also reported decent R_c values with no metal protruding through the HEMT barrier when alloyed at temperatures in excess of 800 °C, as evidenced by TEM.[16,17]

Shown in Fig. 3 are the common-source family of I–Vs and transfer characteristics of an InAlGaN HEMT with $R_c = 0.36\,\Omega$ mm. The device has an on-resistance R_{on} of 1.1 Ω mm and a maximum output current density I_d of 2.2 A/mm at $V_{gs} = 1$ V. The large output conductance arises from strong short-channel effects. The transfer curve measured at $V_{ds} = 6$ V gives $I_{d,max} = 2.3$ A/mm at $V_{gs} = 3$ V, a peak extrinsic transconductance $g_{m,ext} = 560$ mS/mm and an estimated intrinsic transconductance $g_{m,int} = 730$ mS/mm. Small-signal RF measurement was taken using an Agilent E8361C network analyzer with on-wafer open-pad deembedding. The current gain and unilateral power gain cut-off frequencies f_T/f_{max} are determined to be 210/52 GHz

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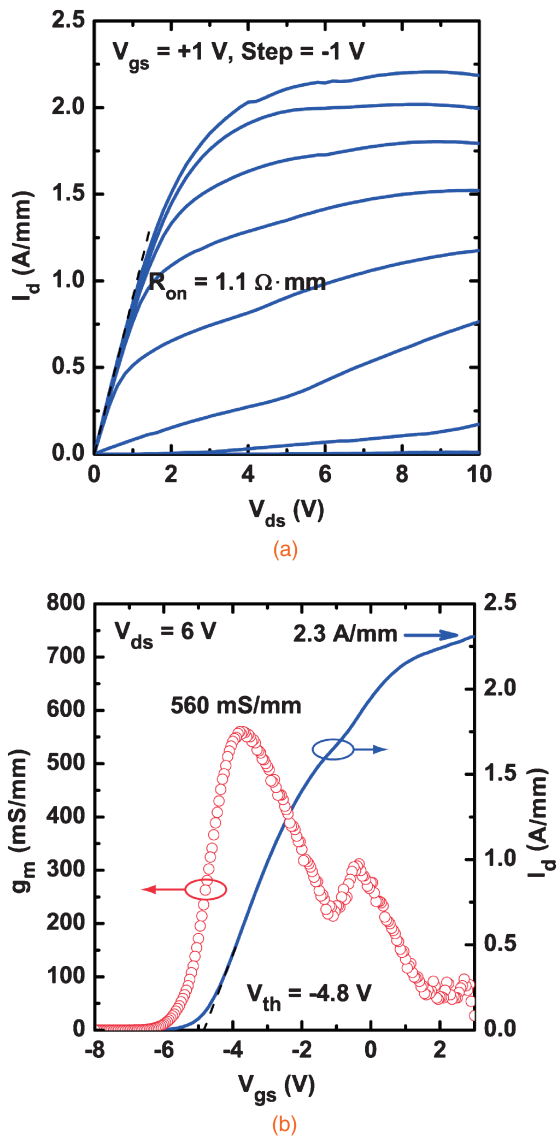

Fig. 3. Quaternary barrier InAlGaN HEMT performance: (a) common-source family of I–Vs showing $R_{on} = 1.1\,\Omega\,\text{mm}$ (b) transfer characteristics indicating $I_{d,max} = 2.3\,\text{A/mm}$ and $g_{m,ext} = 560\,\text{mS/mm}$.

at $V_{ds} = 4.4\,\text{V}$ and $V_{gs} = -3.7\,\text{V}$, and the pre-deembedded values are 142/48 GHz. The 5–10% drops in f_T and f_{max}, compared with the values prior to Al_2O_3 deposition,[8] stem from the increased parasitic capacitance because of the dielectric deposition. These values of $g_{m,ext}$ and f_T/f_{max} are among the highest reported in GaN-based HEMTs with a barrier under the gate thicker than 10 nm. Following the scaling trend in ref. 18, $f_T > 250\,\text{GHz}$ is achievable with a sub-50-nm gate length or higher after adopting back barriers to mitigate short-channel effects.

In conclusion, the impacts of ohmic recess etch and annealing temperature on alloyed contacts in InAl(Ga)N HEMTs were studied. An alloyed contact resistance as low as $0.23\,\Omega\,\text{mm}$ was achieved in quaternary barrier InAlGaN HEMTs. The state-of-the-art device performance with $I_{d,max} = 2.3\,\text{A/mm}$, $g_{m,ext} = 560\,\text{mS/mm}$, and $f_T = 210\,\text{GHz}$ was demonstrated with these recessed alloyed ohmics.

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