

The Resurgence of III-N Materials Development: AlInN HEMTs and GaN-on-Si

O. Laboutin^a, Y. Cao^a, R. Wang^b, G. Li^b, D. Jena^b, H. Xing^b, C.-F. Lo^c, L. Liu^c,
S.J. Pearton^d, F. Ren^c, and W. Johnson^a

^a Kopin Corporation, 200 John Hancock Rd., Taunton, MA 02780, USA

^b Dept. of Electrical Engineering, Univ. of Notre Dame, Notre Dame, IN 46556, USA

^c Dept. of Chemical Engineering, Univ. of Florida, Gainesville, FL 23611, USA

^d Dept. of Materials Science & Engineering, Univ. of Florida, Gainesville, FL 23611,
USA

Heterostructure devices based on the AlInN material system have demonstrated unprecedented high frequency performance but are still limited by materials issues. Likewise, improved crystal growth schemes are envisioned as a key component in the realization of GaN-on-Si high voltage devices for power electronics applications. This work presents materials optimization results from MOCVD growth of quaternary barrier AlInGaN/AlN/GaN HEMTs formed on sapphire and SiC substrates and also a study of AlN nucleation and subsequent GaN growth for crack-free films on silicon (111).

Introduction

The decade of the 2000s was an important one for wide bandgap materials development. Significant materials advances were fueled, in part, by government programs such as the DARPA Wide Bandgap Semiconductor Technology Initiative in the US. In the early part of the decade, the diameter of commercially available SiC substrates increased from 2" to 3" and ultimately reached 4" by the mid- to late-2000s. Transport properties, uniformity, and reproducibility of GaN epitaxial layers deposited on sapphire and SiC substrates were major areas of focus. By the latter part of the decade, most GaN-related development activities had transitioned away from materials and into areas of device and circuit design, reliability, and commercialization of GaN-on-SiC power transistors. Recently, a renewed focus on GaN-based materials research has been led by two promising approaches: AlInN/GaN high electron mobility transistors (HEMTs) for high frequency electronics and GaN-on-Si for high voltage power management and conversion.

Electronic devices based on the AlGaIn/GaN heterostructure have been extensively investigated over the past decade and are now commercially available for RF and power management applications. To fabricate conventional AlGaIn/GaN HEMTs with improved frequency response, thickness of the AlGaIn barrier layer must be reduced as the gate length is scaled. However, at barrier layer thicknesses below ~15nm, surface depletion can significantly degrade sheet charge density. The AlInN/GaN material system offers an attractive alternative for such high frequency applications. The AlInN alloy can be synthesized lattice matched to GaN with large refractive index contrast and sheet charge density roughly twice that of typical AlGaIn/GaN HEMTs. The large spontaneous polarization charge at the AlInN/GaN interface enables thin (<10nm) HEMT structures

with very high current density, low access resistance, aggressive scaling, and monolithic integration of normally-on and normally-off operation. Such devices are promising for high frequency power and mixed-signal applications. However, differences in fundamental properties of the InN and AlN binary components dictate remarkably different growth conditions and have limited progress in the growth of high quality AlInN alloys. The compromise in choice of alloy growth conditions typically results in poor material quality, often manifested in rough or pitted surface morphology and compositional inhomogeneity. It has been predicted that AlInGaN quaternaries have narrower immiscibility gaps than all ternary alloys except AlGaN [1] and quaternary barriers by MBE have been investigated [2] with favorable results.

Increasing emphasis in GaN-on-Si materials is largely fueled by the desire to incorporate GaN into power electronics systems. As compared to Si-based transistors, fundamental material properties of GaN enable devices with higher blocking voltage at a given level of on-resistance or, alternatively, a lower on-resistance at a given voltage rating. Combining these attributes with the ability of GaN power electronics to operate at higher frequencies than comparable Si devices, both a reduction in size and increase in efficiency of power conversion circuits have been demonstrated. While the high quality, low cost, and large diameter of Si substrates are well understood, other inherent advantages of GaN-on-Si include the ability to leverage established Si processes for wafer grinding & polishing, via hole formation, and AuSi eutectic die attach. Growth of GaN-on-Si requires strain-compensating layers to accommodate lattice and thermal expansion mismatch between the substrate and the epilayers. Such layer schemes typically include low temperature AlN interlayers, (Al,Ga)N-based superlattices, and/or graded composition AlGaN layers. Still, these techniques have not yet been demonstrated to reproducibly fabricate standoff layers of several to tens of microns of GaN thickness as required by kV-level device structures.

Experimental

All growths at Kopin were performed in a close-coupled showerhead MOCVD reactor operating at low pressure. Trimethylaluminum (TMA), trimethylindium (TMI) and ammonia (NH₃) were used as the material precursors. For AlInGaN/GaN heterostructures and HEMTs, the structure consisted of a nominally undoped 1.5 - 2 μm thick GaN buffer layer, a thin AlN spacer, and a AlInGaN quaternary barrier. For some AlInGaN structures, a GaN cap was explored. Optimization experiments were performed on sapphire and structures used to fabricate submicron gate HEMTs were grown on semi-insulating (S.I.) SiC substrates. For GaN-on-Si growths, the Si substrates were (111) orientation, on-axis +/- 0.5°. An extended set of on-wafer characterization tools, including atomic force microscope (AFM), high resolution x-ray diffractometer, contactless sheet resistance mapping system, CV mercury probe, were employed for structure evaluation. Select AlIn(Ga)N samples were sent to Evans Analytical Group for Secondary Ion Mass Spectroscopy (SIMS) and Rutherford backscattering spectroscopy (RBS) compositional analysis.

Optimization of MOCVD-Grown AlInGaN Heterostructures

Both ternary AlInN and quaternary AlInGaN heterostructures have been grown and analyzed by SIMS. Growth conditions and procedures can be modified to intentionally incorporate Ga into AlInN films concentration ranging from <1 at% (at these levels, it is believed that the accuracy of Ga compositional determination is limited by the resolution of SIMS and the reference RBS calibration of the SIMS measurement) to several atomic percent. Due to theoretical studies that suggest AlInGaN may be thermodynamically more favorable, and based upon our own experimental results from transport property optimization, we have chosen to focus on growth of quaternary barrier structures. Stoichiometry of $\text{Al}_x\text{In}_{(1-x-y)}\text{Ga}_y\text{N}$ layers investigated in this work was typically $x = 0.83$ and $y = 0.04$.

To improve AlInGaN surface morphology, we studied the growth of thin layers at reactor pressures of 100 and 50 torr. Figure 1 compares the $1 \times 1 \mu\text{m}^2$ AFM surface topography images and the x-ray Omega-2Theta scans of two representative samples grown at (a.) 100 and (b.) 50 torr, respectively. The thickness of AlInGaN was about 30 nm. The In composition in these samples was estimated to be about 12 - 14 % (slightly tensile strain conditions). A dramatic difference in surface topography and x-ray peak appearance is observed. In particular, the root mean square (RMS) surface roughness of AlInGaN grown at 50 torr is only 0.5 nm, more than three times lower when compared to that at 100 torr. Moreover, the x-ray peak full width at half maximum (FWHM) of the sample grown at 50 torr is 0.13° , 50 % narrower than that in sample grown at 100 torr. Growth pressure of 50 torr was used for AlInGaN growth in all subsequent experiments described below.

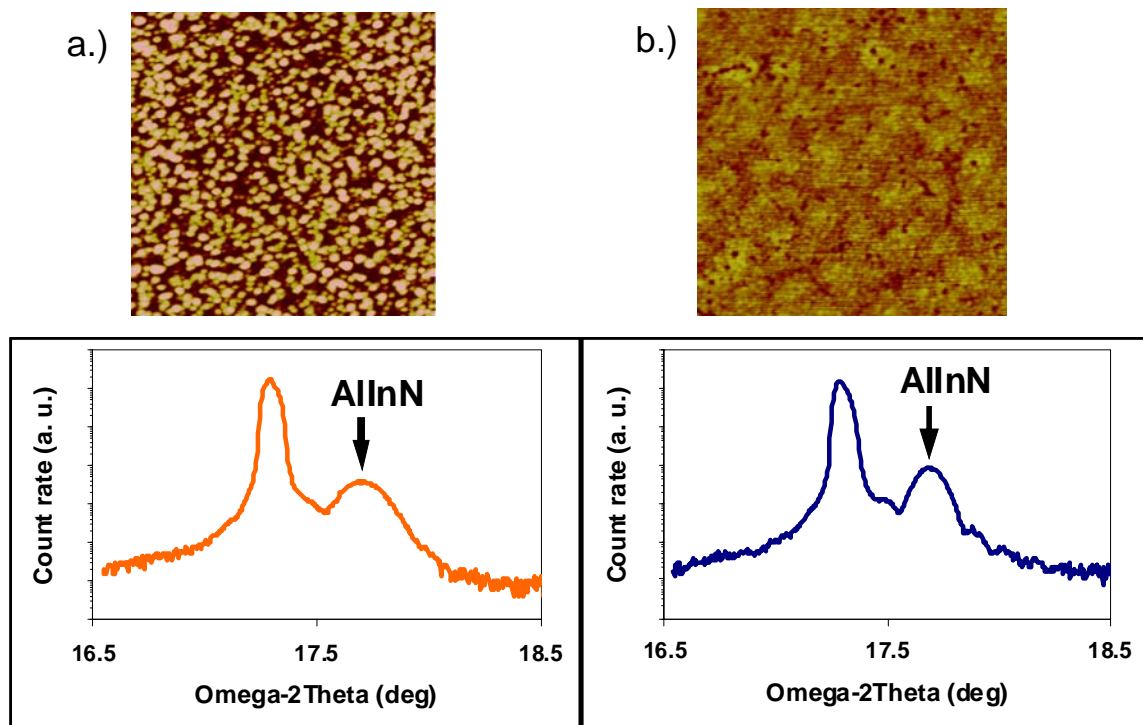


Figure 1. (a) AFM ($1 \times 1 \mu\text{m}^2$) surface topography images and x-ray Omega-2Theta scans of two representative AlInGaN test layers grown at (a.) 100 torr and (b.) 50 torr.

In order to increase the electron mobility at the AlInGaN/GaN interface, a thin AlN spacer has been commonly used between AlInGaN barrier and GaN channel by many research groups [3]. Growth of this binary spacer presents particular challenges since growth of good quality bulk AlN layers on SiC takes place at a temperature and V/III molar flux ratio of $\sim 1300^\circ\text{C}$ and ~ 1000 , respectively, whereas temperature and V/III ratio for typical AlInGaN films in this study are 850°C and 20,800 respectively. To investigate the proper growth conditions for the AlN spacer, AFM surface topography and the Leighton sheet resistance maps were investigated from $\text{Al}_x\text{In}_{(0.96-x)}\text{Ga}_{0.04}\text{N}/\text{AlN}/\text{GaN}$ heterostructures grown at various growth conditions. For AlN spacer growth conditions typical for bulk AlN, a rough surface morphology with characterized by deep craters was observed. In contrast, for samples with AlN spacer growth conditions more typical for AlInN growth, the surface was free of craters and exhibited a planar granular structure very similar to the surface of AlInGaN layer grown without the AlN spacer. The RMS surface roughness was ~ 0.4 nm. Sheet resistance followed the improvement in the surface morphology, with average sheet resistance and its standard deviation of 419 and 22 ohm/sq for the rough sample and 167 and 6 ohm/sq for the optimized, low temperature sample at AlN spacer thickness of 1 nm. The sheet resistance of 167 ohm/sq is comparable to the best results published in the literature for AlInN-based structures [4-6].

The AlInGaN barrier and AlN spacer thicknesses were optimized on the basis of Leighton sheet resistance. Thicknesses of both were estimated from x-ray reflectivity measurements. Figure 2 illustrates that AlInGaN thickness had nearly no effect on the sheet resistance of HEMT structures in the range of 10 - 60 nm. However, the sheet resistance sharply increased above 3,000 ohm/sq when the thickness decreased below 10 nm. The sheet resistance of $\text{Al}_x\text{In}_{(0.96-x)}\text{Ga}_{0.04}\text{N}/\text{AlN}/\text{GaN}$ structures was found to be lowest, about 167 Ohm/sq, when the thickness of the AlN spacer was in the range of 0.5 - 1 nm.

Interestingly, the In composition of the $\text{Al}_x\text{In}_{(0.96-x)}\text{Ga}_{0.04}\text{N}$ barrier layer has a dramatic effect on the sheet resistance of HEMTs grown without an AlN spacer (Fig. 3). In contrast, the composition of AlInGaN has insignificant impact on the sheet resistance of the structure with a ~ 1 nm thick AlN spacer, for which sheet resistance was 160 - 176 ohm/sq over the entire composition range. This is believed to be attributable to increased alloy scattering with increasing indium incorporation for the structures grown without the AlN spacer. For HEMTs including the 1nm AlN spacer, alloy scattering from the quaternary AlInGaN barrier is effectively screened from the channel electrons, leading to increased mobility and greatly reduced impact of stoichiometry.

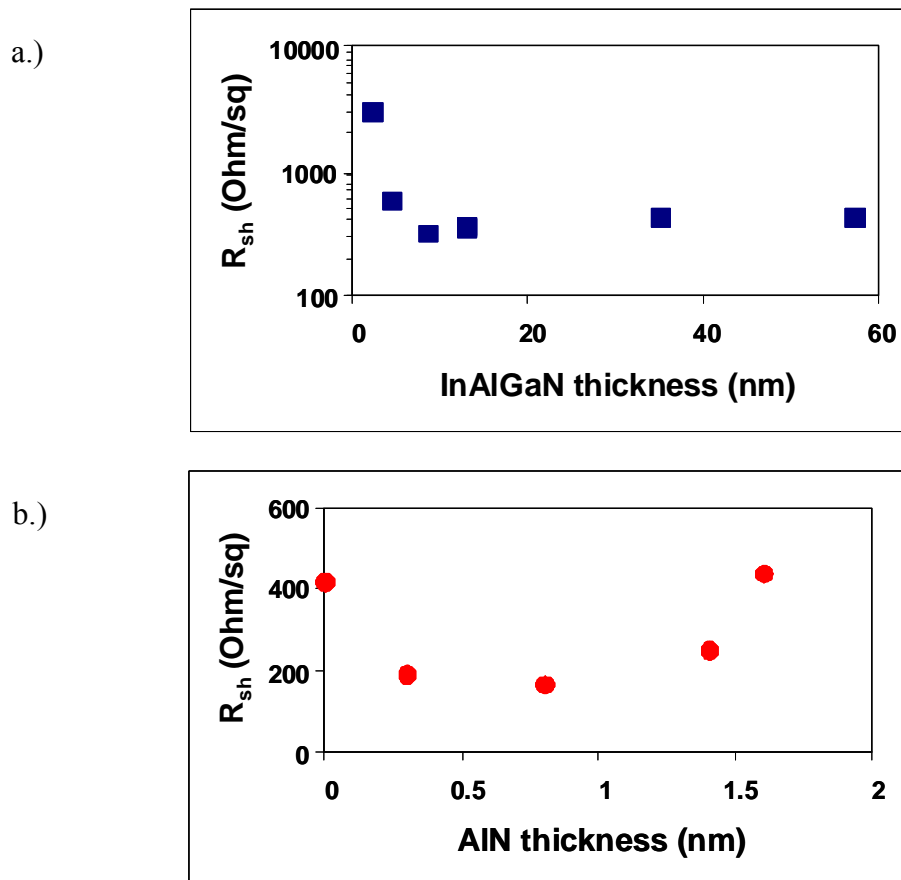


Figure 2. Sheet resistance of $\text{Al}_{0.83}\text{In}_{0.13}\text{Ga}_{0.04}\text{N}/\text{AlN}/\text{GaN}$ heterostructures on sapphire as a function of (a) AlInGaN barrier thickness and (b) AlN spacer thickness.

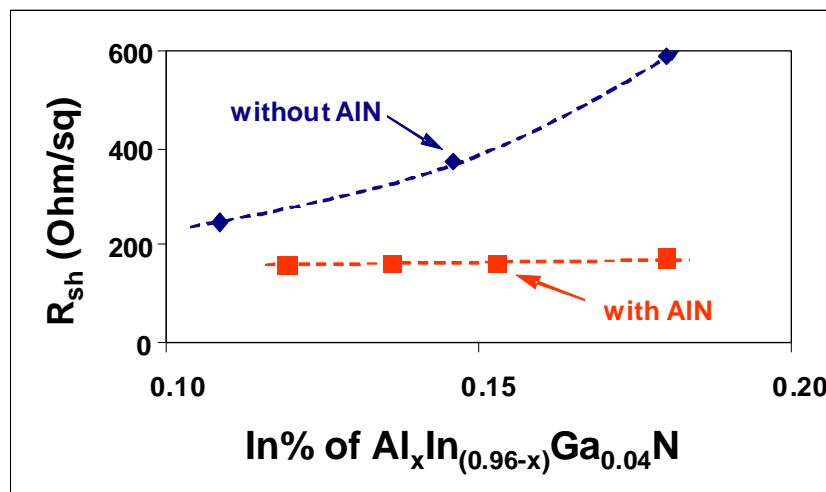


Figure 3. Sheet resistance of $\text{Al}_x\text{In}_{(0.96-x)}\text{Ga}_{0.04}\text{N}/\text{AlN}/\text{GaN}$ heterostructures on sapphire as a function of indium composition.

Using optimized growth conditions and structure design as illustrated in Figs. 1-3, HEMTs that included a 10 nm $\text{Al}_{0.83}\text{In}_{0.13}\text{Ga}_{0.04}\text{N}$ barrier and ~ 2.5 nm GaN cap layer were grown on sapphire substrates. Surface morphology evolution was studied as a

function of GaN cap growth temperature and cap TMG flux. The RMS surface roughness decreased with increasing growth temperature of the GaN cap layer, approaching 0.3 nm at growth temperatures of 150 - 200°C above the growth temperature of AlInGaN. Sheet resistance of the AlInGaN/AlN/GaN HEMTs increased with increasing cap growth temperature and decreased with increasing TMG flux. Hall effect and CV measurements of the capped structures revealed that the variation in the 2DEG mobility was a major cause of the change in sheet resistance. HEMTs with 0.8 μm gate length and 3 μm source-drain spacing, both with and without cap layers, were fabricated at the University of Florida to assess the impact of the GaN cap on leakage current and device performance. DC I-V characteristics of unpassivated devices demonstrated peak drain current of ~ 1.25 A/mm. Transfer curves yielded transconductance of 325 mS/mm for capped structures and 370 mS/mm for uncapped control devices. The pinchoff voltage was shifted by -0.8V for the capped structures due to the increased gate to channel spacing caused by the cap relative to uncapped devices. Two-terminal gate leakage current was reduced in capped structures by roughly a factor of 2, but Schottky barrier height (SBH) extracted from forward gate diode curves was 0.62-0.63eV for both capped and uncapped samples. Gate leakage is an area where AlIn(Ga)N HEMTs have not yet reached their AlGaIn/GaN counterparts. The mechanism for higher leakage currents in AlInN-based HEMTs is still not yet well understood, but is speculated to be associated with compositional nonuniformity in the barrier layer, possibly leading to localized regions of reduced SBH, or defect-assisted current transport.

Uncapped structures with 10.3 nm $\text{In}_{0.13}\text{Al}_{0.83}\text{Ga}_{0.04}\text{N}$ barrier layer and 1 nm AlN spacer were grown on S.I. SiC substrates and used to fabricate submicron HEMTs at the University of Notre Dame. Hall data yielded sheet electron concentration of 1.77×10^{13} cm^{-2} with associated mobility of 1840 cm^2/Vs for unpassivated devices. After dielectric-free passivation [7], sheet charge increased $\sim 20\%$ while mobility only degraded by 6%, resulting in a passivated sheet resistance of 190 ohm/sq . HEMTs with 66 nm trapezoidal gates and 300 nm source-drain spacing produced output current density of 2.0 A/mm and extrinsic transconductance of 548 mS/mm. Short channel effects led to significant output conductance as can be seen in Fig. 4a, but the device maintained pinchoff to $>10V_{\text{ds}}$. Small signal data yielded a peak cutoff frequency (f_T) of 220 GHz with associated maximum oscillation frequency (f_{max}) of 60 GHz. The f_{max} was limited by gate resistance from the trapezoidal gate. A significant increase in f_{max} is expected for similar devices formed with a T-gate structure. A high effective electron velocity of 0.9×10^7 cm/s was calculated from the peak f_T . These results represent a significant advancement beyond performance levels of AlGaIn/GaN HEMTs and clearly demonstrate the suitability of the AlIn(Ga)N system for high frequency applications.

GaN-on-Silicon

GaN-on-Si HEMTs hold great promise for high efficiency power conversion and power management. Here, GaN is expected to enable performance figures-of-merit ten times greater than those attainable from modern Si-based power electronics. The ability to fabricate such devices on industry-standard Si substrates enables a cost structure that can much more easily integrate into commercial applications than comparable SiC or GaN-on-SiC power devices. Through thermal design and advanced packaging, thermal management of GaN-on-Si – sometimes cited as a limiting feature of the technology – can reach levels similar to GaN-on-SiC [8].

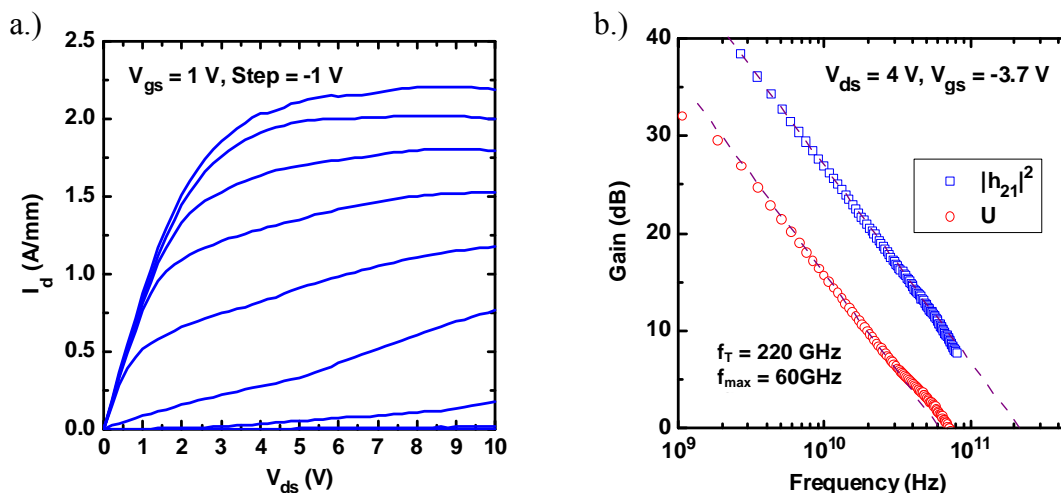


Figure 4. (a.) Output characteristics and (b.) current and unilateral gain of optimized AlInGaN/AlN/GaN HEMT with 66 nm gate length. Peak output current density reaches 2.0 A/mm and peak cutoff frequency is 220 GHz.

The primary impediment to practical realization of GaN-on-Si power electronics has been the lack of availability of high quality, low background concentration, thick GaN epilayers on Si (111). This limitation is caused by difficulties overcoming the lattice and coefficient of thermal expansion mismatches between GaN and Si. These mismatches have been researched extensively and many growth schemes have been proposed to achieve crack-free films, including graded AlGaIn buffers [9], low-temperature interlayers [10], and superlattice structures [11]. A critical aspect of most GaN-on-Si MOCVD growth schemes is nucleation, typically of AlN, and the subsequent coalescence of the overlying GaN film. Here we present a study of HT AlN nucleation and growth focusing on effects of Al predeposition, NH_3 flow, and temperature. This optimization is demonstrated to enable GaN islands to coalesce more quickly during their early stage of growth on AlN.

All test structures included a ~ 160 nm HT AlN nucleation layer and ~ 700 nm GaN layer. Before growth, the silicon substrates were baked in H_2 for ~ 10 min at 1280°C , which is the temperature set point (TSP) corresponding to actual substrate temperature of $\sim 1150^\circ\text{C}$. After desorption bake, the temperature was ramped down to the growth temperature of 1260°C by TSP. To prevent the substrate from forming a surface layer of silicon nitride, TMA was introduced into the reactor prior to any NH_3 flow. Thus a thin layer of Al was pre-deposited before growth initiation. Predeposition times of 1 sec, 2 sec, 5 sec and 8 sec. were investigated, and the HT AlN was grown immediately following the predeposition. The GaN layer was then grown at 1170°C by TSP. The NH_3 flow was 1200 sccm for AlN and 10,000 sccm for GaN. The reactor pressure was 50 torr and 100 torr for AlN and GaN layers, respectively.

Fig. 5 shows AFM $10 \times 10 \mu\text{m}^2$ scans from the GaN surface after growth. From the observation of large holes for longer predeposition time, it is obvious that long predeposition times result in coalescence problem during subsequent GaN growth. The depth

of the holes in the sample with 8 sec pre-deposition is more than 50 nm. The large holes for long pre-deposition times indicate that the AlN grown below the GaN could be defective where the AlN layer did not fully cover the silicon due to excessive pre-deposited Al. This was verified by another series of growths with only AlN on silicon, with pre-deposition times of 2 sec, 5 sec and 10 sec. The AlN film tended to show large-scale defects when the pre-deposition time increased, as shown in the $10 \times 10 \mu\text{m}^2$ AFM scans of Fig. 6. These large defects could correlate with the big holes found in the GaN grown on such AlN templates.

Growth temperature is another important factor for HT AlN. With all other growth parameters fixed, various temperatures were selected for the AlN growth. Fig. 7 shows $10 \times 10 \mu\text{m}^2$ AFM images of AlN grown at different TSP values of 1260°C, 1305°C and 1330°C. At higher temperature, AlN films coalesced better and demonstrated a more uniform coating on the silicon substrate. The pre-deposition time for this series of growths was 2 sec. Since the pre-deposition and the AlN growth were performed at the same temperature, the pre-deposited Al could be insufficient for the growth conducted at 1330°C, which leads to the poor coalescence.

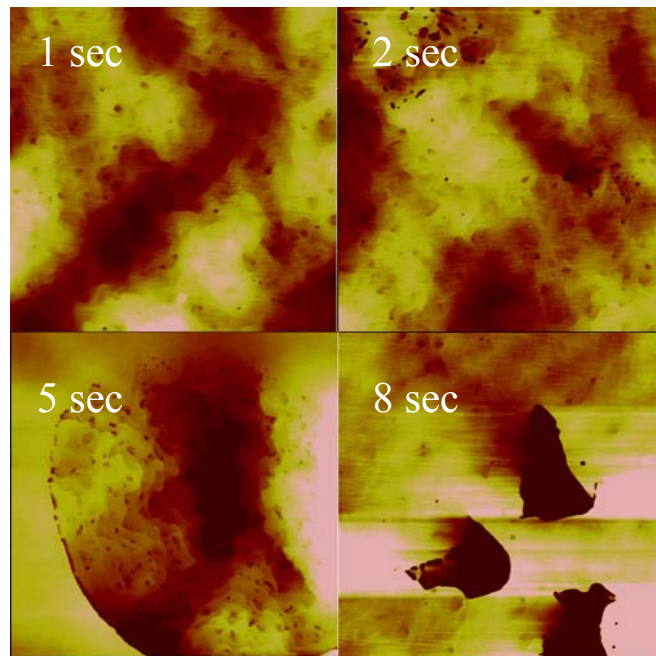


Figure 5. $10 \times 10 \mu\text{m}^2$ AFM images of GaN grown over AlN/Si where the AlN growth was initiated by different Al pre-deposition times.

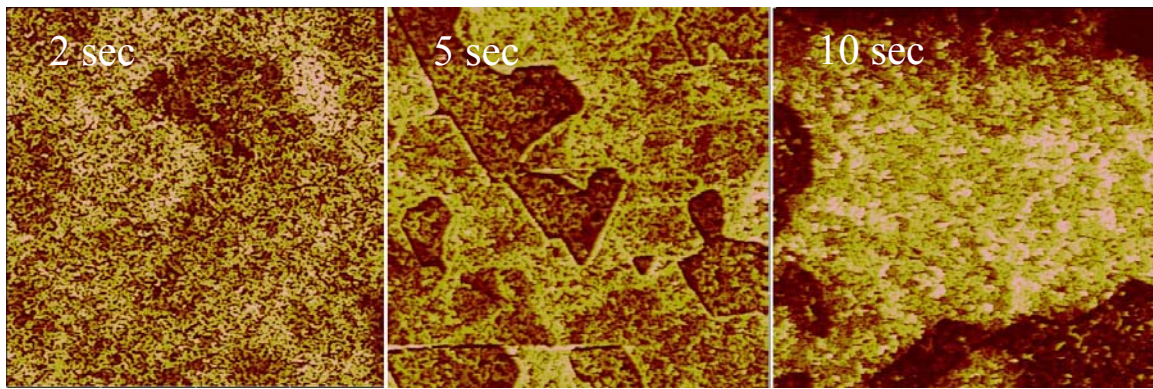


Figure 6. $10 \times 10 \mu\text{m}^2$ AFM images of AlN on Si with different Al pre-deposition time.

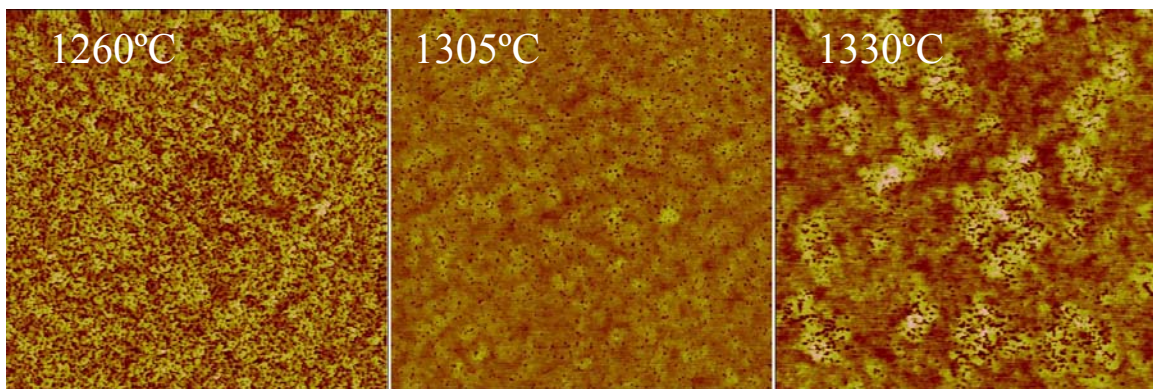


Figure 7. $10 \times 10 \mu\text{m}^2$ AFM images of AlN with different growth temperatures

Using optimized predeposition time and AlN growth temperature, GaN films were then studied on the AlN/Si template. The GaN growth temperature was 1190°C by TSP, reactor pressure was 100 torr, and NH_3 flow was investigated at levels of 10,000 sccm, 8,000 sccm, 5,000 sccm and 3,000 sccm. The GaN growth rate was observed to be slightly higher for higher NH_3 flow and in-situ reflectance showed the surface of the GaN recovered faster with higher NH_3 flow. Fig. 8 shows the in-situ reflectance of two growths where GaN was grown with 8000 and 5000 sccm of NH_3 flow. The in-situ reflectance showed the surface of GaN recovered faster with higher NH_3 flow, which is consistent with GaN growth on sapphire substrates. However, reflectance techniques sample the wafer surface over large spot size and can not observe small features. To illustrate the microscale surface texture, AFM images were collected and are shown in Fig. 9 for NH_3 flows of (a.) 8000 sccm and (b.) 5000 sccm. The optimized NH_3 flow of 5,000 sccm resulted in RMS roughness of 0.9 nm in the $10 \times 10 \mu\text{m}^2$ AFM scan of Fig. 9b. Both GaN layers of Fig. 9 were crack free. Although the direct GaN on AlN/Si nucleation and recovery approach does not enable growth of thick films as required by most device applications, the results can be combined with other stress-mitigation techniques to build thick structures. Subsequent optimization of point defects is necessary to produce GaN buffer films with low background carrier concentration suitable to stand-off high critical fields achieved during high voltage operation.

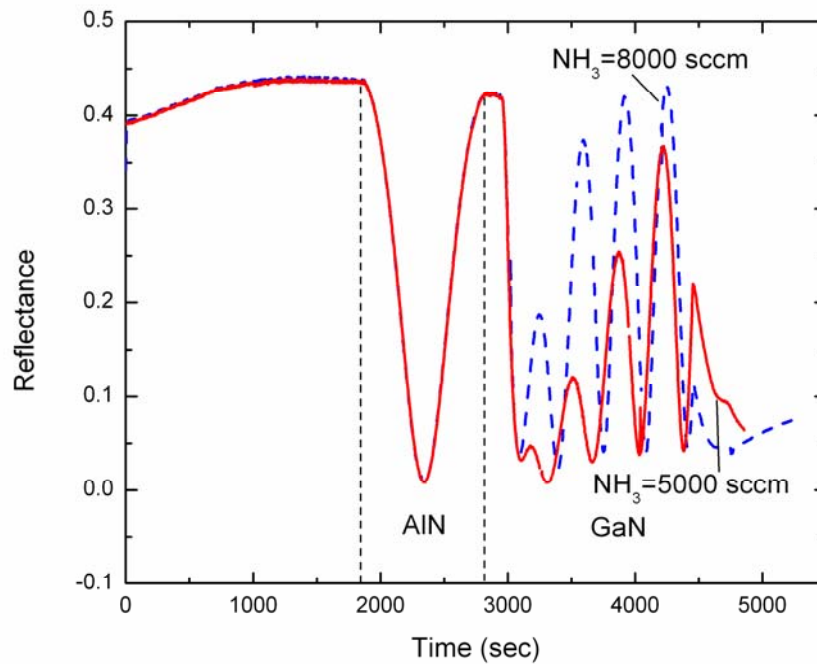


Figure 8. In-situ reflectance of GaN/AlN/Si growths as a function of NH_3 flow. The larger amplitude increase of the 8000 sccm sample indicates faster evolution of a smooth, specular GaN surface than for lower NH_3 flow.

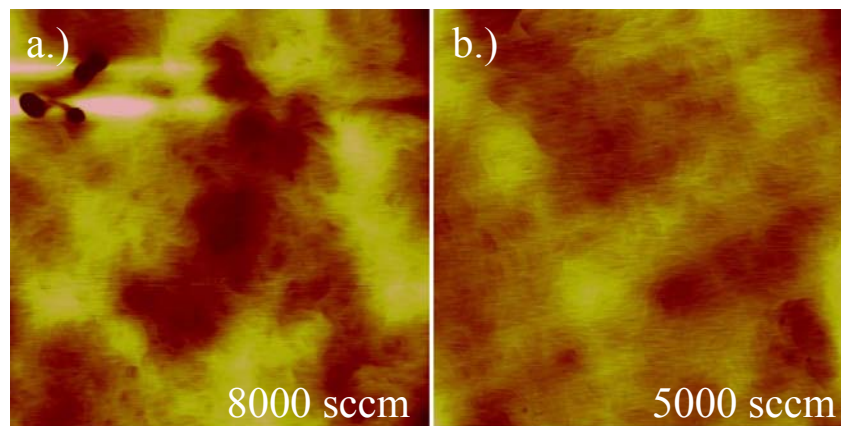


Figure 9. $10 \times 10 \mu\text{m}^2$ AFM images of the GaN surface for the films of Fig. 8. The NH_3 flow was (a.) 8000 sccm and (b.) 5000 sccm. RMS roughness was 1.5 nm and 0.9 nm for (a.) and (b.), respectively.

Conclusions

Optimization of MOCVD growth of quaternary barrier AlInGaN HEMTs employing a thin AlN spacer layer has been demonstrated. Excellent transport properties achieved from the optimization enabled fabrication of heterostructures with sheet resistance < 200 ohms/sq. and HEMTs with $f_T > 200$ GHz. GaN-on-Si growth studies have been presented in the context of HT-AlN nucleation on Si (111) and surface recovery of subsequent GaN growth. As AlInGaN and GaN-on-Si materials mature, there is no reason why these 2

technologies cannot be merged into a high performance AlIn(Ga)N-based HEMT grown on Si. Silicon substrates with low transmission line loss have been demonstrated and will enable high frequency performance of AlInGaN-on-Si RF devices. Likewise, the extremely low sheet resistances available from the AlInGaN system will enable lower on-resistance of switching devices for a given blocking voltage, resulting in lower $R_{on}^2 \cdot A$ (on-resistance squared multiplied by chip area) figure-of-merit (FOM). By combining this low FOM with appropriately designed growth schemes for thick GaN buffer layers on Si, high voltage, low-resistance power electronics of the future are likely to employ both of the material systems described in this work.

Acknowledgments

Funding for this work is partially provided by the Missile Defense Agency via SBIR contract # W9113M-09-C-0071 (John Blevins), Defense Advanced Research Projects Agency (John Albrecht, NEXT program), the Air Force Office of Scientific Research (Kitt Reinhardt), and by a DOD MURI (Gregg Jessen, AFOSR). Ongoing support is acknowledged from Daily Hill and the III-V Product Group at Kopin Corporation.

References

1. T. Takayama, M. Yuri, K. Itoh, T. Baba, and J. S. Harris, *J. Cryst. Growth*, **222**(1), 29 (2001).
2. T. Lim, R. Aidam, P. Waltereit, W. Pletschen, R. Quay, L. Kirste, and O. Ambacher, *Physica Status Solidi (c)*, **8**(N/A) DOI: 10.1002/pssc.201001042 (2011).
3. J. Xie, X. Ni, M. Wu, J. H. Leach, Ü. Özgür, and H. Morkoç, *Appl. Phys. Lett.*, **91**, 132116 (2007).
4. H. P. D. Schenk, M. Nemoz, M. Korytov, P. Venegues, A. D. Dräger, and A. Hangleiter, *Appl. Phys. Lett.*, **93**, 081116 (2008).
5. M. Gonschorek, J.-F. Carlin, E. Feltn, M.A. Py, and N. Grandjean, *Appl. Phys. Lett.*, **89**, 062106 (2006).
6. H. Sun, A.R. Alt, H. Benedickter, E. Feltn, J.-F. Carlin, M. Gonschorek, N. Grandjean, and C.R. Bolognesi, *IEEE Electron Device Lett.*, **31**(9), 957 (2010).
7. R. Wang, G. Li, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, *IEEE Electron Device Lett.*, **32**(7), 892 (2011).
8. S. Singhal, J.D. Brown, R. Borges, E. Piner, W. Nagy, and A. Vescan, *Gallium Arsenide Integrated Circuit (GaAs IC) Symp. Dig.*, (2002).
9. P. Rajagopal, T. Gehrke, J.C. Roberts, J.D. Brown, T.W. Weeks, E.L. Piner, and K.J. Linthicum, *Mater. Res. Soc. Symp. Proc.*, **743**, 3 (2003).
10. A. Krost and A. Dadgar, *Mater. Sci. Eng.* **B93**, 77 (2002).
11. G.-M. Wu, C.-W. Tsai, N.-C. Chen, and P.-H. Chang, *Crystal Research and Tech.*, **42**(12), 1276 (2007).