Enhancement-Mode InAlN/AlN/GaN HEMTs With 10^{-12} A/mm Leakage Current and 10^{12} ON/OFF Current Ratio

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***Abstract*—Postprocessing annealing in forming gas at 400 °C was performed on enhancement-mode lattice-matched InAlN/AlN/GaN high-electron-mobility transistors fabricated by selective etch of InAlN under a Pt gate. After postprocessing annealing, the device reverse gate leakage current decreased from 10^{-7} to 10^{-12} A/mm at $V_{gs} = -1$ V and $V_{ds} = 6$ V, showing an ON/OFF current ratio of 10^{12} that is the highest reported value for all GaN-based transistors. The gate diode breakdown voltage was observed to increase from ∼9 to ∼29 V; the transistor threshold voltage was also found to shift from 0.6 to 1.2 V. All these observations indicate that an electrically thinner and more insulating interlayer is most likely formed between the Pt gate and underlying channel after postprocessing annealing, which is ascribed to multiple possible mechanisms including increase in barrier height, reduction in interface states introduced during the gate recess process, formation of a thin oxide layer, etc.**

***Index Terms*—Enhancement mode (E-mode), gate leakage current, InAlN, postprocessing annealing.**

I. Introduction

LATTICE-MATCHED InAlN/GaN high-electron-mobility transistors (HEMTs) have attracted a lot of attention recently due to the demonstrated high drain current density [1] and superior thermal stability [2] for power electronics, as well as high speed [3]. However, low gate leakage current is still a challenge for GaN-based transistors, since high gate leakage current causes extra noise in power amplifiers [4], additional loss at OFF state in power supplies [5], as well as other reliability problems [6]. Several approaches, including gate dielectric insertion [6], O_2 plasma treatment [7] and CF_4 plasma treatment [8] underneath the gate, and oxide-filled isolation followed by postgate annealing [9], showed gate leakage current reduction and an ON/OFF current ratio of up to $\sim 10^8 - 10^9$ in depletion-mode AlGaN/GaN HEMTs. In enhancement-mode (E-mode) devices, the gate leakage current is usually more severe because of thinner barrier layers.

In this letter, E-mode InAlN/AlN/GaN HEMTs have been fabricated by selectively etching away the InAlN barrier in the gate region. Postprocessing annealing was performed to study the effect on gate leakage current and threshold voltage. After postprocessing annealing, an extremely low gate leakage current of $\sim 10^{-12}$ A/mm, a record high ON/OFF current ratio of $\sim 10^{12}$, a positive threshold voltage shift, and a peak transconductance increase have been observed.

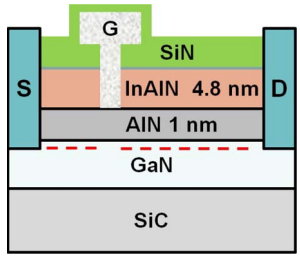

Fig. 1. Schematic cross section of gate-recessed E-mode InAlN/AlN/GaN HEMTs.

II. Experiments

The InAlN/AlN/GaN HEMT structure (Fig. 1) consists of a 4.8-nm InAlN barrier, a 1-nm AlN spacer, an unintentionally doped GaN channel, and a 1.8-μm Fe-doped GaN semi-insulating buffer on SiC substrate, grown by MOCVD at IQE RF LLC. The devices were fabricated at Triquint Semiconductor, Inc., using the AlGaN/GaN HEMT process flow. Nitrogen ion implantation was used for isolation. Unoptimized Ti-based alloy ohmic contact gave a contact resistance R_c of $\geq 0.55\Omega \cdot$ mm. The gate recess to etch away InAlN down to the AlN layer was realized by a BCl_3-based reactive ion etching process following etching of the top SiN passivation using F-based plasma. Electron-beam lithography was used to define 150-nm-long gates with varying gate widths, followed by Pt/Au

Manuscript received October 15, 2010; revised November 12, 2010; accepted November 20, 2010. Date of publication January 6, 2011; date of current version February 23, 2011. This work was supported by the Defense Advanced Research Projects Agency (John Albrecht, the NEXT Program HR0011-10-C-0015). The review of this letter was arranged by Editor J. A. del Alamo. The views, opinions, and/or findings contained in this letter are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

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Digital Object Identifier 10.1109/LED.2010.2095494

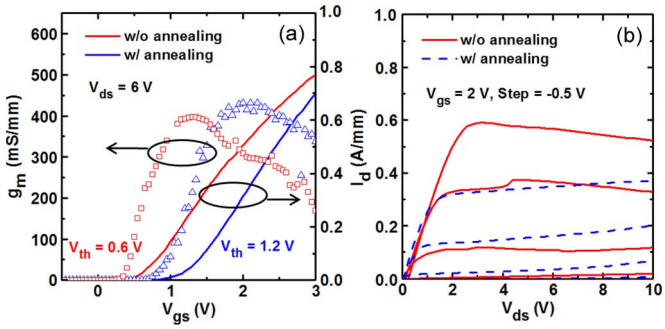

Fig. 2. (a) Linear-scale transfer curves at $V_{\rm ds} = 6$ V and (b) common source family I–V values before and after postprocessing annealing, respectively.

gate metal deposition, and an additional 200-nm SiN passivation. The Hall-effect measurement using the Van der Pauw pattern in an unrecessed region shows a sheet resistance of $\sim$270 Ω/sq, a 2-DEG density of $\sim 2 \times 10^{13}$ cm^{-2}, and an electron mobility of $\sim$1160 cm^2/V $\cdot$ s. More detailed descriptions on dc and RF characteristics of the E-mode HEMTs processed in the same manner have been reported elsewhere [10]. The devices presented here showed lower g_m due to higher R_c and likely higher density of interface states $D_{\rm it}$.

The as-processed devices were annealed in forming gas (5% H_2, balanced with Ar) at 400 °C for 10 min, using a rapid thermal annealing system. Field-effect measurements were performed using a Keithley 4200 semiconductor characterization system at room temperature (RT), before and after postprocessing annealing.

III. Results and Discussion

Shown in Fig. 2 are linear-scale transfer curves and common source family of I–V curves before and after postprocessing annealing, respectively. The device source–drain spacing is 2 μm with a gate width of 8×50 μm. Before postprocessing annealing, the peak extrinsic transconductance $g_{m,\rm ext}$ is 390 mS/mm at $V_{\rm ds} = 6$ V, and the output drain current density is 0.78 A/mm at $V_{\rm gs} = 3$ V. After postprocessing annealing, the transistor threshold voltage $V_{\rm th}$ shifts from 0.6 to 1.2 V, extracted from the linear extrapolation of I_d; meanwhile, the peak $g_{m,\rm ext}$ increases to 420 mS/mm. More than eight chips of devices from the same wafer were individually annealed and compared; the positive threshold voltage shift ($\sim$0.2 – 0.6 V) has been observed in all the devices, and the device $f_t/f_{\rm max}$ was found to improve by $\sim$10%. Two chips were also annealed in N_2 under otherwise the same conditions, and a similar trend in device performance improvement has been observed.

The common trend of a shift in $V_{\rm th}$ shift and increase in peak $g_{m,\rm ext}$ after postprocessing annealing was reported first in Pt-gated InAlAs HEMTs [11] and, more recently, in Ir-gated E-mode InAlN/AlN/GaN HEMTs [12]. Chen *et al.* [11] explained this phenomenon based on the previously reported studies on chemical reaction of Pt gate with underlying InAlAs: Upon annealing, InAlAs barrier was consumed, and conducting $PtAs_2$ was formed on a possible AlAs interface layer [13] on top of the thinned InAlAs barrier. Ostermaier *et al.* [12] postulated based on their transmission electron microscopic (TEM) studies

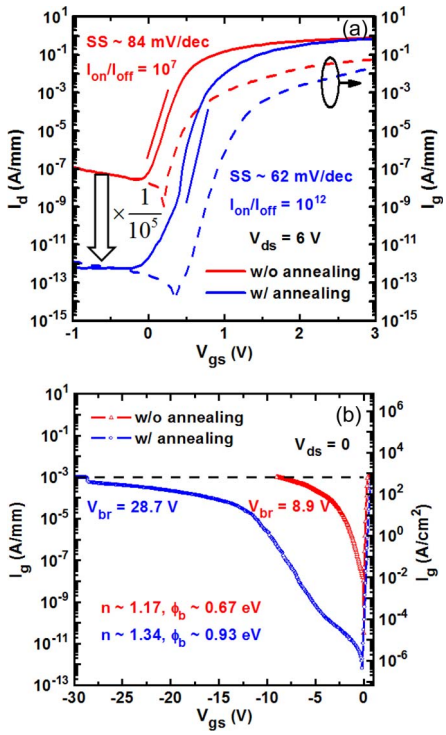

Fig. 3. (a) Semi-log-scale transfer curves at $V_{\rm ds} = 6$ V, and (b) gate diode I–V values showing breakdown voltages before and after postprocessing annealing, respectively.

that the oxygen-bearing interface layer between gate metal Ir and InAlN became thinner upon annealing due to oxygen diffusion into Ir instead of Ir alloying with InAlN. Both processes have been termed as gate sinking, but due to different processes. In our case, on a separate process-control-monitoring chip, it was observed that R_c increased from 0.55 to 0.75 $\Omega \cdot$ mm after postprocessing annealing, while the access resistance did not change based on the Hall-effect measurement. Therefore, the increase of peak $g_{m,\rm ext}$ should stem from gate barrier thinning electrically, which could be due to physical gate sinking and/or interface state $D_{\rm it}$ reduction. Our preliminary TEM study [10] shows that the 1-nm-thick AlN barrier under the Pt gate is continuous; however, an interface layer could exist [14], possibly consisting of residual InAlN and oxygen-bearing materials. Similar to Ostermaier's observations, this interlayer may have become thinner and denser upon thermal annealing, thus leading to physical "gate sinking."

Fig. 3(a) shows semi-log-scale transfer curves measured at $V_{\rm ds} = 6$ V. The gate leakage currents in both reverse and forward directions decrease after postprocessing annealing with an electrically thinner barrier. In the reverse bias direction, the gate leakage current decreasing from 10^{-7} to 10^{-12} A/mm is shown in Fig. 3(a), leading to an ON/OFF current ratio of 10^{12}. To the best of our knowledge, this ON/OFF current ratio is the highest, accompanied by the lowest gate leakage current reported for any GaN-based transistor. In the forward bias direction, the turn-on voltage of gate diodes increases. Moreover, the subthreshold slope (SS) decreases from 84 to 62 mV/dec, which is very close to the theoretical limit at 300 K. One can extract the associated interface states from the SS

values [10] as 1.5×10^{13} and 1.1×10^{12} $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ before and after postprocessing annealing, respectively. This indicates that the interface states that are possibly caused by the plasma treatment during the gate recess process have been repaired by the thermal treatment. It is also noted that the kinks observed in the I–V values of as-fabricated devices, shown in Fig. 2(b), disappeared upon annealing, suggesting these kinks are most likely related to traps.

Shown in Fig. 3(b), the gate diode breakdown voltage at $I_g = 1$ mA/mm increases from 8.9 to 28.7 V after annealing; the three-terminal device breakdown voltages measured at $I_d =$ 1 mA/mm and $V_{\mathrm{gs}} = -1$ V are the same, $\sim$29 V. From the forward biased gate diode I–V characteristics, the effective thermionic barrier height of 0.67/0.93 eV and the ideality factor 1.17/1.34 are extracted before and after annealing, respectively. The extracted effective barrier heights are smaller than expected [10] due to tunnelling currents. Nevertheless, it implies that barrier height increase is one possibility for the observed electrically more insulating and thinner barrier.

Due to the large Schottky barrier height and ultrathin barrier, tunnelling current is the main leakage current mechanism, including both trap-assisted tunnelling (TAT) and direct Fowler–Nordheim tunnelling (FNT). The leakage current density caused by TAT can be expressed as [15]

$$J_{\mathrm{TAT}} \propto N_t E_{\mathrm{die}} \exp\left[-(\varepsilon_T - A\sqrt{E_{\mathrm{die}}})/k_B T\right] \qquad (1)$$

in which N_t is the trap density, E_{die} is the electrical field in the dielectric, ε_T is the trap energy below the dielectric conduction band edge, and A is a constant. Reduction in trap density can lead to gate leakage current reduction. The leakage current density caused by FNT can be expressed as [16]

$$J_{\mathrm{FNT}} = B E_{\mathrm{die}}^2 \exp\left(-C\phi_b^{3/2}/E_{\mathrm{die}}\right) \qquad (2)$$

in which ϕ_b is the barrier height (in eV), and B, C are positive constants. A larger barrier height due to possible formation of interface Al_2O_3 or other insulators upon annealing can lead to gate leakage reduction. However, further work is necessary to gain a better picture of this interface.

IV. Conclusion

The effect of postprocessing annealing on gate leakage current in gate-recessed E-mode InAlN/AlN/GaN HEMTs has been investigated. The record high ON/OFF current ratio of 10^{12} with a very low leakage current of 10^{-12} A/mm has been demonstrated, probably due to interface TAT weakening, Schottky barrier height increase, and ultrathin oxide formation. The positive threshold voltage shift ($\sim$0.6 V) and intrinsic peak transconductance increase ($\sim$23%), indicating barrier thinning electrically, are attributed to D_{it} reduction, barrier height increase, and, perhaps, physical gate sinking during postprocessing annealing.

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