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Subcritical barrier AlN/GaN E/D-mode HFETs and inverters

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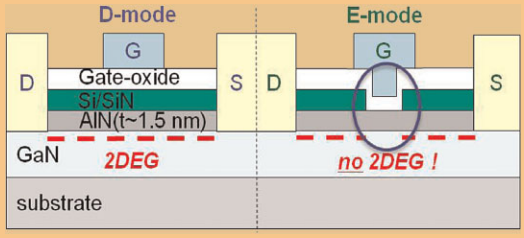
Enhancement- and depletion-mode AlN/GaN HFETs have been fabricated with a subcritical barrier design: a two-dimensional electron gas (2DEG) is induced in the highly resistive as-grown heterostructure when a suitable capping material is deposited over the ultrathin AlN barrier. In this bottom-up approach 2DEGs can be locally induced by patterned cap layers on subcritical barrier AlN/GaN hetero-structures, which can enable the monolithic integration of enhancement- and depletion-mode HFETs. An inverter circuit with 1.5 nm ultrathin AlN barrier E- and D-mode HFETs was successfully demonstrated with reasonable voltage transfer characteristics, noise margin, and gain. To our best knowledge this is the first reported inverter based on subcritical barrier III–V nitride heterostructures.



Integration of E- and D-mode HFETs in a subcritical barrier AlN/GaN heterostructure, where $n_{2DEG} \sim 0$ in the as-grown structure. A patterned cap locally enhances 2DEG at the AlN/GaN hetero-interface due to barrier lowering. It is an additive approach in contrast to the conventional gate recessing technique.

1 Introduction Aggressive downscaling of lateral and vertical dimensions of III-nitride HFETs asks for heterostructures with high-energy band offsets, thin barriers, and high-charge densities. AlN/InN/AlN and AlN/GaN/AlN quantum-well structures, therefore, should be ideal candidates to address these requirements. While AlN/InN heterostructures are challenging to grow due to the large lattice mismatch, high-quality AlN/GaN materials, and devices have been demonstrated by various groups including ours [1, 2]. Two-dimensional electron gas (2DEG) densities in excess of $1 \times 10^{13}\,cm^{-2}$ and electron mobilities of $\sim 1600\,cm^2/Vs$ can be achieved with 2–5 nm AlN barrier heterostructures [3]. In this paper, we report a bottom-up method to realize both depletion-mode as well as enhancement-mode HFETs using subcritical barrier AlN/GaN heterostructures and selectively deposited or patterned capping materials. Employing this approach, an inverter using these E- and D-mode HFETs was demonstrated.

2 Device design and fabrication process The AlN/GaN structures were grown in a Veeco Gen 930 MBE system. Active nitrogen was supplied by a RF plasma source. The growth was performed under metal-rich condition. About 200 nm unintentionally doped (UID) GaN was grown on highly resistive Lumilog semi-insulating (SI) GaN on sapphire, capped with a 1.5 nm AlN barrier. This barrier is of "sub-critical" thickness, meaning no polarization-induced 2DEG was measured in the as-grown AlN/GaN heterostructures. Several capping materials were then deposited *ex situ* and sheet resistance/Hall effect measurements were performed to monitor the formation of 2DEG channel. The following capping materials have been found to induce a 2DEG: low-power PECVD-SiN, ALD-Al_2O_3, and e-beam evaporated Si. A 4 nm e-beam evaporated Al_2O_3 layer was used as the HEMT gate dielectric since it was found to induce $n_s < 4 \times 10^{12}\,cm^{-2}$, which was found to be depleted by the Ni gate at zero bias. The measured sheet resistance of various structures investigated is

shown in Fig. 1. The SI-GaN substrate has a high-sheet resistance of 4×10^7 Ω/sq. The sheet resistance decreased to 2.7×10^5 Ω/sq upon growth of the 200 nm UID GaN buffer. Little change in the resistance was observed when measured on the 1.5-nm-AlN/GaN heterostructure, indicating no 2DEG formed near the AlN/GaN interface. However, after deposition of Si, SiN_x, or ALD-Al_2O_3 a significant decrease in sheet resistance by two orders of magnitude, down to ~400 Ω/sq, was observed (see Figs. 2–4). Hall effect measurements showed that the induced 2DEG has an electron mobility of ~400–800 cm^2/Vs with a density of 2–4 $\times 10^{13}$ cm^{-2}. Conduction through the deposited Si or SiN cap is ruled out by control measurements on SI-GaN with the same capping materials. The 2DEG formation is thus attributed to substantial surface barrier lowering [4]. Silicon caps proved unstable over time in air. In contrast, a thin Si (2 nm)/ALD-Al_2O_3 (4 nm) cap layer and PECVD-SiN reliably enhance 2DEGs in subcritical barrier AlN/GaN structures (Figs. 2 and 5).

As a proof of concept demonstration, E-mode and D-mode subcritical barrier AlN/GaN HFETs were fabricated on two separate pieces from the same wafer as follows. The inverters were then tested by probing pairs of E- and D- mode devices. For D-mode HFETs, a 10 nm PECVD SiN was first blanket deposited over the entire sample. Device isolation was obtained by 300 nm deep reactive ion etching. After source and drain contact lithography, the SiN cap in the contact region was etched away using CF_4-plasma. A contact metal stack consisted of Si/Ti/Al/Ti/Ni/Au layer was deposited, followed by a spike rapid thermal annealing with 5 s ramp time to 560 °C to form ohmic contacts. Finally, the 3 μm long gate was formed by depositing Ni/Au on the SiN cap. For E-mode HFETs, mesa-etching and ohmic contact lithography were first performed, using the same ohmic technology as the D-mode devices. The 2 μm long gate for E-mode devices was formed by depositing e-beam-Al_2O_3 (4 nm)/Ni/Au on the AlN barrier. Next, a 17 nm PECVD-SiN was deposited to induce a 2DEG in the access region. And finally, SiN over the contact pads was removed by RIE for testing. Hall effect measurements showed that the 17 nm PECVD-SiN on 1.5-nm-AlN/GaN induced a 2DEG with $\mu \sim 789$ cm^2/Vs, $n_s \sim 1.95 \times 10^{13}$ cm^{-2}, and R_{SH} of 406 Ω/sq.

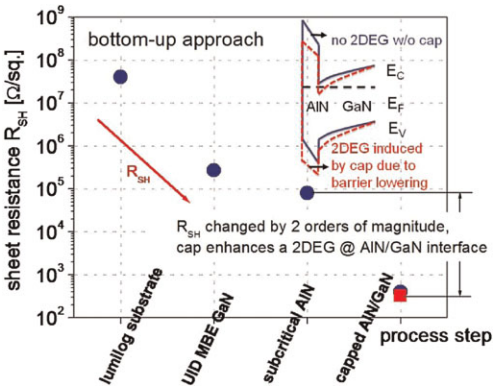


Figure 1 (online color at: www.pss-a.com) Evolution of sheet resistance shows MBE grown subcritical barrier 1.5 nm AlN/GaN heterostructures remain to be largely insulating, however, upon the capping material deposition the sheet resistance decreased to be as low as ~400 Ω/sq.

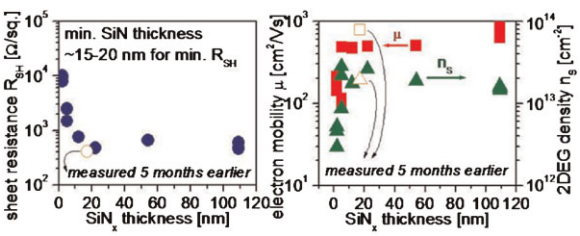


Figure 2 (online color at: www.pss-a.com) Hall effect measurements on SiN-capped subcritical barrier AlN(1.5 nm)/GaN structures. The sheet resistance decreases with increasing SiN thickness but keeps constant with a cap-thickness of more than ~15 nm.

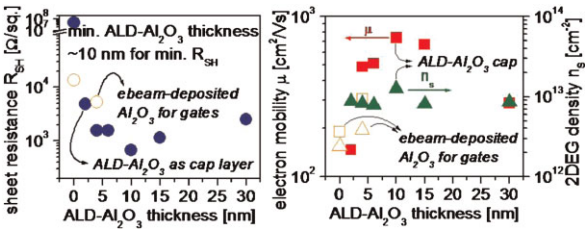


Figure 3 (online color at: www.pss-a.com) R_{SH} of ALD-Al_2O_3 capped subcritical barrier AlN(1.5 nm)/GaN structures minimizes at ~10 nm cap-thickness. Also shown are the results using e-beam-deposited Al_2O_3 cap.

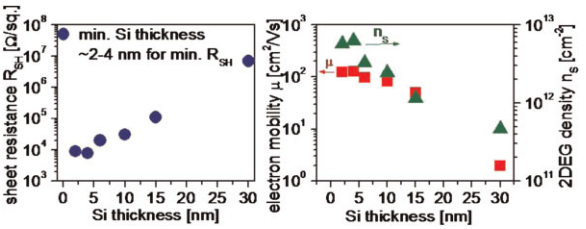


Figure 4 (online color at: www.pss-a.com) R_{SH} of Si-capped subcritical barrier AlN(1.5 nm)/GaN heterostructures minimizes at ~4 nm cap-thickness.

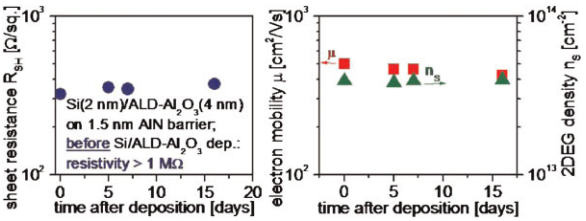


Figure 5 (online color at: www.pss-a.com) Reliability test for 2DEG induced by Si/ALD-Al_2O_3 layer on subcritical barrier AlN(1.5 nm)/GaN heterostructures. A single 2-nm silicon-layer induces similar 2DEGs, however, sheet resistance increases with time due to oxidation of Si in air.

3 Results and discussion Shown in Fig. 6, the E-mode device has a positive threshold voltage $V_{th} = 2.5$ V, a

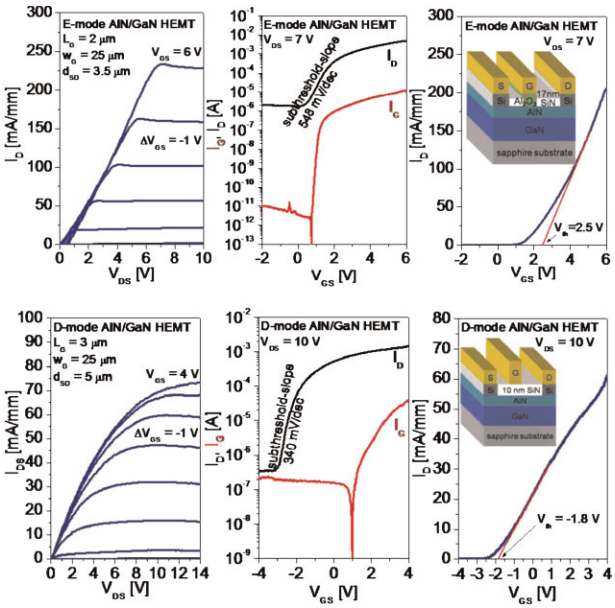


Figure 6 (online color at: www.pss-a.com) DC common-source family of I–V_s and transfer characteristics of E-mode HFET ($V_{th} = 2.5$ V, upper figures) and D-mode HFET ($V_{th} = -1.8$ V, lower figures) fabricated on the same subcritical barrier AlN/GaN structure. Cross-sections of completed devices are shown in the insets.

maximum output current of ~240 mA/mm, and an on/off ratio of ~10^3; the D-mode device has a negative threshold voltage $V_{th} = -1.8$ V, an output current of ~75 mA/mm, and an on/off ratio of ~10^3. Both devices showed higher subthreshold slopes due to background doping in the UID GaN buffer, which can be improved with polarization-engineered buffers recently developed in our laboratory [5].

Both types of devices exhibited relatively low-output currents, which is primarily due to the yet-to-be-optimized ohmic contacts showing contact resistances higher than 10 Ω/sq. The D-mode devices can also be improved by using Si/ALD-Al_2O_3/Ti gate [6]. The E/D-mode AlN/GaN inverter is operating at $V_{DD} = 5$ V (Fig. 7). This inverter consists of an E-mode driver with a threshold voltage $V_{th,e} = +1.1$ V and a D-mode active load with a threshold voltage $V_{th,d} = -1.2$ V. The gate-width of E- and D-mode HFETs is 25 μm and the gate-length is 3 and 2 μm, respectively. A high-operating voltage enables a high-inverter gain but is limited by the turn-on voltage of the gate-diode in the driver E-mode HFET. At $V_{DD} = 5$ V the inverter gain was found to be 8.5 and a transition voltage of 2.3 V was measured. A measure for the robustness of an inverter is the noise margin. High-state and low-state noise margins indicate the tolerable voltage range for which we interpret the inverter output as a logic 1 or 0. A maximum product criteria (MPC) [7] high-state noise margin of $V_{MH} = 1.57$ V was observed but the MPC low-state noise margin was found to be relatively low, $V_{ML} = 1.07$ V, stemming from a mismatch of the active load and driver output characteristics. Yet, the high gain and a reasonable low $\Delta V_{in} = V_{in,H} - V_{in,L} = 0.97$ V and high $\Delta V_{out} =$

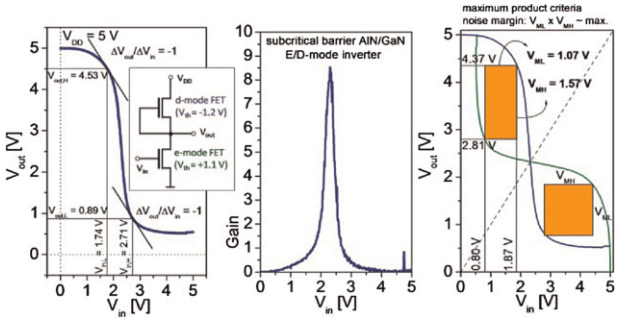


Figure 7 (online color at: www.pss-a.com) Voltage transfer characteristics of an inverter circuit with subcritical AlN barrier E- and D-mode HFETs at $V_{DD} = 5$ V, and the peak inverter gain was found to be 8.5. A MPC high-state noise margin V_{MH} and low-state noise margin V_{ML} was found to be 1.57 and 1.07 V, respectively.

$V_{out,H} - V_{out,L} = 3.64$ V are promising results for developing AlN/GaN-based circuits.

4 Conclusion We successfully demonstrated the concept of E- and D-mode HFETs based on subcritical barrier AlN/GaN heterostructures. By selectively patterning the highly insulating as-grown heterostructures with appropriate capping materials, 2DEG was induced in the access region and the gate region in the D-mode devices while the gate region in the E-mode devices remains to be largely insulating with e-beam-Al_2O_3 gate dielectrics.

To our best knowledge, this is the first report on E/D-mode inverters based on subcritical barrier AlN/GaN structures. Though the individual D- and E-mode device performance is far from optimal at this stage, this proof-of-concept demonstration indicates the distinct possibility of monolithic integration of III-nitride E/D digital logic circuitry based on the subcritical barrier AlN/GaN technology. Such nitride-based digital technology is expected to take advantage of the high-vertical scaling and possibly offer a building block for high-temperature digital electronics.

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References

[1] M. Higashiwaki, T. Mimura, and T. Matsui, IEEE Electron Device Lett. **27**(9), 719 (2006).
[2] T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. Xing, IEEE Electron Device Lett. **29**(7), 661 (2008).
[3] Y. Cao and D. Jena, Appl. Phys. Lett. **90**, 182112 (2007).
[4] N. Onojima, N. Hirose, T. Mimura, and T. Matsui, Appl. Phys. Lett. **93**, 223501 (2008).
[5] Y. Cao, T. Zimmermann, H. Xing, and D. Jena, Appl. Phys. Lett. **96**, 042102 (2010).
[6] G. Li, T. Zimmermann, Y. Cao, C. Lian, X. Xing, R. Wang, P. Fay, H. Xing, and D. Jena, IEEE Electron Device Lett. **31**(9), 954 (2010).
[7] R. John Hauser, IEEE Trans. Educ. **36**(4), 363 (1993).