InAlN/AlN/GaN HEMTs With Regrown Ohmic Contacts and f_T of 370 GHz

Yuanzheng Yue, *Member, IEEE*, Zongyang Hu, Jia Guo, *Student Member, IEEE*, Berardi Sensale-Rodriguez, *Student Member, IEEE*, Guowang Li, *Student Member, IEEE*, Ronghua Wang, Faiza Faria, Tian Fang, Bo Song, Xiang Gao, Shiping Guo, Thomas Kosel, Gregory Snider, *Senior Member, IEEE*, Patrick Fay, *Senior Member, IEEE*, Debdeep Jena, *Member, IEEE*, and Huili Xing, *Member, IEEE*

***Abstract*—We report 30-nm-gate-length InAlN/AlN/GaN/SiC high-electron-mobility transistors (HEMTs) with a record current gain cutoff frequency (f_T) of 370 GHz. The HEMT without back barrier exhibits an extrinsic transconductance ($g_{\mathrm{m.ext}}$) of 650 mS/mm and an on/off current ratio of 10^6 owing to the incorporation of dielectric-free passivation and regrown ohmic contacts with a contact resistance of 0.16 $\Omega \cdot$ mm. Delay analysis suggests that the high f_T is a result of low gate–drain parasitics associated with the rectangular gate. Although it appears possible to reach 500-GHz f_T by further reducing the gate length, it is imperative to investigate alternative structures that offer higher mobility/velocity while keeping the best possible electrostatic control in ultrascaled geometry.**

***Index Terms*—AlN, cutoff frequency, f_T, GaN, high-electron-mobility transistor (HEMT), InAlN, molecular beam epitaxy (MBE), regrown ohmic contacts, transistor.**

I. Introduction

ALTHOUGH the electron saturation velocity in GaN has been predicted to be higher than 2×10^7 cm/s, the current gain cutoff frequency f_T of the state-of-the-art GaN high-electron-mobility transistors (HEMTs) is still low, i.e., $<$ 350 GHz [1], [2], much lower than what has been demonstrated in InAs-based HEMTs, i.e., $>$ 650 GHz [3]. Lattice-matched $In_{0.17}Al_{0.83}N$/AlN/GaN heterostructures offer higher charge density for thin barrier thicknesses ($<$ 10 nm) due to stronger polarization discontinuity than the conventional AlGaN/GaN heterostructure [4]–[13], making them suitable for ultrascaled HEMTs. Recently, several groups have reported $f_T > 200$ GHz using InAlN/GaN heterostructures with alloyed ohmic contacts [8]–[13]. For example, Wang *et al.* demonstrated f_T of 210 GHz on a 66-nm-gate-length (L_g) HEMT with dielectric-free passivation (DFP) [10], Lee *et al.* demonstrated f_T of 300 GHz on a 30-nm-gate-length HEMT with InGaN back barrier and oxygen plasma treatment [13], and Tirelli *et al.* reported impressive and balanced f_T/f_{MAX} of 205/220 GHz using a T-gate with a footprint of 30 nm [2]. However, all these devices suffered from high contact resistance (R_c) of $> 0.3\ \Omega \cdot$ mm and high on-resistance (R_{on}) of $> 1\ \Omega \cdot$ mm due to the alloyed ohmic contacts and large source–drain distance (L_{sd}). To reduce R_c, several groups have successfully demonstrated low contact resistances using molecular beam epitaxy (MBE) regrown contacts in GaN-based HEMTs [14]–[17]. Shinohara *et al.* reported deeply scaled self-aligned gate AlN/GaN HEMTs with both f_T and f_{MAX} higher than 300 GHz by incorporating regrown ohmic contacts, AlGaN back barrier, $L_g \sim 20$ nm, and $L_{\mathrm{sd}} \sim 100$ nm [1].

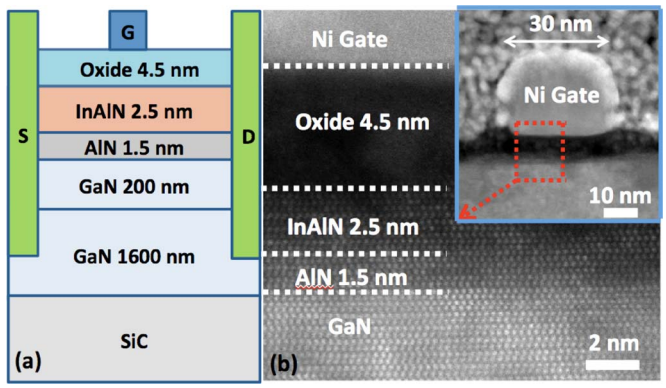


Fig. 1. (a) Schematic of the InAlN/AlN/GaN HEMT cross section and (b) high-resolution TEM and (inset) scanning TEM images confirming the HEMT layer structures and the 30-nm gate length after device fabrication.

To elucidate the details of electron transport in the device and thus gain insight into the fundamental limits of scaled GaN HEMTs, InAlN/AlN/GaN HEMTs with DFP, rectangular gates, and regrown ohmic contacts have been fabricated to achieve high current gain cutoff frequency f_T by minimizing parasitic effects. An f_T of 370 GHz was achieved in 30-nm-gate-length HEMTs without a back barrier, which is, to the best of our knowledge, the highest reported f_T in GaN-based transistors.

II. Experiments

The lattice-matched $In_{0.17}Al_{0.83}N$/AlN/GaN HEMT structure was grown by metal–organic chemical vapor deposition on a SiC substrate, consisting of, nominally, a 7.5-nm InAlN barrier, a 1.5-nm AlN spacer, a 200-nm UID GaN channel, and a 1.6-μm Fe-doped GaN buffer. The HEMT cross-sectional schematic is shown in Fig. 1 along with transmission electron

Manuscript received April 3, 2012; revised April 17, 2012; accepted April 20, 2012. Date of publication June 8, 2012; date of current version June 22, 2012. This work was supported in part by the Defense Advanced Research Projects Agency (John Albrecht, the NEXT program HR0011-10-C-0015) and in part by the Air Force Office of Scientific Research (Kitt Reinhardt and James Hwang). The review of this letter was arranged by Editor G. Meneghesso.

Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing are with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: yyue@nd.edu; zhu1@nd.edu; jguo@nd.edu; bsensale@nd.edu; gli1@nd.edu; rwang@nd.edu; ffaria@nd.edu; tfang@nd.edu; bsong@nd.edu; kosel@nd.edu; gsnider@nd.edu; pfay@nd.edu; djena@nd.edu; hxing@nd.edu).

X. Gao and S. Guo are with IQE RF LLC, Somerset, NJ 08873 USA (e-mail: xgao@iqep.com; sguo@iqep.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2012.2196751

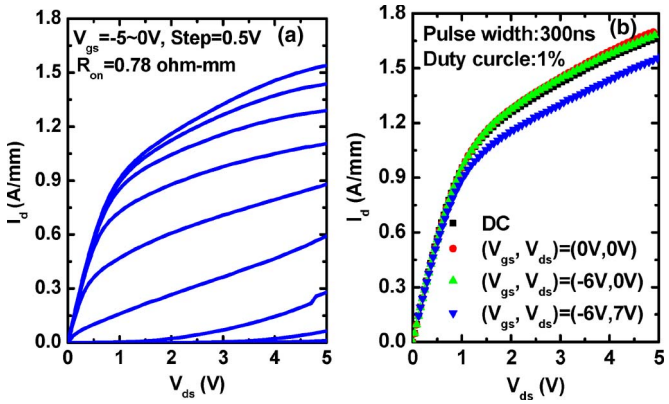


Fig. 2. (a) DC common source family of I–V's and (b) pulsed I–V measurements with 300-ns pulsewidth of the 30-nm 2×25 μm^2 gate InAlN/AlN/GaN HEMT with a source–drain spacing $L_{\rm sd}$ of 865 nm.

microscopy (TEM) images confirming the layer thicknesses and the gate length after device fabrication.

The device fabrication process started with patterning of SiO_2 mask for n^+ GaN ohmic regrowth by MBE. A regrowth well-to-well distance (i.e., $L_{\rm sd}$) of 865 nm was defined by stepper lithography for the reduction of parasitic resistance and capacitance. The preregrowth etch depth into the HEMT structure was 40 nm, and regrown n^+ GaN was 80 nm with a Si doping level of $\sim 1 \times 10^{20}$ cm^{-3}. The poly-GaN on top of SiO_2 was lifted off by BHF after regrowth. Nonalloyed ohmic contact of Ti/Au was deposited by electron-beam (e-beam) evaporation, followed by mesa isolation using chlorine-based plasma dry etching. Subsequently, the sample was blanket treated with DFP—an O_2-containing plasma process [10]—which results in an oxidized InAlN of about 4.5-nm thickness. Finally, 30-nm 2×25 μm^2 rectangular Ni gates were defined by e-beam lithography and liftoff. Further details on processing and regrowth can be found in [16] and [17]. The 2-D electron gas (2DEG) concentration and electron mobility are 1.92×10^{13} cm^{-2} and 1240 cm^2/V $\cdot$ s, respectively, leading to a sheet resistance of $\sim$262 Ω/sq, determined by the Hall effect measurement after the HEMTs were fabricated.

III. Results and Discussion

The contact resistance components were analyzed based on the transmission line method (TLM) measurements after the HEMTs were fabricated; in the analysis, all TLM dimensions were confirmed by scanning electron microscopy. From the TLM patterns with HEMT channel and regrown contacts, a total contact resistance of 0.16 $\Omega \cdot$ mm and a sheet resistance of 274 Ω/sq were extracted. From the TLM patterns with regrown n^+ GaN channel and contacts, a contact resistance of 0.06 $\Omega \cdot$ mm and a sheet resistance of 67 Ω/sq were obtained. The contact resistance between the regrown n^+ GaN and the 2DEG channel is thus calculated to be 0.08 $\Omega \cdot$ mm, which is higher than our previous reported value [17] likely due to the use of a plasma treatment before the regrowth.

Fig. 2(a) shows the dc common source family of I–V's of the 30-nm 2×25 μm^2 gate InAlN/AlN/GaN HEMT. A maximum drain current density I_d of 1.5 A/mm is obtained at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 5$ V. The device $R_{\rm on}$ extracted at $V_{\rm gs} = 0$ V and $V_{\rm ds}$ in the range between 0 and 0.5 V is 0.78 $\Omega \cdot$ mm, a result of adopting regrown contacts and reduced $L_{\rm sd}$ from our prior

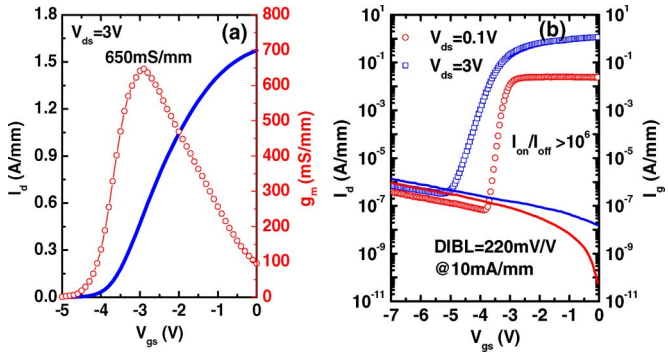
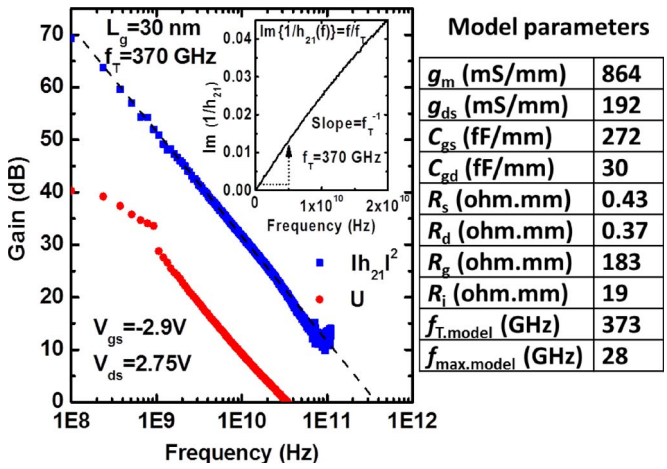


Fig. 3 Transfer characteristics of the InAlN/AlN/GaN HEMT at $V_{\rm ds} = 3$ V and 0.1 V: (a) Linear scale and (b) semilog scale.

work. This $R_{\rm on}$ value is higher than the sum of the source and drain resistances ($R_s + R_d = 0.54$ $\Omega \cdot$ mm) calculated based on the four-probe TLM result; the origin of the additional 0.24 $\Omega \cdot$ mm is yet unclear. Pulsed I–V measurements were used to investigate the surface passivation effectiveness of the DFP O_2 plasma treatment, as shown in Fig. 2(b) using 300-ns pulsewidth and 0.03-ms period. The cold pulsed drain current density at $V_{\rm gs} = 0$ V is slightly higher than that at dc owing to suppression of self-heating. No current collapse is observed in the gate lag measurement, a noteworthy improvement over previous reports in which only the access regions were subjected to DFP treatment [10]. A drain lag of 6% is observed, which merits further investigation.

Shown in Fig. 3 are the device transfer characteristics on the linear and semilog scales, with $V_{\rm gs}$ swept from 0 to -5 V. At $V_{\rm ds} = 3$ V, the threshold voltage $V_{\rm th}$ extracted from the linear extrapolation of I_d is -3.5 V, and the peak extrinsic transconductance $g_{\rm m.ext}$ is 650 mS/mm at $I_d \sim 535$ mA/mm. The drain-induced barrier lowering (DIBL) was measured to be 220 mV/V at $I_d = 10$ mA/mm, comparable to 174 mV/V reported in 20-nm gate GaN/AlN/GaN (2.5/3.5/20-nm) HEMTs with $Al_{0.08}$GaN back barrier [1]. Although the high DIBL value is indicative of significant short-channel effects, more than six orders of magnitude in the current on/off ratio was observed. This good pinchoff behavior of the HEMT is attributed to the low gate leakage resulting from the blanket DFP treatment. The three-terminal breakdown voltage at $I_d = 1$ mA/mm and $V_{\rm gs} = -12$ V is 30 V.

On-wafer device RF measurements were taken using an Agilent N5250C vector network analyzer from 250 MHz to 110 GHz. The network analyzer was calibrated using an off-wafer standard LRRM calibration, and on-wafer open and short structures were used to deembed the pad parasitics from the measured S-parameters. Fig. 4 shows the current gain $|h_{21}|^2$ and unilateral gain U of the device as functions of frequency at the peak f_T bias condition, $V_{\rm ds} = 2.75$ V, and $V_{\rm gs} = -2.9$ V. The extrapolation of $|h_{21}|^2$ with a -20-dB/dec slope gives f_T of 370 GHz after deembedding, from the predeembeded values of 160 GHz. The value of f_T in our device was also verified using Gummel's method [18], shown in the inset of Fig. 4. The low $f_{\rm MAX}$ of 30 GHz from the predeembeded values of 27 GHz is due to the high gate resistance induced by the rectangular gate. To the best of our knowledge, an f_T of 370 is the highest reported in any GaN-based HEMT. An $f_T \cdot L_g$ product of 11.1 GHz $\cdot$ μm was achieved, with a gate-length-to-barrier-thickness aspect ratio of 3.3.



Model parameters	
g_m (mS/mm)	864
g_{ds} (mS/mm)	192
C_{gs} (fF/mm)	272
C_{gd} (fF/mm)	30
R_s (ohm.mm)	0.43
R_d (ohm.mm)	0.37
R_g (ohm.mm)	183
R_i (ohm.mm)	19
$f_{T.model}$ (GHz)	373
$f_{max.model}$ (GHz)	28

Fig. 4. Small-signal RF characteristics of the InAlN/AlN/GaN HEMT showing f_T of 370 GHz and the table of extracted equivalent circuit parameters.

Also shown in Fig. 4 are the extracted equivalent circuit model parameter values obtained from the measured S-parameters; good agreement between the simulated and measured $f_T/f_{\rm MAX}$ values is obtained. A transistor delay analysis in the style of Moll *et al.* [19] results in an intrinsic delay $\tau_{\rm int}$ of 0.282 ps, a drain delay $\tau_{\rm drain}$ of 0.045 ps, and a channel charging delay $\tau_{\rm cc}$ of 0.103 ps. For HEMTs with relatively low mobilities such as in GaN, a significant part of $\tau_{\rm cc}$ actually describes the time for carriers to accelerate to the saturation velocity under the gate on the source side [20]. We thus recalculated the gate delay $\tau_{\rm gate}$ to be $\tau_{\rm int} + (\tau_{\rm cc} - C^*_{\rm gd}(R_s + R_d)) = 0.361$ ps. Since the parasitic $C_{\rm gs}$ and $C_{\rm gd}$ are minimized in our device owing to the rectangular gate, we can estimate the effective electron velocity to be $\sim 1 \times 10^7$ cm/s, assuming an effective gate length of 40–50 nm by taking into account charge depletion toward drain and source under the peak f_T bias condition. This velocity, as well as the positive bias-dependent drain delay (0.02 ps/V in our device), is similar to the observations in Shinohara's unscaled devices ($L_{\rm sd}$ of 1000 nm) [1]. Given that the gate delay dominates the total delay ($\sim$80%), it appears possible to achieve f_T of 500 GHz ($\sim$0.33-ps total delay) by further reducing the gate length. To enhance $f_{\rm MAX}$, however, aside from keeping the parasitics low, it is imperative to improve the intrinsic g_m in ultrascaled devices with the best possible electrostatic control, which can be potentially realized in quantum-well AlN/GaN/AlN structures [21].

IV. Conclusion

We have reported a record current gain cutoff frequency of 370 GHz in InAlN/AlN/GaN HEMTs on a SiC substrate without back barrier. The delay analysis shows that the high f_T obtained can be attributed to the reduction of parasitic effects and further improvement is possible by shrinking the gate length.

References

[1] K. Shinohara, D. Regan, A. Corrion, D. Brown, S. Burnham, P. J. Willadsen, I. Alvarado-Rodriguez, M. Cunningham, C. Butler, A. Schmitz, S. Kim, B. Holden, D. Chang, V. Lee, A. Ohoka, P. M. Asbeck, and M. Micovic, "Deeply-scaled self-aligned-gate GaN DH-HEMTs with ultrahigh cutoff frequency," in *IEDM Tech. Dig.*, 2011, pp. 19.1.1–19.1.4.

[2] S. Tirelli, D. Marti, H. Sun, A. R. Alt, J.-F. Carlin, N. Grandjean, and C. R. Bolognesi, "Fully passivated InAlN/GaN HEMTs with $f_{\rm T}/f_{\rm MAX}$ of 205/220 GHz," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1364–1366, Oct. 2011.

[3] D. Kim, B. Brar, and J. del Alamo, "$f_{\rm T} = 688$ GHz and $f_{\rm MAX} = 800$ GHz in $L_{\rm g} = 40$ nm $In_{0.7}Ga_{0.3}As$ MHEMTs with $g_{\rm m\_max} > 2.7$ mS/um," in *IEDM Tech. Dig.*, 2011, pp. 13.6.1–13.6.4.

[4] J. Kuzmik, "Power electronics on InAlN/(In)GaN: Prospect for a record performance," *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 510–512, Nov. 2001.

[5] R. Wang, P. Saunier, X. Xing, C. Lian, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Gate-recessed enhancement-mode InAlN/AlN/GaN HEMTs with 1.9 A/mm drain current density and 800 mS/mm transconductance," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1383–1385, Dec. 2010.

[6] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 309–311, Mar. 2011.

[7] Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng, and L. Liu, "AlGaN/GaN MOS-HEMT with HfO_2 dielectric and Al_2O_3 interfacial passivation layer grown by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 838–840, Aug. 2008.

[8] H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J.-F. Carlin, M. Gonschorek, N. Grandjean, and C. R. Bolognesi, "205-GHz (Al, In)N/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 957–959, Sep. 2010.

[9] R. Wang, G. Li, J. Verma, B. Sensale, T. Fang, J. Guo, Z. Y. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, "220-GHz quaternary barrier InAlGaN/AlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1215–1217, Sep. 2011.

[10] R. Wang, G. Li, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, "210-GHz InAlN/GaN HEMTs with dielectric-free passivation," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 892–894, Jul. 2011.

[11] R. Wang, G. Li, J. Verma, T. Zimmermann, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. Xing, "Si-containing recessed ohmic contacts and 210 GHz quaternary barrier InAlGaN high electron mobility transistors," *Appl. Phys. Exp.*, vol. 4, no. 9, pp. 096502-1–096502-3, 2011.

[12] D. Lee, J. Chung, H. Wang, X. Gao, S. Guo, P. Fay, and T. Palacios, "245-GHz InAlN/GaN HEMTs with oxygen plasma treatment," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 755–757, Jun. 2011.

[13] D. Lee, X. Gao, S. Guo, D. Kopp, P. Fay, and T. Palacios, "300-GHz InAlN/GaN HEMTs with InGaN back barrier," *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1525–1527, Nov. 2011.

[14] S. Dasgupta, Nidhi, D. Brown, F. Wu, S. Keller, J. Speck, and U. K. Mishra, "Ultralow nonalloyed ohmic contact resistance to self aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth," *Appl. Phys. Lett.*, vol. 96, pp. 143 504-1–143 504-3, Apr. 2010.

[15] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. J. Willadsen, C. Butler, A. Schmitz, D. Wheeler, A. Fung, and M. Micovic, "220 GHz $f_{\rm T}$ and 400 GHz $f_{\rm MAX}$ in 40-nm GaN DH-HEMTs with re-grown ohmic," in *IEDM Tech. Dig.*, 2010, pp. 30.1.1–30.1.4.

[16] J. Guo, Y. Cao, C. Lian, T. Zimmermann, G. Li, J. Verma, X. Gao, S. Guo, P. Saunier, D. Jena, and H. Xing, "Metal-face InAlN/AlN/GaN high electron mobility transistors with regrown ohmic contacts by molecular beam epitaxy," *Phys. Stat. Sol. (A)*, vol. 208, no. 7, pp. 1617–1619, Jul. 2011.

[17] J. Guo, G. Li, F. Faria, Y. Cao, R. Wang, J. Verma, X. Gao, S. Guo, E. Beam, A. Ketterson, M. Schuette, P. Saunier, M. Wistey, D. Jena, and H. Xing, "MBE regrown ohmics in InAlN HEMTs with a regrowth interface resistance of 0.05 ohm-mm," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 525–527, Apr. 2012.

[18] H. K. Gummel, "On the definition of the cutoff frequency $f_{\rm T}$," *Proc. IEEE*, vol. 57, no. 12, p. 2159, Dec. 1969.

[19] N. Moll, M. R. Hueschen, and A. Fischer-Colbrie, "Pulse-doped AlGaAs/InGaAs pseudomorphic MODFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 7, pp. 879–896, Jul. 1988.

[20] Y. Kwon and D. Pavlidis, "Delay time analysis of submicron InP-based HEMT's," *IEEE Trans. Electron Devices*, vol. 43, no. 2, pp. 228–237, Feb. 1996.

[21] G. Li, R. Wang, J. Guo, J. Verma, Z. Hu, Y. Yue, F. Faria, Y. Cao, M. Kelly, T. Kosel, H. G. Xing, and D. Jena, "Ultra-thin body GaN-on-insulator quantum well FETs with regrown ohmic contacts," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 661–663, May 2012.