Fabrication of top-gated epitaxial graphene nanoribbon FETs using hydrogen-silsesquioxane

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(Received 28 December 2011; accepted 23 February 2012; published 12 March 2012)

Top-gated epitaxial graphene nanoribbon (EGNR) field effect transistors (FETs) were fabricated on epitaxial graphene substrates which demonstrated the opening of a substantial bandgap. Hydrogen silsesquioxane (HSQ) was used for the patterning of 10 nm size linewidth as well as a seed layer for atomic layer deposition (ALD) of a high-k dielectric aluminum oxide (Al_2O_3). It is found that the resolution of the patterning is affected by the development temperature, electron beam dose, and substrate materials. The chosen gate stack of HSQ followed by Al_2O_3 ALD permits stable device performance and enables the demonstration of the EGNR-FET. © *2012 American Vacuum Society*. [http://dx.doi.org/10.1116/1.3693593]

I. INTRODUCTION

Graphene has been investigated as one of the promising candidates to replace current channel materials for a field effect transistor (FET) due to its high carrier mobility for both electrons and holes.[1] In spite of its excellent electronic properties, the lack of significant bandgap is a major obstacle to compete with other candidate materials. In fact, it has been demonstrated that a bandgap can be created in graphene by quantum confinement of the carriers in patterned nanometer size graphene nanoribbons (GNRs).[2] However, to date, most GNRs have been fabricated from exfoliated graphene and operated by back gates,[3,4] in this configuration; formation of gate stack is inconsistent with standard metal oxide silicon (MOS) transistor processing. Furthermore, the formation of GNRs produced by gas phase chemical approach has uncontrollable and irreproducible results.[5–7] Therefore, it is important to demonstrate GNR properties fabricated by conventional semiconductor device processing methods and operated in the conventional manner (top-gated) on large-size wafer. In this work, we report the fabrication of top-gated epitaxial graphene (graphene on Si-face SiC) GNR (EGNR) transistors, which satisfies the desired fabrications methods and conventional structure. Further, these EGNR-FETs demonstrate the opening of a substantial bandgap.

II. EXPERIMENTAL PROCEDURES

Epitaxial graphene was formed on nominally on-axis, semi-insulating (0001) 6H-SiC substrates at 1620 °C for 2 h in an Ar ambient at 100 mbar (Ref. 8) and then cooled in Ar to 800 °C; prior to graphene formation, the substrates were etched in H_2 at about 1550 °C. Hydrogen silsesquioxane (HSQ) diluted with methylisobutylketone was used as an electron-beam resist to form sub-10-nm EGNRs. The HSQ was coated on the graphene/SiC wafer at speed of 4000 rpm for 30 s followed by baking at 120 °C for 2 min and at 170 °C for 2 min, respectively. The thickness of HSQ film is measured to be 20 nm by atomic force microscopy. The wafer was then exposed to an electron beam with an acceleration voltage of 75 kV and beams current of 50 pA to define the EGNR. After exposure, the wafer was developed by immersion in a solution of tetramethyl ammonium hydroxide (TMAH) at elevated temperature. After forming the HSQ mask, uncovered graphene was etched in O_2 plasma at reactive ion etcher power of 150 W, 25 mTorr, and 25 sccm of O_2 flow. Finally the EGNR was formed after removing the HSQ mask in buffed hydrochloric acid (BHF) and then new HSQ was coated at the channel region followed by atomic layer deposited (ALD) Al_2O_3 at 200 °C. The thickness of Al_2O_3 is 30 nm and HSQ is 20 nm and the measured capacitance (@$V_{GS} = 0$ V, 100 kHz) is 7.41×10^{-8} F cm^{-2}. In this work, HSQ was used not only as an EGNR patterning mask but also as the seeding layer for the ALD deposition of Al_2O_3. After removing the first HSQ in BHF, the second HSQ was formed and latter was used as a seeding layer for the ALD. A stack of Cr (5 nm)/Au (100 nm) using electron-beam evaporator was used for both gate electrode and source/drain contacts. The EGNR is connected to the two dimensional (2D) graphene areas and the contact metal was seated on the 2D area.

III. RESULTS AND DISCUSSION

Figure 1(a) shows the linewidth of patterned HSQ as a function of electron beam line dose (nC/cm) at two different development temperatures. It is observed that the width of HSQ pattern is proportional to the line dose of the electron beam at each development temperature. Figure 1(b) shows scanning electron microscope (SEM) images of HSQ linewidth depending on different line dose of the electron beam and different development temperature. Even though a 10

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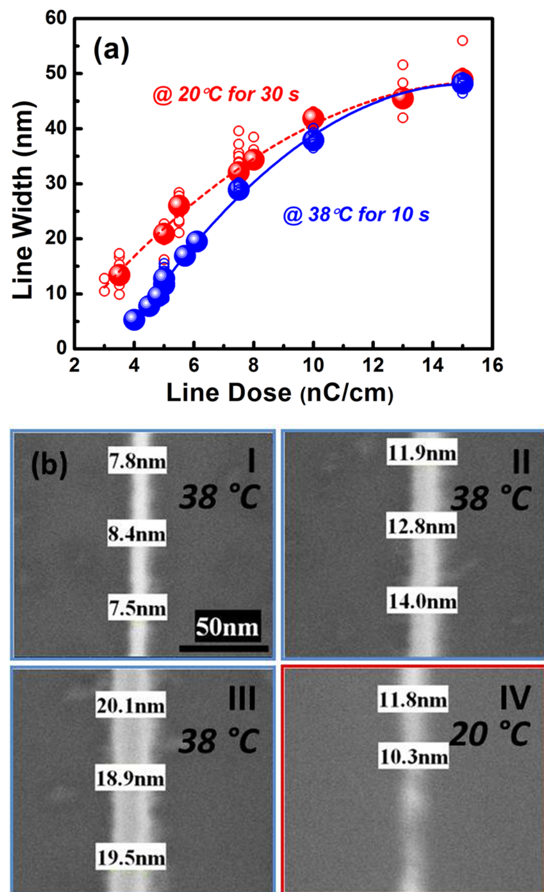

FIG. 1. (Color online) (a) HSQ linewidth (thickness of 20 nm) on graphene as a function of line dose of electron beam lithography at two different developer temperatures. (b) SEM images of HSQ linewidth depending on different line dose of electron beam lithography: I (4.5 nC/cm), II (5 nC/cm), and III (6 nC/cm), respectively, at a developer temperature of 38 °C and IV (3.5 nC/cm) at a developer temperature of 20 °C.

nm linewidth can be achieved using the room temperature development, the line is incomplete and discontinuous, whereas at the elevated development temperature those lines become complete and continuous. It reveals that at higher development temperature the resolution of HSQ patterns increases. In addition, the uniformity becomes better at elevated temperature. This is attributed to the increase of differential dissolution rate between exposed and unexposed regions at higher development temperature.[9,10] Too high development temperature shortens the developing time and causes the loss of process margin. If the developing time is not sufficient, webbed-feet like residue appear between lines. On the other hand, swelling of the HSQ line was observed under the over-developing condition.

Formation of array and even grid pattern is another method to verify the efficacy of process parameters such as resist thickness, baking temperature/time, electron beam lithography (EBL) conditions, and development conditions. Based on the process recipe from Fig. 1, both array and grid patterns were formed as shown in Fig. 2, respectively. Figures 2(a) and 2(b) show that array patterns of 12 nm linewidth (white) with spacing (black) of 10 nm and grid patterns of 15 nm linewidth (white) with spacing (black) of 30 nm. The 22 nm pitch of HSQ patterns on wafer-size substrate in this work are the smallest feature dimension ever reported.[9] These results are possible due to the superior resolution and low root mean square roughness of HSQ films as well as hydrophobic properties of graphene surface. In addition, these results are highly dependent on the substrate materials.

Previous reports indicate that these nanoscale patterns, especially array patterns, can be easily collapsed during the development or rinse processes, and often a critical point drying (CPD) method is necessary to prevent such collapse.[11] This work reveals that HSQ patterning of nanometer size can be achieved on the graphene surface without the CPD method. Figure 3 shows the behavior of the HSQ array pattern during the development process depends on the properties of the substrate (hydrophobic substrate: graphene versus hydrophilic substrate: SiO_2). It shows that when HSQ pattern is formed on the SiO_2 substrate, the aqueous solution of TMAH or rinse deionized water remains on the surface. The remaining solution near the HSQ sidewall causes the surface tension toward the HSQ sidewall surface during dry process; finally leading to collapse of the array patterns. The substrate material dependence of patterning implies that the graphene layer can be used as a buffer layer for formation of the extreme small patterning by changing the polarity of the

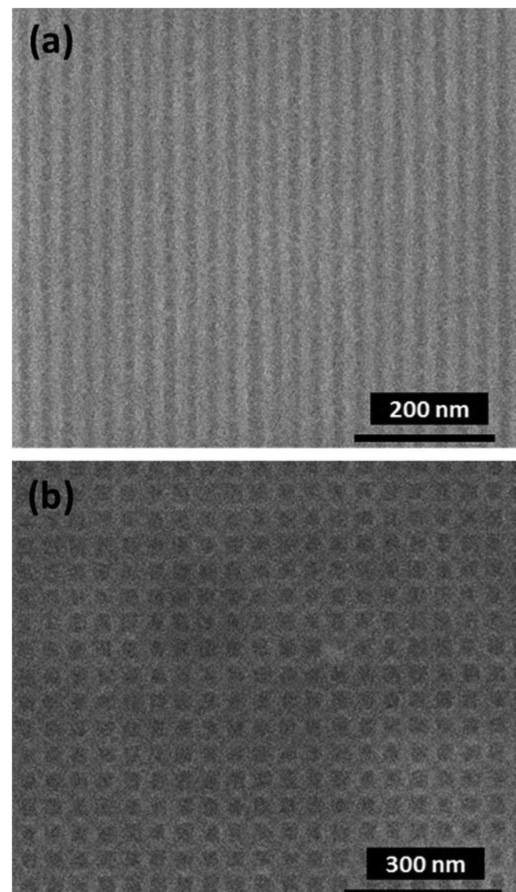

FIG. 2. SEM images of (a) array HSQ line, the linewidth (white) of 12 nm and space (black) of 10 nm, and (b) HSQ grid pattern, the linewidth (white) of 15 nm and space (black) of 30 nm.

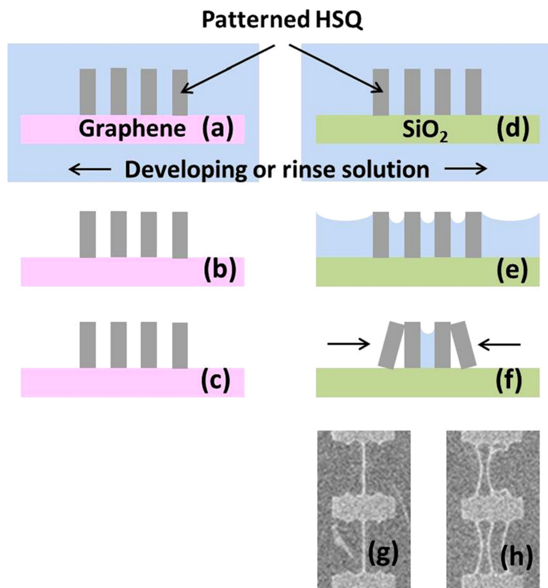

FIG. 3. (Color online) Schematic pictures of HSQ patterns on graphene (a)–(c) and on SiO_2 (d)–(h). Both (a) and (d) represents the situation during the developing or rinse solution. Both (b) and (e) represent the situation after taking out from the solution. Both (c) and (f) represent the situation during the dry in N_2 gas. (g) Single HSQ pattern and (h) array HSQ pattern representing the distortion of line due to the surface tension during the dry process.

surface. The schematic shown in Fig. 3(f) is representative of the SEM image as shown in Fig. 3(h). The array patterns collapse as shown in Fig. 3(h), while the single pattern does not collapse as shown in Fig. 3(g). The stress caused by rinse solution can be expressed by following equation:[11]

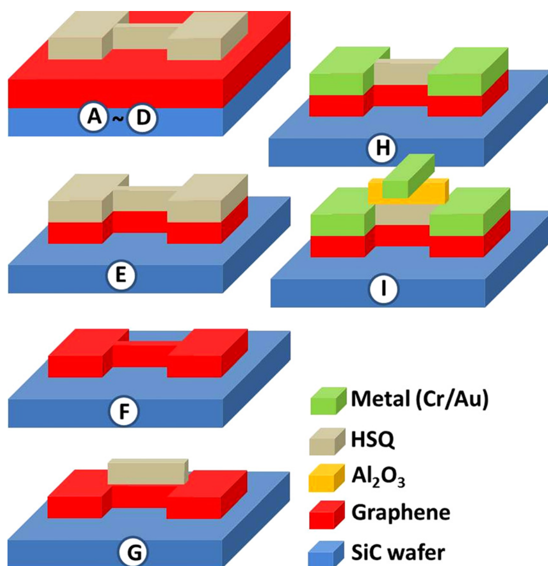

FIG. 4. (Color online) Schematic process flow of the EGNR-FET: (A) Starting with epigraphene on SiC, (B) coating and baking HSQ (4000 rpm and 120/170 °C for 2 min, respectively, (C) E-beam lithography (75 kV and 50 pA), (D) development, (E) etching of graphene in O_2 plasma, (F) removal of HSQ by BHF, (G) another HSQ for gate dielectric, (H) metal contact for source and drain, (I) Al_2O_3 ALD followed by gate metal.

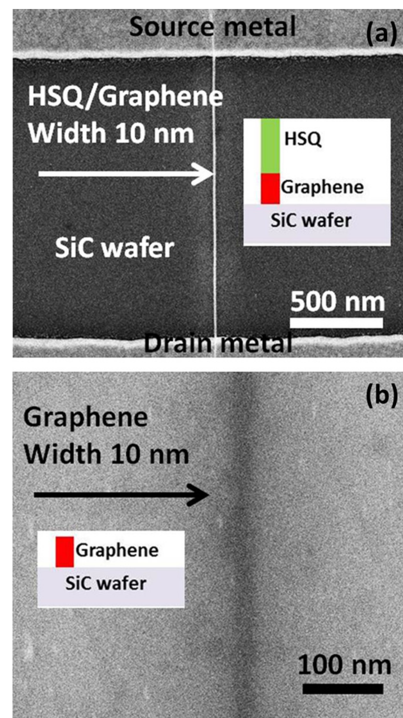

FIG. 5. (Color online) (a) SEM image of HSQ pattern with source and drain metal electrode. (b) SEM image of graphene line after removing HSQ pattern in buffered hydrofluoric acid (BHF).

$$\sigma = \frac{6\gamma\cos\theta}{D}\left(\frac{H}{W}\right)^2.$$

The stress (σ) forced on the side wall of a line by capillary force is related to the height (H) and width (W) of the line, surface tension of the rinse solution (γ), contact angle between HSQ and the rinse solution (θ), and the line space (D). As seen in this equation, the aspect ratio of the HSQ line is the critical parameter. For the single line case, all of the patterns remain in a good shape for an aspect ratio of 5 (width of 11 nm with height of 55 nm), yet all of the patterns collapse once the aspect ratio becomes higher than 7 (width of 8 nm with height of 55 nm). As the aspect ratio increases from 5 to 7, the stress toward sidewall of the line doubles. A

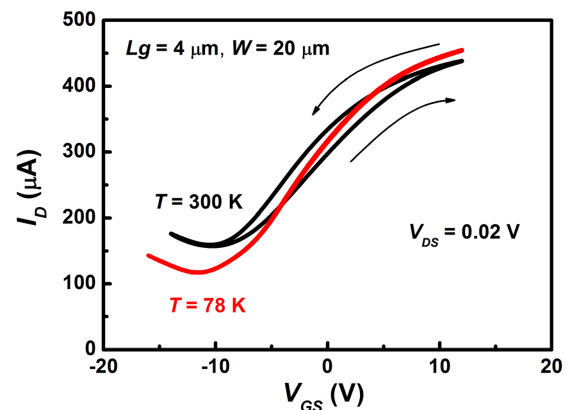

FIG. 6. (Color online) I_D vs V_{GS} of 2D EG-FET at 300 and 78 K, respectively. The gate dielectrics stack consists of Al_2O_3 on HSQ.

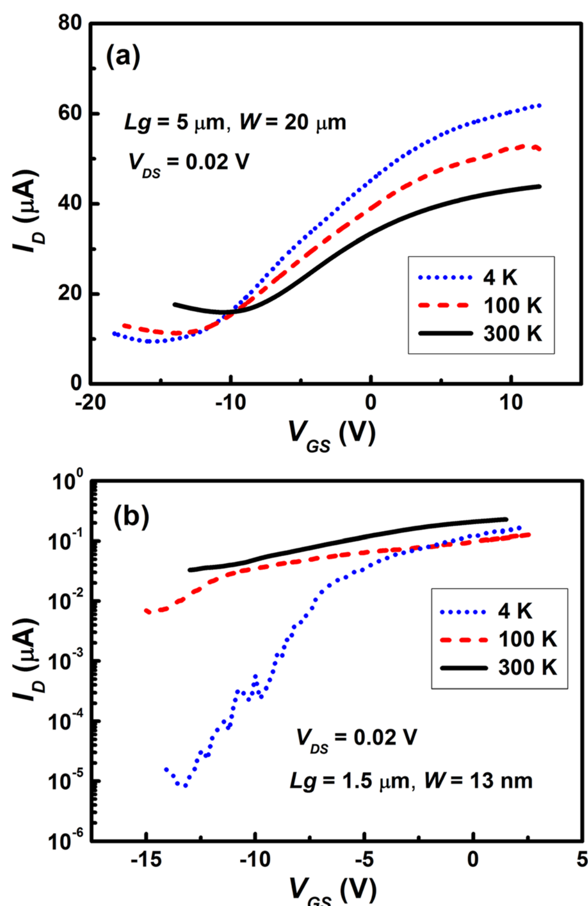

FIG. 7. (Color online) I_D vs V_{GS} of (a) 2D EG-FET and (b) 13 nm width EGNR-FET at various temperatures.

schematic picture of the above process flow for EGNR-FET is shown in Fig. 4.

Figure 5(a) shows a 10 nm width HSQ pattern with source and drain metal electrodes at the end of the line. The HSQ patterns were successfully transferred into epitaxial graphene by oxygen plasma etching, leading to EGNRs with line widths of ∼10 nm as shown in Fig. 5(b).

Before fabrication of an EGNR-FET, the properties of the gate stack was characterized using two dimensional epitaxial graphene (2D-EG) field effect transistor (FET) since 2D-EG-FET results can be used to reflect the gate stack quality without consideration of the edge effect of EGNR-FET. Figure 6 shows a hysteresis curve of I_D vs V_{GS} at 300 and 78 K, respectively. While a small hysteresis is observed at 300 K, negligible hysteresis is observed at 78 K. Note that the small hysteresis observed at 300 K is mainly caused by traps in the compound gate dielectric bulk, and more importantly, the Dirac point is unchanged. This implies that the interface between graphene and gate dielectric is robust during the device operation. This result suggests that a stack of gate dielectrics (Al_2O_3/HSQ) on graphene leads to stable device performance and can be implemented to investigate EGNR-FET.

Figure 7 shows an I_D vs V_{GS} of a 2D-EG-FET as shown in Fig. 7(a) and an EGNR-FET as shown in Fig. 7(b) at various temperatures. While there is a negligible temperature dependence of the minimum current at charge neutral point for 2D-EG-FET, there is a significant temperature dependence of the minimum current at charge neutral point for EGNR-FET. This strong temperature dependence of EGNR-FET, as shown in Fig. 7(b), indicates the presence of a potential barrier in the channel region; in other words, an opening of a bandgap in the channel.[12] A detailed analysis and discussion of this bandgap will be presented in a future paper.

IV. CONCLUSIONS

In conclusion, a top-gated EGNR-FET having performance characteristics indicative of a bandgap was fabricated. For the patterning of 10 nm size linewidth (smallest ever reported), hydrogen silsesquioxane (HSQ) was used. HSQ is also used in a subsequent step as a seeding layer for an ALD. It is found that the resolution of the patterning is affected by the HSQ development temperature and substrate material. With the hydrophobic properties of graphene, a stable array pattern can be achieved without distortion and collapse or the need for critical point drying methods. The chosen gate stack of ALD Al_2O_3 and HSQ shows stable I_D vs V_{GS} characterization and enables demonstration of an EGNR-FET.

ACKNOWLEDGMENTS

This work was supported by the Semiconductor Research Corporation (SRC), Nanoelectronics Research Initiative (NRI), and the National Institute of Standards and Technology (NIST) through the Midwest Institute for Nanoelectronics Discovery (MIND) and, in part, by the Office of Naval Research (ONR) and National Science Foundation (NSF). All work conducted at the U.S. Naval Research Laboratory is supported by the Office of Naval Research.

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