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High-mobility and low-power thin-film transistors based on multilayer MoS₂ crystals

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Unlike graphene, the existence of bandgaps (1–2 eV) in the layered semiconductor molybdenum disulphide, combined with mobility enhancement by dielectric engineering, offers an attractive possibility of using single-layer molybdenum disulphide field-effect transistors in low-power switching devices. However, the complicated process of fabricating single-layer molybdenum disulphide with an additional high-*k* dielectric layer may significantly limit its compatibility with commercial fabrication. Here we show the first comprehensive investigation of process-friendly multilayer molybdenum disulphide field-effect transistors to demonstrate a compelling case for their applications in thin-film transistors. Our multilayer molybdenum disulphide field-effect transistors exhibited high mobilities ($>100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), near-ideal subthreshold swings ($\sim 70 \text{ mV}$ per decade) and robust current saturation over a large voltage window. With simulations based on Shockley's long-channel transistor model and calculations of scattering mechanisms, these results provide potentially important implications in the fabrication of high-resolution large-area displays and further scientific investigation of various physical properties expected in other layered semiconductors.

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The discovery of graphene opened the door to the exotic electronic, optical and mechanical properties of two-dimensional (2D) crystals¹. Graphene has a conical Dirac spectrum of energy states without a bandgap and a linear dispersion. While these properties are the root of much of the novel electronic and optical phenomena of graphene, the gapless bandstructure also makes it unsuitable for conventional transistors for electronic switching. Similar to the storyline of the graphite and graphene family, transition metal dichalcogenides of the form MX_2 where M = metal and X = S, Se or Te are emerging as highly attractive candidates for the study of fundamental physics in 2D and in layered (thin-film) structures. These materials form layered structures, where layers of covalently bonded X–M–X atoms are held together by Van der Waals interactions. But, because of the broken symmetry in the atomic basis, they can have bandgaps of ~ 1 eV.

Among these layered semiconductors, recently, special emphasis has been given to single-layer (SL) MoS_2 owing to its intriguing electrical and optical properties. While bulk MoS_2 is usually an *n*-type semiconductor with an indirect bandgap (~ 1.3 eV)² and carrier mobility in the $50\text{--}200\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ range at room temperature³, SL MoS_2 is found⁴ to have a direct bandgap of ~ 1.8 eV. Field-effect transistors (FETs) using SL MoS_2 exhibited high on/off ratios ($\sim 10^8$) and low subthreshold swing (SS, ~ 70 mV per decade)⁵. The electron mobility of SL MoS_2 FETs varied from $\sim 1\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ (in air/ $\text{MoS}_2/\text{SiO}_2$ structures) to $\sim 200\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ (in $\text{HfO}_2/\text{MoS}_2/\text{SiO}_2$ structures) depending on dielectric environment. Thus, in addition to fundamental scientific interest, SL MoS_2 FETs can be an attractive alternative for electronic switches in the form of thin-film transistors (TFTs) for high-resolution liquid crystal displays and organic light-emitting diode (OLED) displays. These devices have a critical need for high field-effect mobility ($> 30\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$), high on/off ratio ($> 10^3$), steep-subthreshold slopes for low power consumption, and electrical and optical reliabilities⁶. But, the synthesis of SL MoS_2 followed by a deposition of an additional high-*k* dielectric layer may not be well suited for commercial fabrication processes. Based on the physics of MoS_2 , we identify a number of reasons why multilayer MoS_2 can be more attractive for TFT application than SL MoS_2 . The density of states of multilayer MoS_2 is three times that of SL MoS_2 , which will lead to considerably high drive currents in the ballistic limit. In long-channel TFTs, multiple conducting channels can be created by field effect in multilayer MoS_2 for boosting the current drive of TFTs, similar to silicon-on-insulator MOSFETs.

However, multilayer MoS_2 and corresponding dichalcogenide semiconductors have not been extensively studied for use in electronics. The characteristics in the few early reports^{7,8} are not vastly competitive with current TFT technologies. Therefore, in this work, we explore the case of multilayer MoS_2 FETs further and show that it offers a compelling case for applications in TFTs. We report the first demonstration of multilayer MoS_2 FETs with single back-gated insulator of 50-nm-thick Al_2O_3 by atomic layer deposition (ALD) achieving high room-temperature mobilities ($> 100\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$) and very low SS (~ 70 mV per decade), which suggest that, with a proper use of a dielectric substrate, the mobility and the SS in multilayer MoS_2 FETs may reach near the intrinsic limits at room temperature. We also demonstrate robust current saturation over a large voltage window. This is an important step towards real applications as TFTs in OLED displays are operated in the saturation region of drain current. Such saturation is elusive in FETs based on nanomaterials owing to poor electrostatic control, or exists in a very small voltage window in graphene owing to the lack of a bandgap⁹. We describe the experimental results with comprehensive simulations based on Shockley's long-channel transistor model and calculations of scattering mechanisms, and further suggest future directions to improve mobility in layered semiconductors.

Results

Device fabrication. TFTs based on multilayer MoS_2 were fabricated with the architecture shown in Fig. 1a. After multilayer MoS_2 flakes were mechanically exfoliated from bulk MoS_2 crystals and transferred on ALD- Al_2O_3 -covered Si substrates, electrical contacts of Au/Ti were patterned on top of MoS_2 flakes as described in the Methods section. Optical micrograph of a completed device is shown in Fig. 1b. The thickness of MoS_2 channels measured by atomic force microscope (AFM) was in the range of 20–80 nm. Between the two stacking polytypes that are observed in bulk MoS_2 crystals (hexagonal 2H and rhombohedral 3R)¹⁰, crystal orientation mapping by electron backscatter diffraction indicated only 2H MoS_2 within the measured devices as shown in Fig. 1c. Subsequent inverse pole figure in Fig. 1c confirmed that the MoS_2 channels are (0001)-oriented single crystals. Raman spectra of MoS_2 channels were almost identical with those of bulk single crystals as shown in Fig. 1d, and no noticeable difference in Raman shifts of MoS_2 channels were found among measured devices, indicating minimal structural modifications.

Electronic properties. Figure 2 shows the measured device characteristics of a multilayer MoS_2 TFT. The thickness of the MoS_2 layer is $t_{\text{ch}} \sim 30$ nm, and the back gate oxide thickness is $t_{\text{ox}} \sim 50$ nm (Fig. 2a). Figure 2b shows the major features observed: the *n*-type nature of the MoS_2 layer as indicated by it turning on at positive gate biases owing to accumulation of electrons, and a window of gate biases where the device stays off (depletion). This feature was observed in all measured devices, but a fraction of the devices also showed a recovery of the current at large negative gate biases as in Fig. 2b, which is a clear indication of an inversion channel. The inversion layer formation is described further in Supplementary Fig. S4 and in the Supplementary methods. We note that the gate capacitance in this geometry is ~ 20 times higher than a recent report⁷. As a result, while exhibiting the high on/off ratio expected of a semiconductor with a bandgap of 1.3 eV, a sharp SS (~ 80 mV per decade for Fig. 2, 70 mV per decade for some devices) is also measured at room temperature in deep depletion. In a typical field-effect geometry, the subthreshold slope is given by¹¹ $\text{SS} = (1 + (C_S + C_{\text{it}})/C_{\text{ox}}) kT/q \ln 10$, where C_S is the capacitance in the MoS_2 conducting channel, $C_{\text{it}} = qD_{\text{it}}$ is the capacitance owing to interface traps of density D_{it} and $C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}}$ is the oxide capacitance. Based on this model, $(C_S + C_{\text{it}}) \sim C_{\text{ox}}/3$. As the semiconductor capacitance is negligible in the deep-subthreshold region, the interface trap density is $D_{\text{it}} \sim 2.6 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, a very low value indeed¹². The SS value was measured to be ~ 24 mV per decade at 77 K, indicating D_{it} does not vary with temperature. We note that similar to the recent report⁵ for monolayer MoS_2 , the subthreshold slope (and D_{it}) of multilayer MoS_2 TFTs is also exceptionally low, comparable to state-of-the-art silicon transistors. But it is obtained without the decades of processing improvement that was necessary to reduce interface trap densities between the dielectric insulator and silicon. Currently III–V semiconductors are facing the same challenge¹³. This is because of the layered nature of the semiconductor—for 2D crystals and their stacks, there are no out-of-plane broken bonds, and thus the interface traps are expected to be in the dielectrics and materials placed in contact with them, not in the semiconductor itself. This is a major advantage of MoS_2 for TFT applications.

Current saturation. The second major boost is seen in Fig. 2c. The drain current is observed to saturate at high drain biases for all gate voltages. The saturation occurs over a wide drain voltage window (unlike graphene). This is the first observation of a robust current saturation in a layered semiconductor composed of 2D crystals. Current saturation in transistors is an important feature towards real applications as the TFTs in OLED displays are operated in the saturation region. Like in a long-channel transistor made of

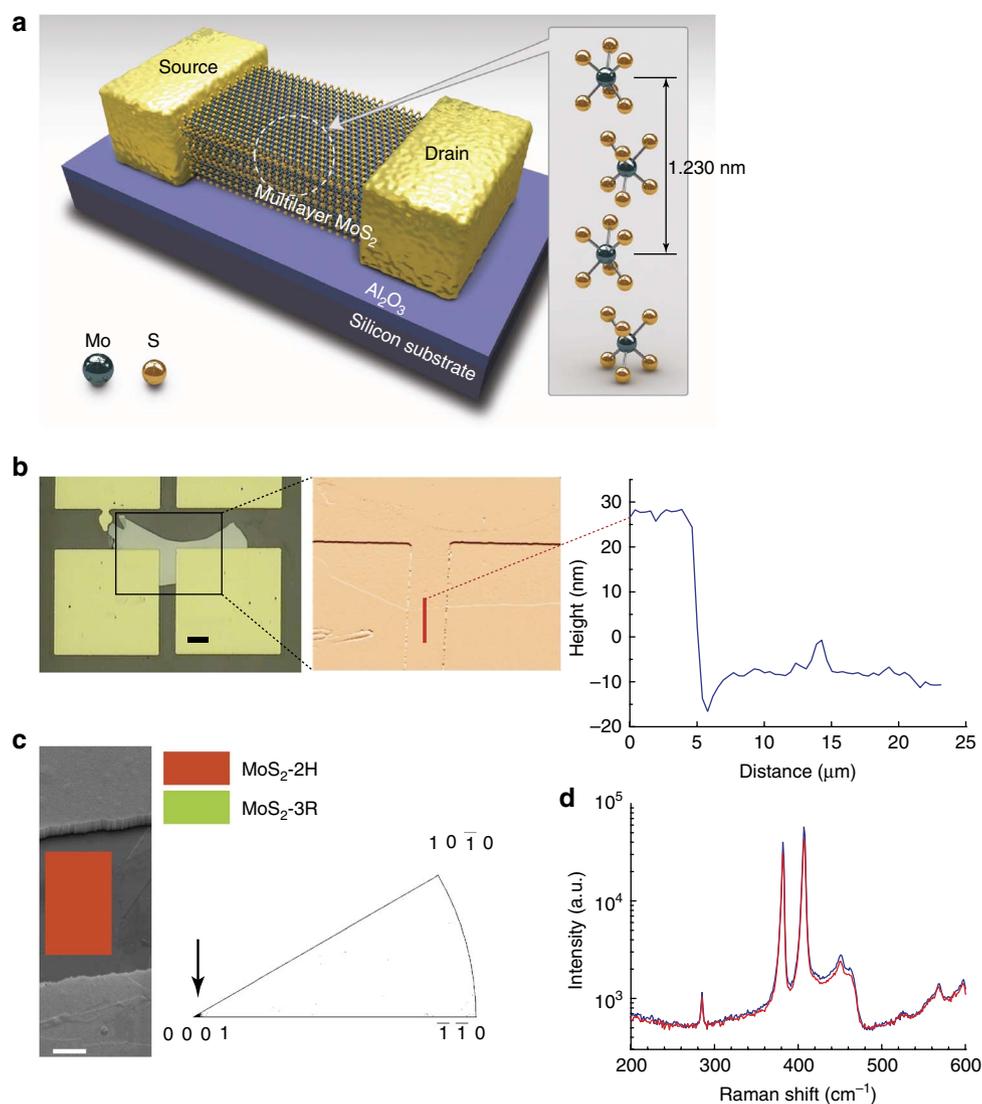


Figure 1 | MoS₂ TFT device and its structural properties. (a) Schematic perspective view of a MoS₂ TFT with a multilayer MoS₂ crystal. (b) Optical and AFM image of a device deposited on top of a silicon substrate with a 50-nm-thick Al₂O₃ layer. The scale bar is 20 μm. Also shown is a cross-sectional plot along the red line in AFM image. (c) Scanning electron microscope image of the MoS₂ channel with a crystal orientation mapping. The scale bar is 3 μm. Also displayed is a partial inverse pole figure indicating a <0001>-oriented single crystal. (d) Raman spectroscopy measurements on a bulk single crystal (blue) and a transistor channel (red).

a covalent semiconductor, the saturation of current occurs in the MoS₂ TFT owing to pinch-off of the conducting channel at the drain side as the gate-drain diode becomes reverse-biased at high V_{DS} . As graphene has zero bandgap, instead of pinch-off, the drain side of the conducting channel becomes p-type at high drain bias⁹, restricting current saturation and current modulation to a very small window, if at all. The bandgap of MoS₂ makes both current modulation and saturation robust, as borne out by Fig. 2b,c.

The saturation of current observed here is quantitatively understood based on a long-channel device model based on surface potential. Poisson equation is solved to determine the surface potential at the MoS₂/ALD oxide interface as a function of the gate and the drain bias voltages. Then, the Shockley model of transistor performance is used to calculate the current. The only unknown input parameters to the model are the carrier mobility, the doping density and the contact resistance. At high positive gate biases, the channel is flooded with accumulated carriers and is highly conductive, and the contact resistances limit the current. This helps us to deduce

the contact resistance to be $\sim 17\text{ k}\Omega$ as described in Supplementary Fig. S1 and in the Supplementary methods. This value is rather high, and reducing it by an order of magnitude is necessary for the future.

Thus, the mobility and the doping density remain as the unknown parameters. In Fig. 2d, using a mobility of $100\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and a doping density of $N_D \sim 10^{16}\text{ cm}^{-3}$, an excellent fit to the measured device characteristics is obtained. We assert that these values are not fortuitous, as borne out by complementary capacitance-voltage and field-effect mobility measurements, which are described next. The device model for TFTs provides insight into the performance of 2D layered semiconductor devices, and thus is a powerful tool to extract physical parameters of the material.

Accumulation and inversion channels. At large negative gate biases, the drain current recovers as seen in Fig. 2b, indicating the formation of an inversion channel (formation of a hole gas in a *n*-type semiconductor). However, the source/drain contacts are formed to

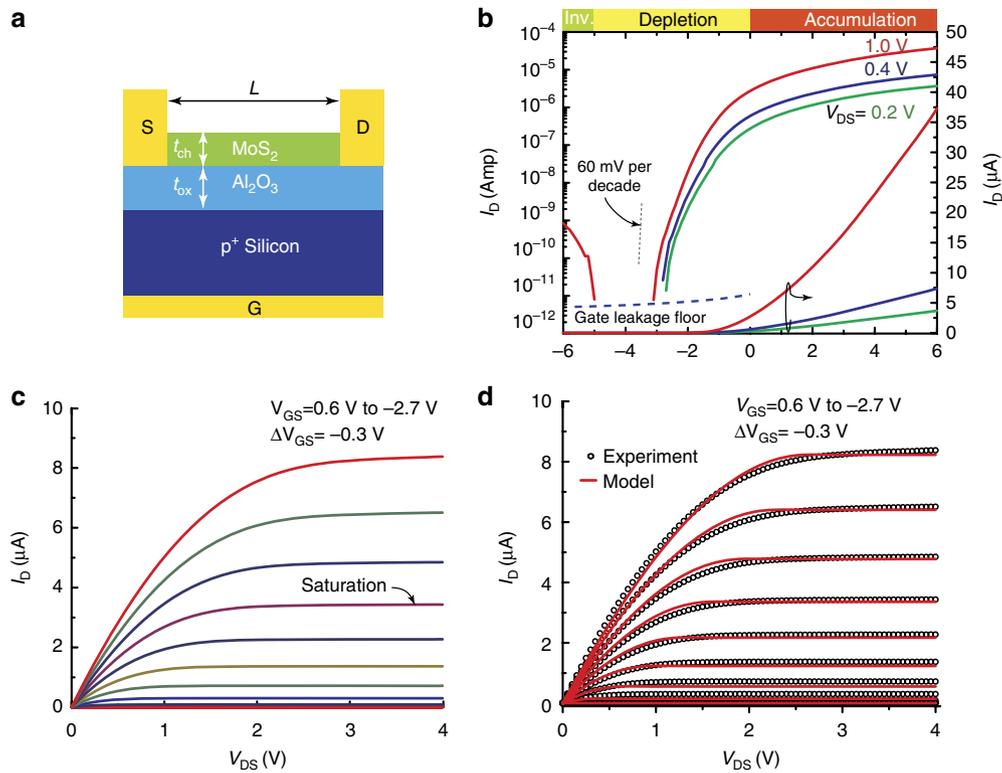


Figure 2 | Device geometry and electronic properties of MoS₂ TFTs. (a) The device geometry of a back-gated MoS₂ TFT. The TFT device was measured at $T = 300$ K. The device geometries are: $W/L = 4/7 \mu\text{m}$, $t_{\text{ox}} = 50$ nm and $t_{\text{ch}} = 30$ nm. (b) Drain current versus back gate bias showing -10^6 on/off ratio and -80 mV per decade subthreshold slope. (c) Drain current versus drain bias showing current saturation. (d) Same as (c), including a long-channel model (red lines) showing excellent agreement between the TFT model and measured device behaviour.

the conduction band, and therefore there exists a large barrier for conduction through a p-type inversion channel. To explore these features quantitatively, capacitance-voltage measurements were performed, and the measured device characteristics were compared with energy-band diagram-based models.

Figure 3a–c show the calculated energy band diagrams for the MoS₂ TFT structure for various gate bias conditions. For the calculation, we self-consistently solve Poisson and Schrödinger equations in the effective-mass approximation. The bandgap of SL MoS₂ occurs at the K -points in the hexagonal k -space lattice⁴, implying a valley degeneracy of $g_v = 2$, similar to graphene. On the other hand, the conduction band minimum of multilayer MoS₂ moves to a lower symmetry point in the k -space along the Γ - K line. This results in a higher valley degeneracy ($g_v = 6$ for the Γ - K line) than SL MoS₂, effectively tripling the density of states, implying higher carrier densities and higher currents in the ballistic limit¹⁴. The net drive current for a given voltage is a product of the carrier density and the velocity. Thus, in addition to high velocity, a high density of states (DOS) is equally attractive for attaining high speed. Driven by higher valley degeneracy, multilayer MoS₂ has the potential for considerably higher current drives than SL MoS₂ in the ultrascaled limit, and high charge densities have recently been reported¹⁵. Even in the long-channel structure, thin-film MoS₂ can take advantage of its multilayer nature. It can provide multiple conducting channels for boosting the current drive by using double gates, similar to silicon-on-insulator MOSFETs. The semiconducting material properties of multilayer MoS₂ such as the conduction and valence band offsets with Si and ALD Al₂O₃, the valley degeneracy, band-edge effective masses, dielectric constant and bandgap were used in the calculation. The values are provided in Supplementary Table S1 and Fig. S6. The model indicates that owing to the work-function

difference between MoS₂ and p^+ Si, the thin MoS₂ layer is initially depleted of mobile carriers. Upon application of positive bias on the Si gate, a 2D electron gas in the MoS₂ layers closest to the ALD Al₂O₃ forms. This accumulation channel conducts current between the source and the drain. Figure 3d shows the accumulation carrier density profile in more detail. Most of the carriers are electrostatically confined close to the MoS₂/ALD interface, similar to the case in a Si MOSFET. Thus, the ‘quantum capacitance’, which dictates the voltage drop in the semiconductor to sustain the conducting charge $C_S \sim \epsilon_S / \langle z \rangle$ is large as the centroid of the charge distribution $\langle z \rangle$ is ~ 1 – 2 nm from the interface.

Capacitance measurements. Figure 3e shows the measured two-terminal capacitance as a function of the voltage between an ohmic contact pad to the MoS₂ and the back gate. Several interesting features are evident from the measurement. As the pads are large as seen in Fig. 1b, they form a parasitic pad capacitance, which sets the floor of the measured value (~ 12 pF). When the MoS₂ layer is depleted of mobile carriers, the measured capacitance is this pad capacitance. As positive gate biases are applied, the formation of an electron accumulation layer in the MoS₂ results in an increase in the capacitance. The electron accumulation layer also electrically connects the two ohmic pads, effectively doubling the parasitic pad capacitance—this is exactly what is measured. In Supplementary Fig. S2 and the Supplementary methods, we describe this effect in more detail, and also include the capacitance-voltage measurements of a MoS₂ flake in contact with just one metal pad in Supplementary Fig. S3, which confirms the above analysis. The capacitance of the MoS₂ layer alone (C_{MoS_2}) is dependent on its doping density. The calculated values of C_{MoS_2} for three different doping densities are shown in Fig. 3e, from which it is concluded that the

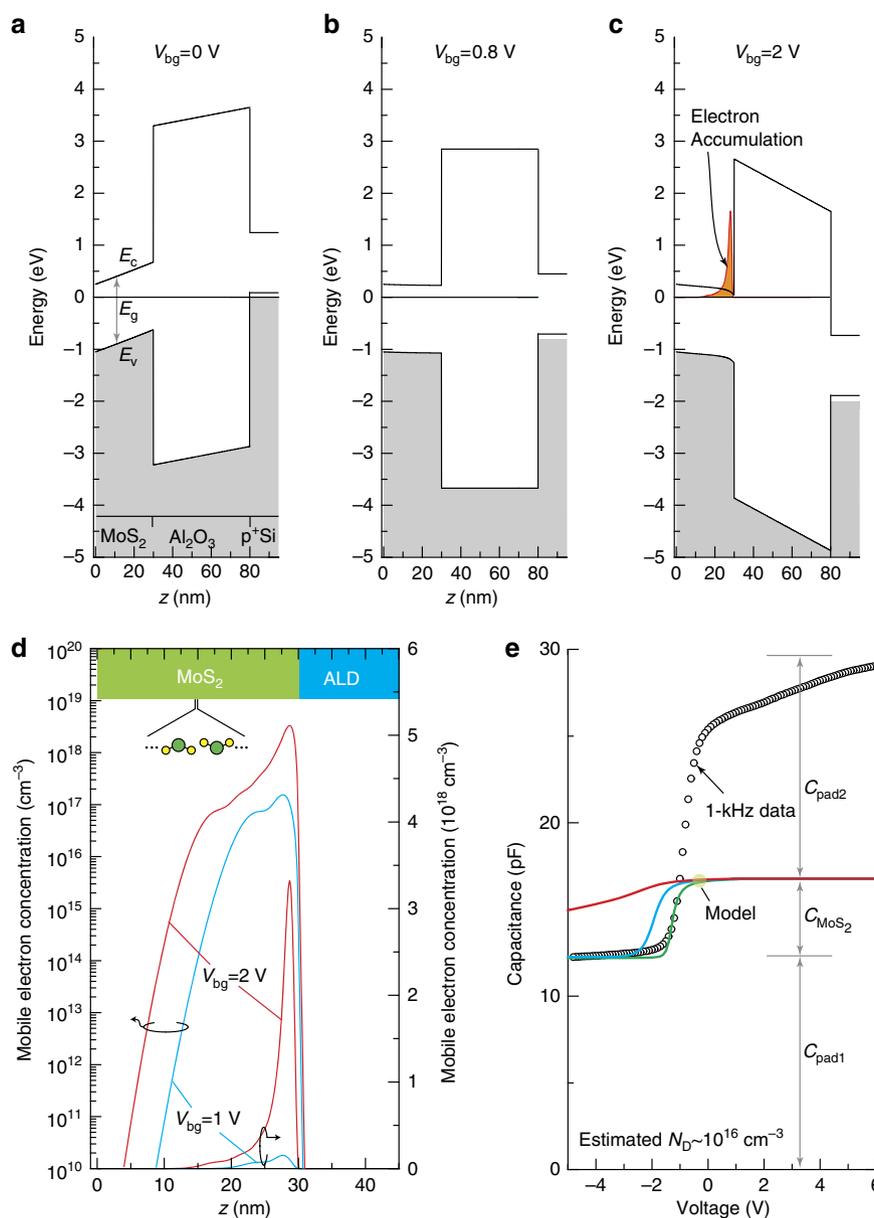


Figure 3 | Energy band diagrams, carrier distributions and measured capacitance-voltage profile of the MoS₂ TFT device. (a–c) Energy band diagrams of the MoS₂/Al₂O₃/p⁺Si device under various bias conditions. The band offsets and physical parameters relevant for the calculation are described in the Supplementary methods. The self-consistent Schrödinger-Poisson calculation shows that at large positive gate bias, a 2D electron gas is formed at the MoS₂/Al₂O₃ interface. (d) The 2D electron gas that forms the conductive channel is shown in an enlarged scale. Most conduction occurs by electrons accumulated in a few layers at the MoS₂/Al₂O₃ interface. With increasing bias, the centroid of the electron distribution shifts closer to the interface. This indicates that the ‘quantum’ capacitance in the semiconductor increases with positive gate bias. (e) Measured capacitance-voltage curves of the MoS₂/Al₂O₃/back-gate capacitors (circles). The solid lines show the calculated capacitance for three different doping densities (red: 10¹⁸, blue: 10¹⁷ and green: 10¹⁶ cm⁻³), not including parasitic pad capacitances. The slope indicates a doping density close to 10¹⁶ cm⁻³.

unintentional doping density in the measured MoS₂ layer is of the order of $N_D \sim 10^{16} \text{ cm}^{-3}$. We note that this is a low doping level, and can vary between naturally occurring samples not grown by controlled means. The extracted doping density has a direct impact on impurity scattering and carrier mobility, which is what was investigated next.

Charge transport and scattering. The field-effect mobility of MoS₂ TFTs was extracted from the I_D - V_{GS} curves of Fig. 2b, and the corresponding measurements for temperatures 77–300 K. The mobility values are extracted in the linear region at $V_{GS} = 2 \text{ V}$ or equivalently at a carrier density $n = C_{ox}(V_{GS} - V_T) \approx 1.6 \times 10^{12} \text{ cm}^{-2}$. The intrinsic

carrier mobility (mobility without the effect of the contact resistance R_c) was calculated using an equivalent circuit as shown in Fig. 4c and described further in Supplementary Fig. S5 and the Supplementary methods, and are shown as blank circles in Fig. 4a. Also shown are data reported from Fivaz and Mooser’s work³ from 1967. The values are very similar. We note here that Fivaz and Mooser used MoS₂ crystals grown by transport reaction as opposed to the naturally occurring MoS₂ used in this work, which bodes well for large-area growth for practical TFT applications. The decrease in mobility with temperature is a typical signature of diffusive band transport, as opposed to activated (hopping) transport. If there were significant Schottky barrier heights, the mobility would appear to

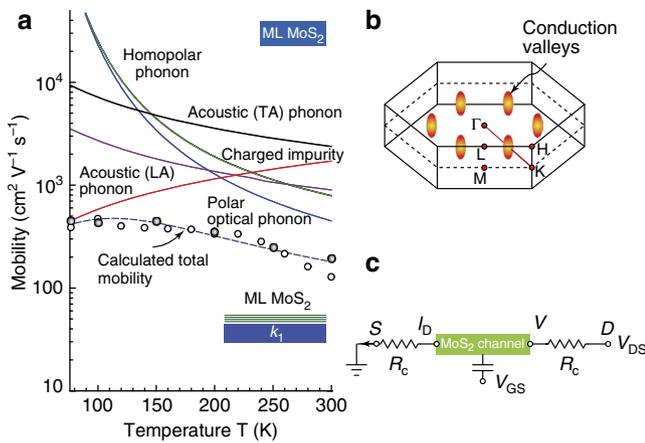


Figure 4 | Charge transport properties of the multilayer MoS₂ channel.

(a) Measured temperature-dependent field-effect mobility of MoS₂ TFTs. The open circles are data measured in this work, and the filled circles are data from ref. 3. From the theoretical transport model, the electron mobility (dashed line) is limited by impurity scattering (red line) at low temperatures. At room temperature, the mobility is limited by the combined effect of the homopolar (out-of-plane) phonon (green line) and the polar-optical phonon (blue) scattering. Details of these scattering mechanisms are described in the Supplementary methods. (b) The hexagonal Brillouin zone of multilayer MoS₂ with the high symmetry points and six equivalent conduction valleys. (c) An equivalent circuit model for the MoS₂ TFT including the effect of the contact resistance R_c .

increase with temperature. This can lead to erroneous conclusions on the nature of charge transport (that is, activated versus band transport). To avoid such confusion, samples that exhibited ohmic contacts over the entire temperature range were carefully chosen for mobility extraction.

To explain the temperature-dependent carrier mobility, the semiclassical Boltzmann transport equation under the relaxation time approximation is used. The model is described in detail in the Supplementary methods. A typical characteristic of layered structures (such as MoS₂) is that the carriers move independently in each layer. Neglecting the vanishing interlayer interaction, the energy dispersion of carriers becomes¹⁶ $E(k) = \hbar^2(k_x^2 + k_y^2)/2m^*$, where $\mathbf{k} = (k_x, k_y)$ is the 2D wave vector of carriers and m^* is the in-plane effective mass. The corresponding 2D density of states is $g_{2d} = g_v m^* / \pi \hbar^2$, where \hbar is the reduced Planck constant and g_v is the valley degeneracy. Recent experiments and models indicate the conduction band minima to be along the Γ -K line¹⁷ of the Brillouin zone, as indicated in Fig. 4b. The sixfold symmetry of this point leads to a valley degeneracy of $g_v = 6$. We have used this value for transport calculations, consistent with the energy band diagram and capacitance calculations of Fig. 3. Carrier scattering from (a) ionized impurities, (b) acoustic phonons, (c) in-plane polar optical phonons and (d) out-of-plane lattice vibrations (homopolar phonons) are taken into account to explain the transport measurements. A 2D ionized impurity scattering model is invoked where carriers scatter from a sheet of impurities located at the surface of the MoS₂ layers. Coupling of carrier with both longitudinal acoustic (LA) phonons and transverse acoustic (TA) phonons are taken into account under the deformation potential approximation. The energies of optical phonons in bulk MoS₂ are in the frequency range of 400–500 cm⁻¹ (50–60 meV)¹⁹ as also measured in Fig. 1d. Electron-polar optical phonon scattering is described by the Fröhlich interaction²⁰ with a static dielectric constant $\epsilon_0 = 7.6$ and optical dielectric constant²¹ $\epsilon_\infty = 7.0$ with phonon energy $\hbar\omega_{op} = 49$ meV for the E_{2g}^1 mode.

For homopolar phonon modes, the sulphur atoms of opposite planes vibrate out of phase (A_{1g} mode) and the corresponding phonon energy is^{19,22} $\hbar\omega_{hp} = 52$ meV.

The resultant mobility is calculated using Mathiessen's rule $\mu^{-1} = \mu_{imp}^{-1} + \mu_{LA}^{-1} + \mu_{TA}^{-1} + \mu_{op}^{-1} + \mu_{hp}^{-1}$. The calculated mobility associated with the individual scattering mechanisms as well as the resultant mobility is shown in Fig. 4a along with the measured data. At low temperatures, the mobility is limited by ionized impurity scattering. At room temperature, the mobility decreases by enhanced optical phonon and acoustic phonon scattering. A reasonably good match is found between calculated and experimentally measured mobility (at low temperatures) for a choice of impurity sheet density $n_{imp} \sim 1.8 \times 10^{10}$ cm⁻², which corresponds to a volume density of $\sim 3 \times 10^{15}$ cm⁻³. This value is comparable to the background doping density for unintentionally doped bulk MoS₂, and consistent with the value estimated from the capacitance-voltage measurements in Fig. 3e.

A large electron effective mass and the strong optical phonon (out-of-plane and polar phonon) scattering set an upper bound on the mobility in multilayer MoS₂. We note here that the accuracy of the calculation is subject to the uncertainty in the electron-phonon coupling coefficients and the bandstructure parameters used in the model. However, these parameters are not expected to be vastly different from those assumed. Higher mobilities could potentially be achieved by intercalation of MoS₂ layers (similar to recently demonstrated encapsulations of silicon carbide crystals in graphite enclosure²³). By sandwiching SL MoS₂ between two dielectric layers, the out-of-plane phonon vibrations can be suppressed. If the homopolar phonon mode is damped, ionized impurity scattering and in-plane polar optical phonon scattering determine the charge transport. Strain effects can also potentially be used to deform the bandstructure, leading to lowering of the electron effective mass and improvement in mobility. Electron mobility in MoS₂ can be further expected to improve as the growth and processing methods improve, leading to fewer impurities. Moreover, charged impurity scattering in these devices can be damped using high k dielectrics (dielectric engineering)^{24–26}. Effects such as remote phonon scattering could limit this improvement²⁷. As the current experimental values are far below limits expected of remote phonon scattering, there is ample room for improvement.

Discussion

The mobility measured for multilayer MoS₂ already exceeds most competing semiconductor materials for large-area TFTs by orders of magnitude. The values may be further improved by proper dielectric choices to near the intrinsic phonon limits. When combined with the large current modulation, the low subthreshold slope, and robust current saturation, multilayer MoS₂ makes a compelling case for TFT applications. All these properties are achieved in a back-gated structure, without the need for an additional dielectric layer on top, which is highly attractive for TFT implementation. The first demonstration of these attractive properties, combined with the comprehensive modelling of the behaviour, is expected to move multilayer MoS₂ towards real applications. The multilayer structure is easier to achieve over large areas by chemical vapour deposition or allied techniques, which are well suited for large-area applications. Looking beyond MoS₂, other transition metal dichalcogenides can offer competitive or complementary features. In addition to technological applications, conduction band electron states in these layered semiconductors have contributions from d orbitals, quite unlike traditional group-IV and III–V semiconductors and carbon nanomaterials, where chemical bonding is restricted to s and p orbitals. Thus, a rich range of physical phenomena that depend on d orbitals, such as magnetism, correlated-electron effects and superconductivity, can be expected in these materials. Such features can possibly be integrated with the

semiconducting properties demonstrated here seamlessly, as there are no out-of-plane bonds to be broken.

Methods

Device fabrication. An amorphous Al₂O₃ dielectric layer of ~50 nm in thickness was deposited on a highly doped p-type Si wafer (resistivity $5 \times 10^{-3} \Omega \text{ cm}$) by ALD process using trimethylaluminum (TMA, UP Chemical Co. Ltd., South Korea) and H₂O as a precursor and a reactant, respectively. The deposition temperature was maintained at 300 °C and the gas injection schedule for one cycle of deposition were 0.5/10/1.5/15 seconds for the TMA/N₂/H₂O/N₂ gases. Multilayer MoS₂ flakes were mechanically exfoliated from bulk MoS₂ crystals (SPI Supplies, USA) and transferred on the substrate. Electrical contacts (100 μm × 100 μm) were patterned on top of MoS₂ flakes using conventional lift-off technique. Ti (10 nm) and Au (300 nm) were deposited by electron-beam evaporation at room temperature. The device was then annealed at 200 °C in a vacuum tube furnace for 2 h (100 sccm Ar and 10 sccm H₂) to remove resist residue and to decrease contact resistance.

Measurements. The thickness of MoS₂ was measured using an AFM (Nanoscope III, Digital Instruments-Veeco, USA). The electron backscatter diffraction (JEOL JSM7000F, Japan) and Raman spectra (Renishaw RM-1000 inVia, UK) with a 514-nm Ar laser were measured to characterize the MoS₂ flakes on the substrate. Electrical characterizations were carried out with current-voltage measurements (Keithley, Semiconductor Characterization System 4200-SCS). During the low-temperature measurement of transport properties, temperature was controlled using a variable temperature cryogenic probe system (LakeShore, TTPX). Capacitance-voltage characteristics were measured with an HP 4284A Precision LCR Metre.

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Author contributions

S.K. and W.C. initiated the research and worked on device fabrication, current-voltage measurements and analysis of MoS₂ crystal properties. D.J. and A.K. performed device analysis and modelling, and calculations of scattering mechanisms. S.K., W.C., W.-S.H. and J.L. performed capacitance-voltage measurements. J.H.L., C.J., J.-B.Y. and J.-Y.C. worked on fabricating MoS₂ flakes and atomic force microscopy measurements. J.Y. and H.K. worked on ALD. Y.W.J., S.Y.L. and K.K. advised on planning and executing the research. D.J., A.K., W.C. and S.K. wrote the manuscript.

Additional information

Supplementary Information accompanies this paper at <http://www.nature.com/naturecommunications>

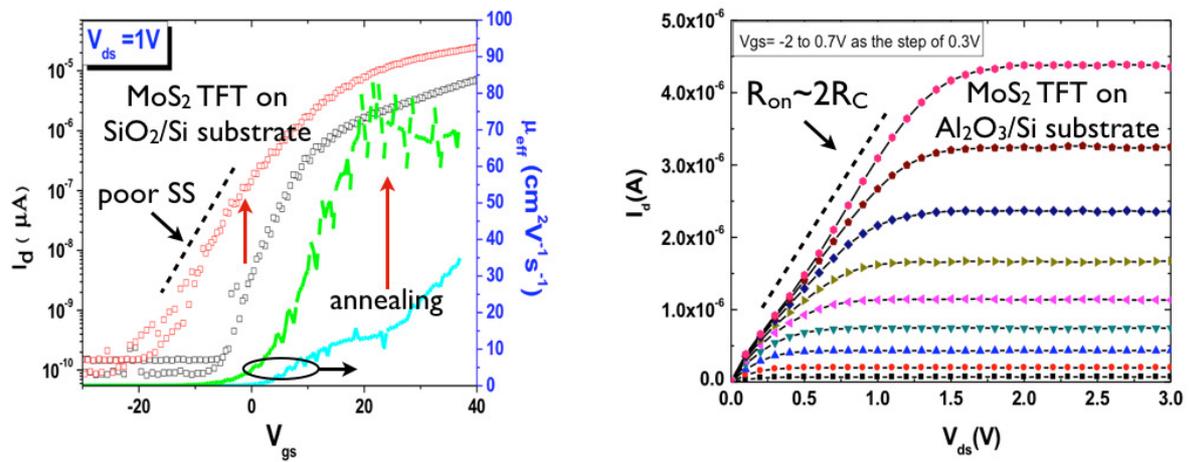
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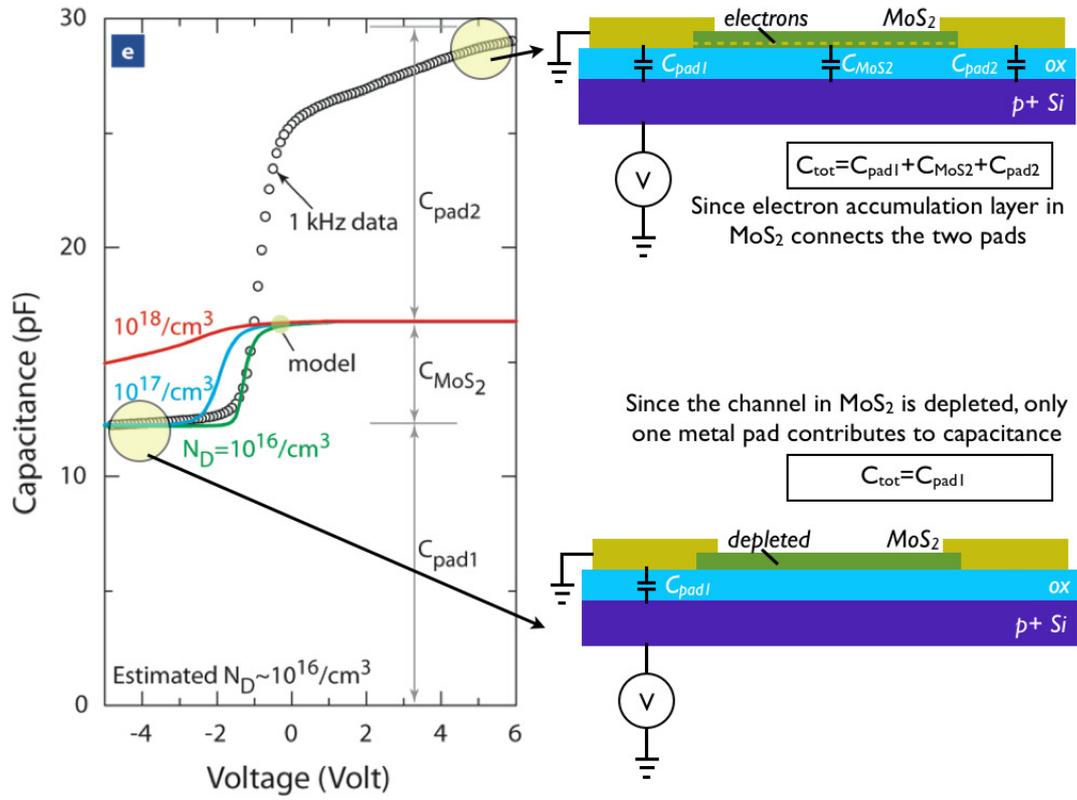
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Supplementary Information

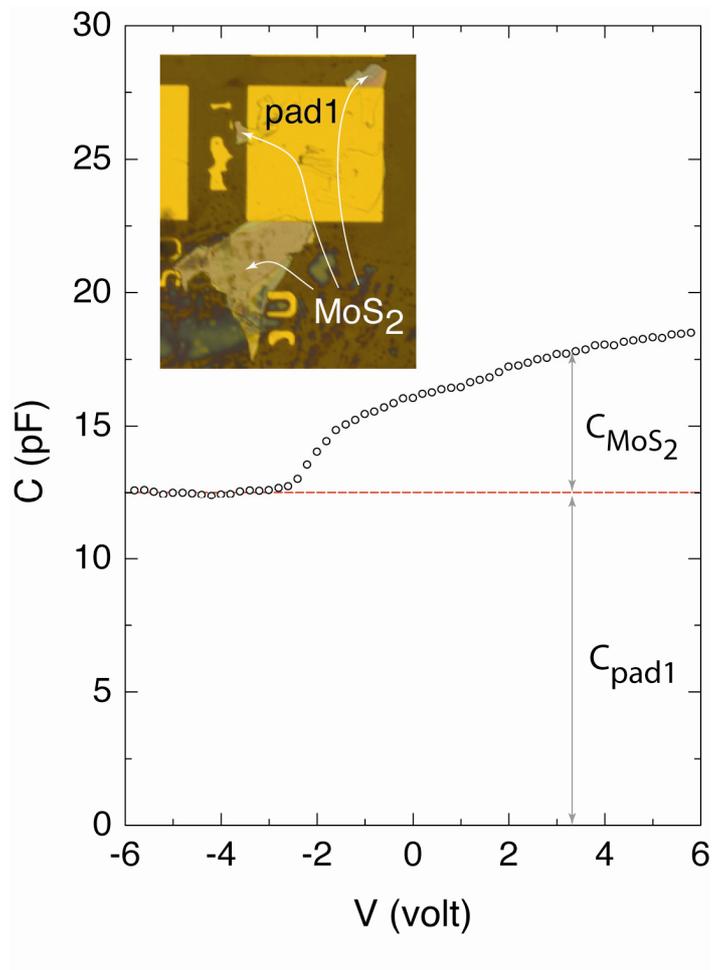
Supplementary Figures



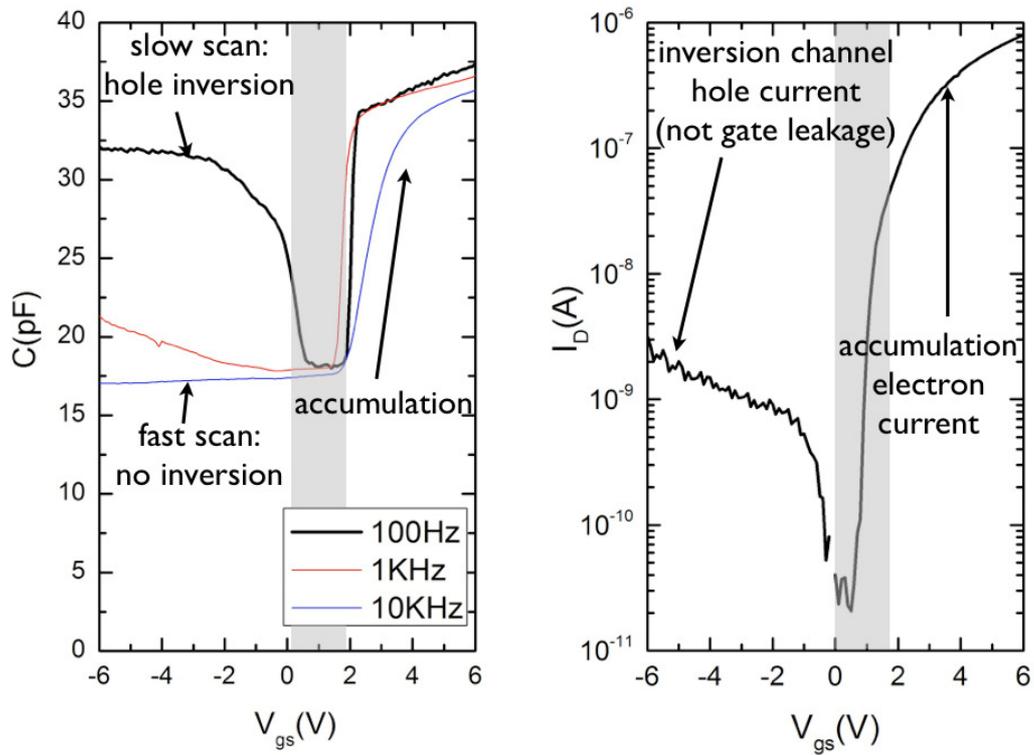
Supplementary Fig S1: Multilayer MoS₂ FETs on SiO₂/Si substrates, and contact resistance effects. (Left): Transfer curves and effective mobility of multilayer MoS₂ TFTs fabricated on SiO₂/Si substrates showing poor switching characteristics. The performance improves marginally upon annealing. (Right): Estimation of the contact resistance from the on-resistance of a multilayer MoS₂ TFT on ALD Al₂O₃/Si substrate.



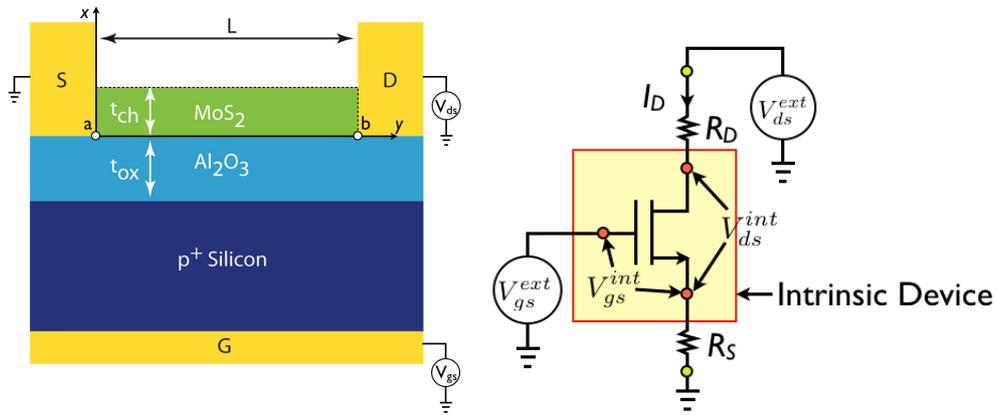
Supplementary Fig S2: Capacitance-voltage curves of MoS₂ TFT devices. The floor or ‘off-state’ capacitance corresponds to the pad capacitance of a single pad, whereas the on-state capacitance corresponds to that of the MoS₂ layer *and* two ohmic pads.



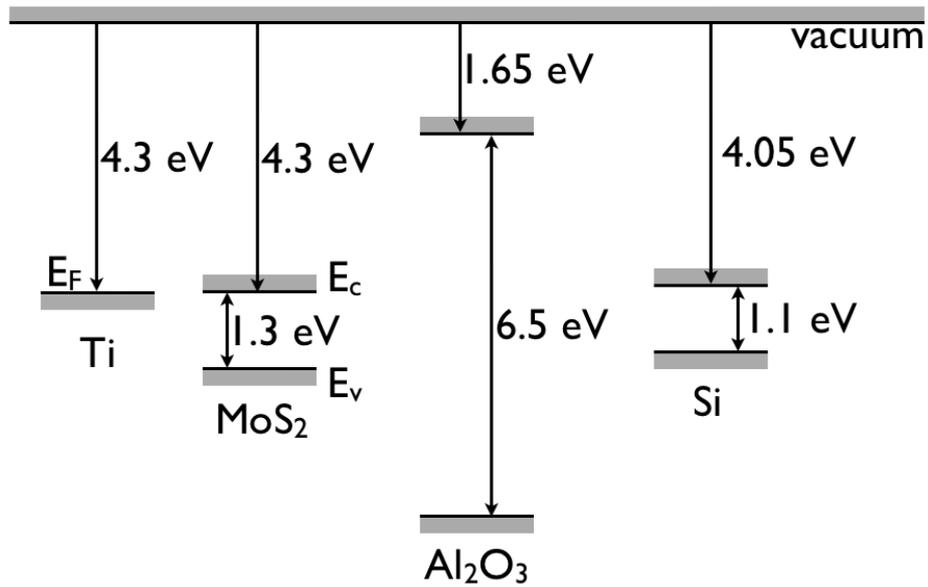
Supplementary Fig S3: Capacitance-voltage curves of a single MoS₂ flake connected to a metal pad. The floor or 'off-state' capacitance corresponds to the pad capacitance of a single pad, similar to Fig S2, whereas the on-state capacitance for this case corresponds to that of the MoS₂ flake. Note that it is necessary to locate a large flake for such a measurement to be successful.



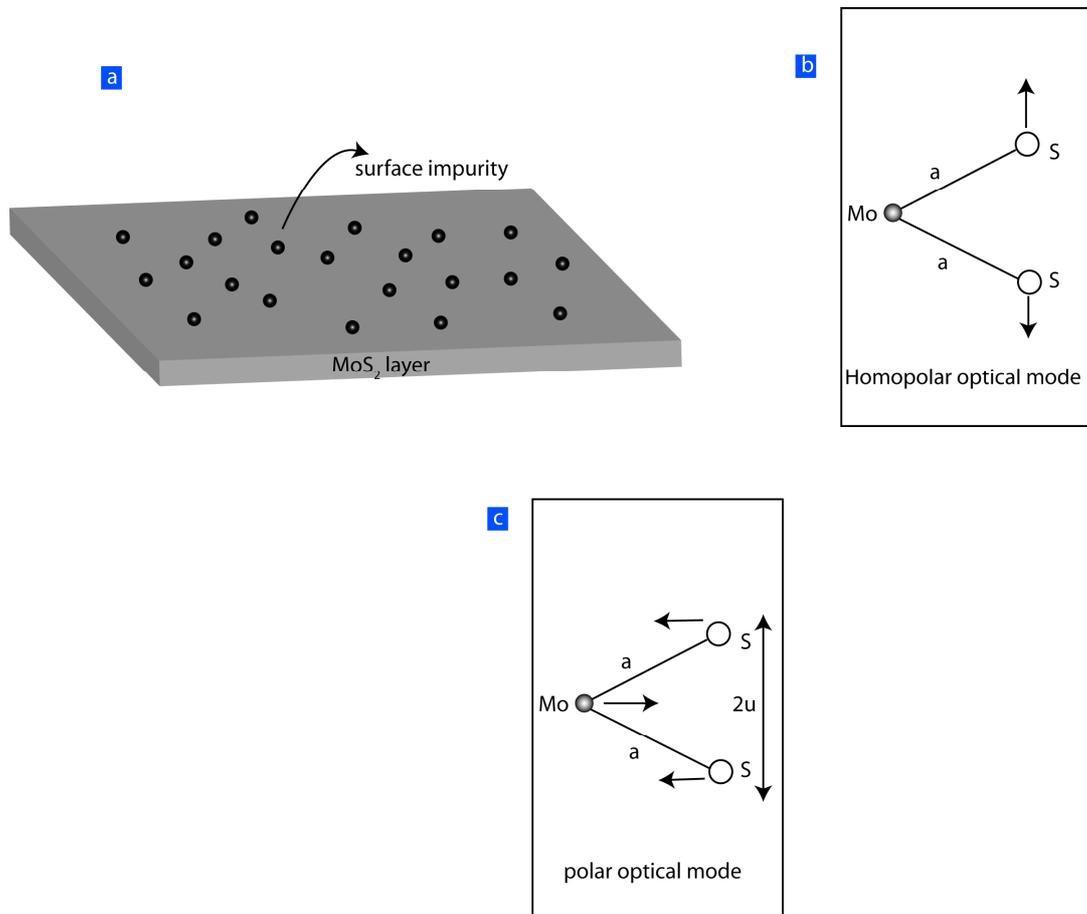
Supplementary Fig S4: Capacitance-voltage measurement of multilayer MoS₂ TFTs and corresponding drain currents. The low-frequency scans clearly indicate the formation of an inversion layer of holes. Since the ohmic contacts are formed to the electron channel, the slow RC charging from the Schottky barrier contacts to the hole gas results in the delay in hole channel formation. With the optimal contacts, inversion hole channels are expected to form with equal ease as the n-channel accumulation layers.



Supplementary Fig S5: Device geometry of the multilayer MoS₂ TFT and the circuit diagram showing the effect of extrinsic contact resistances on measured gate and drain voltages compared to the intrinsic transistor.



Supplementary Fig S6: Work function of Ti, and electron affinities and bandgaps of silicon, ALD Al₂O₃, and multilayer MoS₂ used for the energy band-diagram calculations. The band offsets can be directly inferred. The band alignment shows the feasibility of Ti for ohmic contact to the conduction band of MoS₂.



Supplementary Fig S7: Impurities and phonon modes in MoS_2 that affect charge transport. (a) Ionized impurities at the surface of a MoS_2 layer. Relative movements of molybdenum and sulphur atoms for (b) homopolar phonon mode, (c) polar optical phonon mode. Note that in homopolar modes, the sulfur atoms move out-of-plane in opposite directions.

Supplementary Methods

Device Characteristics and Modeling

a) Device Characteristics: The initial multilayer MoS₂ TFTs fabricated on 300nm SiO₂/Si substrates looked similar to earlier reports, exhibiting poor subthreshold characteristics as shown in Supplementary Fig S1. Annealing of these transistors improved the mobility and the current drive. Since the subthreshold slope is given by $SS = (1 + \frac{C_s + C_{it}}{C_{ox}}) \frac{kT}{q} \ln 10$, the oxide capacitance $C_{ox} = \epsilon_{ox} / t_{ox}$ is 20 times smaller for TFTs on SiO₂/Si compared to Al₂O₃/Si. This explains the high SS for the initial TFTs, compared to the near-ideal values for those on ALD high-*k* substrates, as discussed in the main text. The annealing strategy was used for all subsequent devices.

The contact resistance in traditional FETs is extracted from transmission-line method (TLM) measurements. However, due to the small area of the currently available multilayer MoS₂ flakes, such a measurement was not possible using optical lithography. Another dependable method for the extraction of the contact resistance is by measuring the on-resistance of the FET at a very large gate bias. The channel is highly conductive under this condition, and the current in the linear region flowing in the channel is limited by the source and drain contact resistances connected in series to the drain voltage source. The I_D - V_{DS} curves merge for various gate biases when this condition is achieved, since the gate capacitor cannot control the contact resistance. This feature is shown for a TFT in Supplementary Fig S1 (right), from where a $R_C \sim 17$ k Ω is extracted. The contact resistance varied between devices close to this value, and respective values were used for subsequent simulations. For applications of multilayer MoS₂ for TFTs, lowering of the contact resistance will lead to increase in drive currents.

b) Capacitance-Voltage measurements & Inversion channel formation: Supplementary Fig S2 is necessary to explain the measured C-V profiles under various bias conditions. The measured capacitance floor (~ 12 pF) corresponds accurately to the net capacitance of one ohmic metal pad with the back gate. However, when an accumulation layer of electrons is formed in the MoS₂ layer, it connects the two pads electrically. Since there is no current flow between them, the two pads and the MoS₂ accumulation layer are equipotential – they are all grounded. This explains the measured capacitance behavior. To further confirm this interpretation, we were able to locate a large MoS₂ flake that was in contact with just one metal pad: the measured C-V curve is shown in Supplementary Fig S3, and confirms our interpretation. Note that the pad capacitance floor is 12 pF in both Supplementary Figs S2 and S3. The net capacitance of the MoS₂ is now directly evident in Supplementary Fig S3. We note however, that this is a different (and much larger and of a different thickness) flake than those for which the FETs were measured. Therefore, a direct comparison of the model is not warranted.

In addition, some (not all) C-V measurements indicated a recovery of the capacitance at large negative voltages, indicating the formation of an inversion layer of holes in the MoS₂ layer. However, this requires efficient ohmic contacts to the valence band, which was not intended in the experiment. It is also indicated in Fig 2(b) in the TFT transfer curves. This preliminary observation is of immense interest given the possibility of complementary logic devices. We discuss this further to the extent we have been able to investigate it till now. As alluded to in the main text and in Fig 2(b) there, some devices showed the formation of an inversion channel of holes at large negative gate biases. This is expected of a semiconductor layer, as long as the contacts are able to electrically connect to the valence band of the semiconductor. Though the

contacts are designed for the conduction band electrons, the high contact resistance indicates that it is not yet ideal. Thus, one can expect a Schottky-barrier contact to be formed to the valence band. If so, it should be possible to observe conduction by inversion channels in the multilayer MoS₂ TFTs. A fingerprint of an inversion channel is through capacitance-voltage measurements that are complementary to the current-voltage measurements. For devices that show inversion channel current conduction, we performed capacitance-voltage scans, and indeed observed the recovery of the capacitance only when the scans were performed at a slow rate. The complementary C-V and I-V curves are shown in Supplementary Fig S4 for a device that did show the presence of an inversion channel.

As is evident in the figure, the capacitance at large negative bias voltages is able to recover under slow scan, but not under rapid scans. This is completely identical to what happens in a silicon MOS structure²⁸. Since the contact is electron-rich, and there is no direct source of holes, they have to form by thermal interband excitations or by the minute leakage currents into the contacts. This is a slow process, requiring ~ms to ~second time scales, depending on the size of the bandgap and the nature of the contacts. It is foreseen that with proper choice of metal workfunctions, this preliminary observation will seed the realization of complementary n-FET and p-FET based multilayer MoS₂ TFTs, with significant technological impact.

c) Modeling of device characteristics: The electrical characteristics of the back-gated FET structure are modeled using a long-channel model. The device geometry is shown in Supplementary Figure S5. The transistor model uses the fact that under flat-band conditions, the carrier density at all points (x, y) in the MoS₂ channel is equal to the unintentional doping, i.e., $n_{FB}(x, y) = N_D$. When the potential in the channel is changes due to gate and drain voltages, the electron density changes to $n(x, y) = N_D \exp[\beta V(x, y)]$, where $V(x, y) = \psi(x) - V_{ch}(y)$ is the long-channel approximation and $\beta = q/kT$ is the inverse of the thermal voltage. The Poisson equation in the channel is given by $\partial^2 \psi / \partial x^2 \approx -(qN_D / \epsilon_s)[1 - \exp[\beta(\psi - V_{ch})]]$ in the gradual channel approximation. This equation has no analytic solutions, but for bias conditions for which the device is “on”, the exponential term dominates, and the equation can be integrated to yield the solutions for the potential ψ as a function of the drain-induced potential V_{ch} . The solution is $\psi = V_{GF} + (2/\beta) \cdot W[\exp[\beta(V_{GF} + V_{ch})/2] \times C_D / C_{ox}]$, where $V_{GF} = V_G - V_{FB}$, $C_D = \epsilon_s / L_D \sqrt{2}$ is the accumulation or ‘Debye’ capacitance with $L_D = \sqrt{\epsilon kT / q^2 N_D}$ as the Debye length in MoS₂, and $W(\dots)$ is the Lambert-W function, the solution of the equation $W(u) \cdot \exp[W(u)] = u$. Since the source and the drain points labeled ‘a’ and ‘b’ in Supplementary Fig S5 have $V_{ch} = 0$ and $V_{ch} = V_{ds}$ respectively, the values ψ_a and ψ_b are obtained as a function of the gate and the drain bias voltages. The drain current is then obtained by integrating the transport equation in the long channel approximation. Doing so, one obtains²⁹

$$I_D = \frac{W}{L} \mu_{eff} C_{ox} [(V_G + \frac{2}{\beta})(\psi_b - \psi_a) - \frac{1}{2}(\psi_b^2 - \psi_a^2)] + \frac{W}{L} \frac{q}{\beta} \mu_{eff} n_{tch} (1 - \exp[-\beta V_{ds}]), \quad (S1)$$

where n_i is the intrinsic carrier concentration in MoS₂ due to thermal interband excitation, and μ_{eff} is the effective (x -averaged) electron mobility. We have used this formalism to model the current-voltage curves as shown in Figure 2 of the main text. However, the measured gate and drain voltages are not those of the intrinsic device, but are higher due to potential drops at the source and drain contact resistances, as shown in Supplementary Fig S4. The extrinsic voltages are given by $V_{gs}^{ext} = V_{gs}^{int} + I_D R_S$ and $V_{ds}^{ext} = V_{ds}^{int} + I_D (R_S + R_D)$. We use $R_S = R_D = R_C$, the contact resistance for the evaluation. The value of R_C is easily obtained at a high gate bias, since under that condition the channel resistance is negligible, and the net resistance is $V_{ds} / I_D = 2R_C$. We measure $R_C \sim 20 \text{ k}\Omega$ for the device modeled. The values are expected to reduce with further process development. The fit to the experimental data in Fig 2(d) of the main text requires an effective mobility of $100 \text{ cm}^2/\text{V}\cdot\text{s}$. The fitting can be considered to be an effective extraction of the mobility, which is complemented by calculation of the mobility due to various scattering mechanisms as described later in this supplementary section.

d) Energy band diagram simulation details: The energy band diagrams to explain the device characteristics were calculated by solving Poisson equation and Schrödinger equation self-consistently. The Schrödinger equation is solved in the effective mass approximation using a freely available tool³⁰ by incorporating material properties specific to the device. The energy band offsets and energy bandgaps used in the calculation for silicon, ALD Al₂O₃, and multilayer MoS₂ are shown in Supplementary Fig S6. The values for MoS₂ were taken from Refs^{31, 32}. The required material parameters for the simulations are shown in Supplementary Table ST1.

Modeling of Charge Transport

Since the MoS₂ TFTs studied here are long channel ($L \sim 10 \mu\text{m}$) devices, carrier transport phenomena are best explained in the drift-diffusion scheme. The electrical response is linear and the change in the carrier distribution function and the resulting conductivity depends linearly on the electric field³³. In such a scenario, the temperature-dependent carrier mobility is given by

$$\mu(T) = \frac{e}{m^*} \left[\frac{\int \tau(\varepsilon) \varepsilon e^{-\varepsilon/k_B T} d\varepsilon}{(k_B T)^2} \right] \quad (\text{S2})$$

where $\tau(\varepsilon)$ is the energy-dependent momentum relaxation time, k_B is the Boltzmann constant, and e is the charge of an electron. Note that in ensemble averaging of momentum relaxation time, we use the Boltzmann distribution function instead of the Fermi-Dirac distribution. The Fermi energy of electrons in each MoS₂ layer is given by

$$\varepsilon_F = k_B T \ln \left(e^{\frac{\pi \hbar^2 n}{8 s_v m^* k_B T}} - 1 \right), \quad (\text{S3})$$

where n is the 2D electron density and $g_v=6$ is the valley degeneracy. Due to the high electron effective mass $m^* \sim m_0$ where m_0 is the bare electron mass, and the high valley degeneracy, MoS₂ behaves as a non-degenerate semiconductor. For example, for a carrier density $n=5 \times 10^{13}/\text{cm}^2$, the Fermi energy lies 4 meV ($\ll k_B T = 25$ meV @ 300K) above the conduction band edge at room temperature.

Scattering mechanisms considered to model the experimental data are: i) ionized impurity scattering, ii) acoustic phonon scattering, and ii) optical phonon scattering. For ionized impurity scattering, the impurities are assumed to be at the two surfaces of each MoS₂ layer (similar to the ionized impurity scattering in graphene³⁴) as shown in Supplementary Fig. S7(a). The energy-dependent momentum relaxation time is calculated using Fermi's Golden rule.

For screening by free carriers, a finite-temperature Thomas-Fermi screening model is used.

The finite-temperature Thomas-Fermi wave vector is given by

$$q_{TF}(T) = \frac{2g_v}{a_B^*} \left(1 - e^{-\frac{\pi \hbar^2 n}{g_v m^* k_B T}} \right), \quad (\text{S4})$$

where a_B^* is the bulk Bohr radius in MoS₂.

Acoustic phonons are low energy excitations of coherent lattice vibrations with energy dispersion of $E(q) = \hbar v_\lambda q$, where v_λ is the phonon velocity (sound velocity) of phonon mode λ , and q is the wave vector of phonons. As a result, the electron-acoustic phonon scattering can be considered as an elastic scattering mechanism. Under deformation potential approximation, the acoustic phonon limited mobility can be written as

$$\mu_{ac}(T) = \frac{e\hbar^3 \sigma_s v_\lambda^2}{(m^*)^2 \Xi_\lambda^2 k_B T}, \quad (\text{S5})$$

where $\sigma_s = 6.4 \times 10^{-6} \text{ kg/m}^2$ is the areal mass density of multilayer MoS₂, and Ξ_λ is the acoustic deformation potential. In the calculation of electron-acoustic phonon scattering, a nondegenerate ($E(q) \ll k_B T$) phonon spectrum is assumed. The justification lies on the fact that the characteristic Bloch Grüneisen (BG) temperature $T_{BG} = \sqrt{\frac{4\pi n}{3}} \left(\frac{v_\lambda}{k_B} \right)$ above which the phonon spectrum is nondegenerate, is low even at high carrier densities. For example, for $n = 10^{13} / \text{cm}^3$, the BG temperature of multilayer MoS₂ is $T_{BG} \approx 32 \text{ K}$. The reason for the low BG temperature is the high valley degeneracy in multilayer MoS₂ film. Using this impurity density and fitting the measured carrier mobility over the temperature range, we extract acoustic deformation potentials $\Xi_{LA} \approx 2.6 \text{ eV}$ for LA phonons and $\Xi_{TA} \approx 1 \text{ eV}$ for TA phonons respectively. Though the extraction of deformation potentials from a single transport measurement involves a certain level of uncertainty, nevertheless these values are similar to the deformation potentials values of single layer MoS₂ predicted recently³⁵ using density functional calculations. This is justified since the in-plane transport properties of multilayer MoS₂ should resemble that of a single layer due to the weak van der Waals interaction between adjacent layers. Future atomistic simulations and transport experiments are expected to reveal the more accurate values of these parameters of multilayer MoS₂ and determine the relative importance of different scattering mechanisms at room temperature.

For optical phonon scattering, two types of optical phonons are considered: a) polar optical phonon mode, and b) homopolar optical phonon mode. In polar optical phonon mode, the two sulfur atoms in a MoS₂ unit cell move in the same direction whereas the metal atom moves in the opposite direction as shown in Supplementary Fig S7(c). This mode has an energy

$\hbar\omega_{\text{op}}=0.049$ eV at the Γ point of the Brillouin zone³⁶. The high polar optical phonon energy inhibits emission and only phonon absorption occurs in electron-optical phonon scattering events at low electric fields (in the mobility-regime). For electron-polar optical phonon scattering, we use the results of Gelmont and Shur³⁷ originally developed for 2D electron gas transport in GaN high-electron mobility transistors.

For the homopolar optical phonon mode, the two sulfur atoms move in opposite directions as shown in Supplementary Fig. S6(b). The net dipole moment associated with this mode vanishes due to the inversion symmetry about the metal plane resulting a non-polar optical phonon mode. The homopolar phonon limited mobility in MoS₂ is given by³⁸

$$\mu_{\text{hp}}(T) = \frac{e}{8\pi m^* \omega_{\text{hp}} g^2} \frac{\left(e^{\frac{\hbar\omega_{\text{hp}}}{k_B T}} - 1 \right)}{1 + \frac{\hbar\omega_{\text{hp}}}{2k_B T}}, \quad (\text{S6})$$

where g ($\sim \varepsilon_d^2$, ε_d is the deformation potential) is a dimensionless coupling constant and $\hbar\omega_{\text{hp}}$ is the homopolar optical phonon energy. The value of g is extracted by fitting the transport data with the theory. A reasonable fit in Fig. 4(a) of the main text is found for $g=0.08$. This leads to a deformation potential $\varepsilon_d \approx 3$ eV, comparable to the previously reported³⁸ value of 6 eV. The above transport theory is based on the assumption that the applied electric field is small. The small electric field is implicitly defined by the relation $v_d \ll v_{\text{th}}$, where $v_d = e\tau E/m^*$ (E = applied electric field) is the drift velocity of carriers due to applied electric field and v_{th} is the mean thermal velocity. For a Maxwellian velocity distribution of carriers in 2D $f(v) = (m^*/2\pi k_B T) \exp[-m^* v^2 / (2k_B T)]$, and the mean thermal velocity is $v_{\text{th}} = (\pi k_B T / 2m^*)^{1/2}$. This leads to a critical electric field $E_{\text{cr}} = (1/e\tau)(\pi m^* k_B T / 2)^{1/2}$, below which the low-field theory is valid. For mobility $\mu \sim 100$ cm²/V·s ($\tau \sim 5 \times 10^{-15}$ s), the critical field is $E_{\text{cr}} \approx 10^5$ V/cm. As the

mobility values were extracted from the linear (ohmic) region of the I_D - V_{ds} curve (see Fig. 2(d)), the applied electric field is $E=(V_{ds} - 2I_D R_c)/L$ in contrast to the saturation region. For $I_D \sim 5 \mu\text{A}$, $V_{ds} \sim 1\text{V}$ and $L=4 \mu\text{m}$, the typical applied field is $E \sim 10^3 \text{ V/cm}$, which is orders of magnitude lower than the critical field E_{cr} . This justifies the linear response modeling.

Supplementary Tables

Material	Bandgap (eV)	Dielectric constant	Conduction band degeneracy	Electron effective mass	Heavy Hole eff. mass	Dopant act. ener. (meV)	Intrinsic Conc. n_i (cm ⁻³)
MoS ₂	1.3	4.3	6	1.0	1.0	6	1.6×10^8
Si	1.12	11.9	6	0.33	0.49	10	1.0×10^{10}
Al ₂ O ₃	6.5	7.0					

Supplementary Table S1: Material properties of silicon, ALD Al₂O₃, and multilayer MoS₂ used for the energy band-diagram calculations. Note that the anisotropic properties of MoS₂ are included through requisite averaging.

Supplementary References

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