Polarization-Induced GaN-on-Insulator E/D Mode p-Channel Heterostructure FETs

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***Abstract*— Polarization-induced *p*-type doping is realized in molecular beam epitaxy (MBE) grown ultrathin body GaN/AlN heterostructures. The novel heterostructure consisting of a thin strained GaN layer grown on an AlN template exhibits a hole gas density close to the interface polarization charge (~5 x 10^{13} /cm^2). Both enhancement- and depletion-mode (E/D) p-channel heterostructure field effect transistor (HFETs) are demonstrated. Driven by the high hole density, a 2.4-μm-long D-mode HFET with alloyed ohmic contacts shows improvement of drain current from 150 mA/mm ($V_{GS} = 12$ V, $V_{DS} = 30$ V) at 300 K to 270 mA/mm ($V_{GS} = 15$ V, $V_{DS} = 30$ V) at 77 K. The extrinsic peak transconductance of the D-mode device increases from 11 mS/mm ($V_{GS} = 6$ V, $V_{DS} = 30$ V) at 300 K to 16 mS/mm ($V_{GS} = 4$ V, $V_{DS} = 30$ V) at 77 K. Both the drive current and transconductance are recorded in nitride p-channel FETs. MBE regrown heavily Mg-doped p$^+$-GaN is then employed for ohmic contacts of E-mode p-channel HFETs. A 2-μm-long E-mode device with a drain current of 4 mA/mm ($V_{GS} = 10$ V, $V_{DS} = 80$ V) and ON/OFF current ratio of 10^3 is achieved.**

***Index Terms*— AlN, enhancement and depletion (E/D) mode, GaN, molecular beam epitaxy (MBE), p-channel, polarization, transistor.**

I. INTRODUCTION

FEW reports exist for wide-bandgap III-nitride-based p-channel field effect transistors (pFETs) [1], [2]. The current performance of III–V pFETs vastly lags behind that of n-channel High Electron Mobility Transistors (HEMTs) Finding methods to boost the performance of pFETs will greatly extend the applications of nitride-based electronics by enabling complementary logic devices. Polarization-induced doping [3] overcomes limitations imposed by the large thermal activation energy for holes [4], and has the potential to enable high-density mobile hole channels. Conducting hole layers were reported in GaN/AlGaN heterostructures [5], [6]. Through polarization field ionization, the effect of impurity scattering can be suppressed, and 2-D hole gases with high mobility are expected. Another possible way to boost the hole mobility is to utilize the crossover of heavy and light hole bands either by strain or in high Al composition AlGaN [7]. To maximize the polarization-induced hole concentration and to employ high Al composition AlGaN channels, AlN is the natural choice as the barrier because of its largest band gap and spontaneous polarization charge in III-nitrides. For metal polar p-channel (In, Al)GaN/AlN heterostructures, AlN acts as the back barrier, providing excellent electrical insulation and simultaneously excellent thermal conductivity. It also enables incorporation of epitaxially strained channel layers, which is expected to play an increasing important role in III-nitride devices of the future, just as it does in silicon devices today.

We recently reported the first realization of ultrathin GaN-on-insulator quantum well (QW) n-channel FETs consisting of strained GaN channels sandwiched in strain-free AlN barriers [8]. In this letter we demonstrate the *p*-type counterpart *on the same platform* by simply removing the top AlN barrier and introducing Mg acceptors. The GaN/AlN heterojunction exhibits high mobile hole carrier density, and the resulting p-channel heterostructure FETs (HFETs) show record drive current and transconductance. In addition, enhancement-mode (E-mode) operation is also demonstrated with regrown p$^+$-GaN ohmic contacts.

II. EXPERIMENTS

The nitride heterostructures are grown on ~1-μm-thick semi-insulating metal-polar AlN templates on sapphire by molecular beam epitaxy (MBE) in a Veeco Gen 930 system. A 200-nm-thick unintentionally doped (UID) AlN buffer is epitaxially grown, followed by a ~1/1 nm UID GaN and a ~4/7.5 nm Mg-doped (~4 × 10^{18} cm^{-3}) *p*-type GaN layer for the enhancement- and depletion-mode (E/D) devices. The as-grown surface exhibits a smooth morphology, with ~0.6-nm rms roughness for 10 × 10 μm^2 regions.

In D-mode devices, Ni/Au (10/5 nm) stacks are deposited and annealed at 500 °C for 10 min in O_2 ambient for ohmic contacts. Ni/Au (40/110 nm) layers are deposited directly on the *p*-type GaN channel without annealing for the Schottky gate metal stacks.

For E-mode devices, we employ a MBE regrowth process for ohmic contacts. A ~200-nm-thick SiO_2 mask is deposited, and the nitride regrowth regions are etched for ~40 nm. Regrowth of ~90-nm-thick heavily Mg-doped (~3 × 10^{19} cm^{-3}) p$^+$-GaN is performed in the MBE system. Then, Ni/Au (10/5 nm) stacks are deposited and annealed at 500 °C for 10 min in O_2 ambient for ohmic contacts, followed by 10-nm Al_2O_3 using atomic layer deposition (ALD) as gate dielectric. Ti/Au (40/110 nm) layers are deposited as the gate metal stacks.

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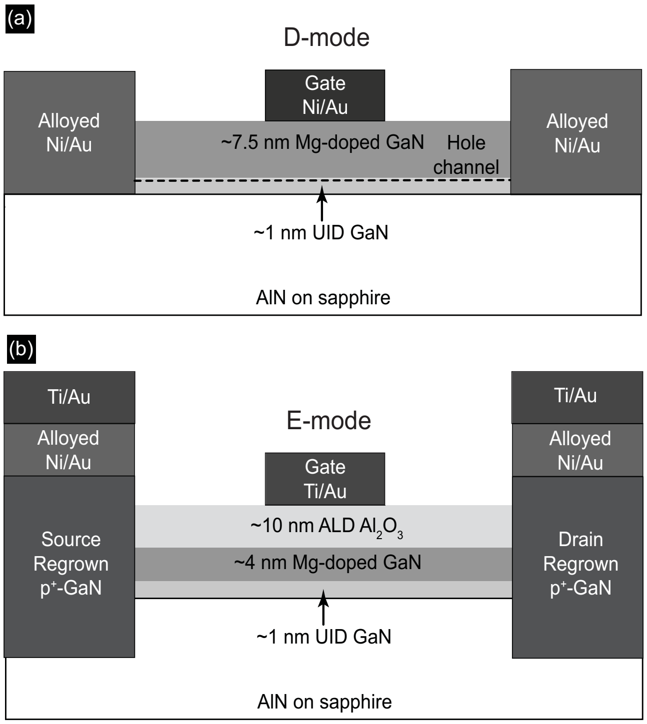

Fig. 1. Schematic view of device structures for (a) D-mode and (b) E-mode p-channel heterostructure FETs (not to scale).

III. Results and Discussion

The schematic device structure is shown in Fig. 1. At the pseudomorphic GaN/AlN heterojunction a negative bound polarization charge creates band banding, and field-ionized mobile holes accumulate at the heterojunction to form a conducting p-type channel. The Mg-acceptor dopant atoms assist to compensate deep level traps and keep the Fermi level close to the valence band [3]. Details of the origin of the hole gas formation will be discussed in a separate paper. The E-mode heterostructure is highly resistive in Hall-effect measurement. For D-mode heterostructures, the post-process measured 300/77 K Hall-effect hole concentration is $\sim$5.7/4.9 $\times$ 10^{13} /cm^2, with hole mobility of $\sim$6.6/13 cm^2/Vs and sheet resistance of $\sim$1.7/0.96 $\times$ $10^4 \Omega/\square$. We observe that the mobile holes resist freeze out at low temperature, with an improved mobility, which are signatures of polarization-induced doping. Though the UID GaN is intended to reduce the effect of impurity scattering, the hole mobility is still moderate. The measured hole gas density is the highest reported in *any* semiconductor heterostructure, and is a direct consequence of the giant polarization charge. Further improvement in control of the hole gas density could be achieved using (Al, In)GaN/AlN heterostructures: 1) tuning the channel composition (AlGaN, InGaN, etc.) to control the polarization charge; 2) doping the AlN with donors to compensate the 2DHG; and 3) employing work function engineering to control the surface barrier height and the Fermi level.

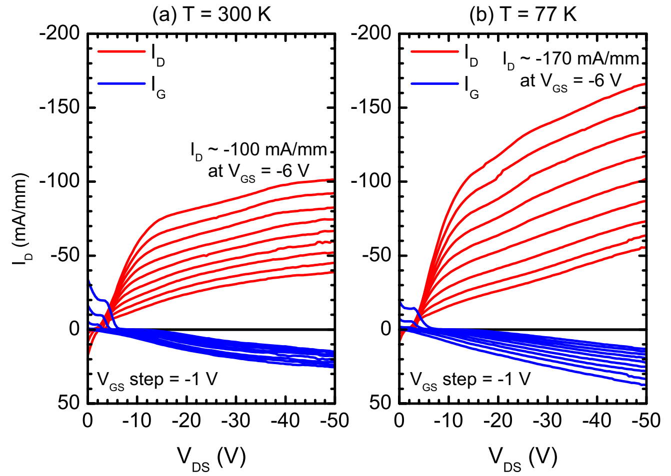

Fig. 2. (a) 300- and (b) 77-K output characteristics of a D-mode p-channel FET with $L_g = 2.4$ μm, showing improved current drive at low temperature.

The device dimensions of the fabricated D-mode pFETs are $W_g/L_g = 49/2.4$ μm and $L_{gs}/L_{sd} = 0.8/5.3$ μm. The output characteristics of the D-mode pFET are shown in Fig. 2(a) and (b). Because of surface depletion of the ultrathin p-type GaN layer and nonoptimal annealing conditions, the intended ohmic contacts show Schottky-like behavior and turn on around $V_{DS} = -3$ V. With the drain biased up to -50 V, the 300/77 K drain current reaches $-100/-170$ mA/mm at $V_{GS} = -6$ V. The drain current *increases* at low temperature. Because of the high density of hole carriers and gate leakage, the device is not completely pinched off at $V_{GS} = +2$ V. With incorporation of high-κ gate dielectric and advanced device structures that have better electrostatic control over the channel like FinFETs [9], the pinch-off characteristics can be improved. In spite of these issues, the measured drive currents are the highest in GaN pFETs, and are a direct consequence of the high density of the polarization-induced hole gas.

The device dimensions of the fabricated E-mode pFETs are $W_g/L_g = 49/2$ μm and $L_{gs}/L_{sd} = 1/6$ μm. The output characteristics of the E-mode pFET at 300 K are shown in Fig. 3(a). Though regrowth of thick heavily Mg-doped p-type GaN in the source and drain regions is employed, the source-gate and gate-drain access regions are highly resistive as there is no 2DHG channel. This leads to space-charge-limited injection of carriers from the contacts, an issue that can be remediated in self-aligned structures, or by selective recess. A high turn-on voltage around $V_{DS} = -10$ V is observed, with very characteristic space charge transport behavior [10]. With $V_{DS} = -80$ V, the drain current reaches -4 mA/mm at $V_{GS} = -10$ V. A threshold voltage of -2.5 V is extracted, which is the gate bias intercept of the linear extrapolation of drain current from the point of peak transconductance in the linear plot of transfer characteristics at $V_{DS} = -80$ V (not shown).

In Fig. 3(b) the transfer characteristics of the E/D mode p-channel devices are plotted. With the incorporation of an ALD Al_2O_3 gate dielectric, the E-mode device shows an ON/OFF current ratio exceeding three orders of magnitude. High-resistance access regions, however, severely limit the current drive. On the other hand, with the maximum hole gas in the D-Mode device a current density >100 mA/mm is measured. The ideal device will need E-Mode behavior under the gate, but D-mode like access regions to combine high

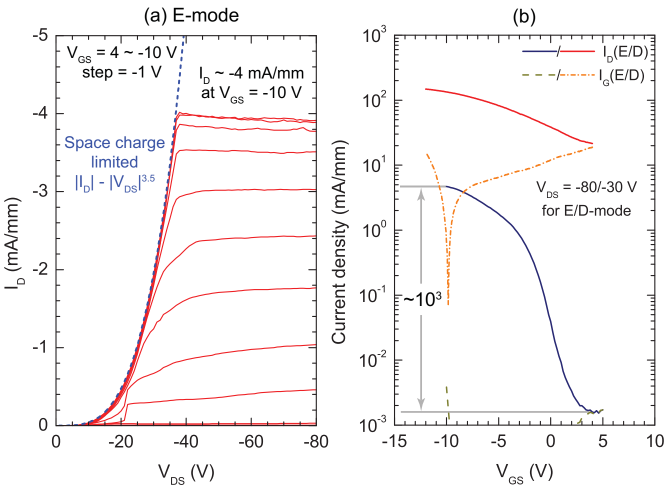

Fig. 3. (a) Output characteristics of an E-mode p-channel FET with $L_g = 2\ \mu$m at room temperature. (b) Semi-log plot of transfer characteristics and gate current for E/D-mode p-channel FETs at room temperature.

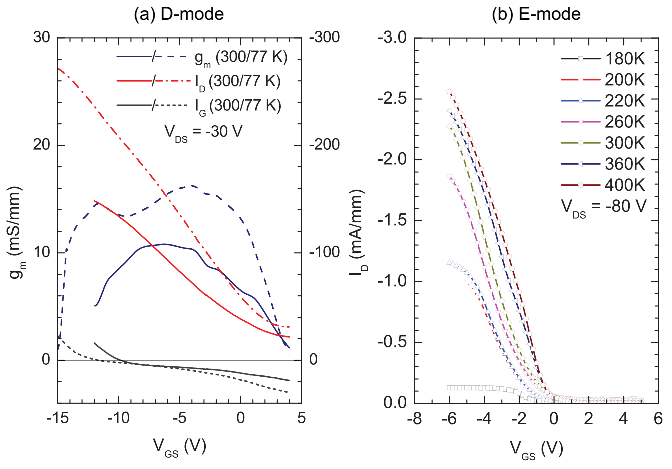

Fig. 4. (a) 300/77 K transfer characteristics for a D-mode pFET with $L_g = 2.4\ \mu$m. (b) Transfer characteristics for an E-mode pFET with of $L_g = 2\ \mu$m on temperature ranging from 180 K to 400 K.

on-currents, high ON/OFF ratios, and normally-off behavior. Our results show that the components of such a device are achievable on the GaN-on-insulator platform, but the ideal device combination remains a challenge for the future.

Fig. 4(a) shows the 300/77 K transfer characteristics of the 2.4-μm-long D-mode pFET device with $V_{\mathrm{DS}} = -30$ V. At 300 K, I_{D} is modulated from ~ -200 mA/mm to ~ -150 mA/mm when V_{GS} is swept from +4 V to −12 V; while at 77 K I_{D} is modulated from ~ -30 mA/mm to ~ -270 mA/mm with V_{GS} swept from +4 V to −15 V. The device is capable of modulating drive currents of ∼120/240 mA/mm at 300/77 K. The peak extrinsic transconductance g_m increases from ∼11 mS/mm around $V_{GS} = -6$ V to ∼16 mS/mm around $V_{GS} = -4$ V with the decrease of temperature from 300 K to 77 K. The corresponding gate currents are also shown to highlight the gate leakage issue. The lower bound of 300/77 K field effect hole mobility is extracted as ∼ 2.8/6.3 cm^2/Vs, using ideal long-channel FET model without considering the effects of Schottky contacts.

Fig. 4(b) shows the temperature-dependent transfer characteristics for a 2 μm-long E-mode device ($W_{\mathrm{g}}/L_{\mathrm{g}} = 49/2\ \mu$m; $L_{\mathrm{gs}}/L_{\mathrm{sd}} = 1/6\ \mu$m). As the regrown p$^+$ contacts are thick and bulk-like, the holes freeze out at low temperature and the drive current is decreased. At high temperatures, holes are thermally ionized and the contacts improve, boosting the current.

IV. CONCLUSION

This letter reported the first polarization-induced ultrathin body strained GaN/AlN p-channel HFETs. Both E/D-mode operations were achieved. In spite of the contact and gate leakage issue, the highest drive current in III-nitrides reported here prove the successful realization of polarization-induced hole channel pFETs with the highest hole gas density ever measured in semiconductor heterostructures. The measured performance provided a glimpse into what is possible in III-nitride pFETs. If the contact and gate issues were solved, the performance stands to benefit tremendously by lateral scaling. By introducing InGaN or AlGaN channels, strain can be used to deform the valence band structure to improve the hole mobility in the future. Combined with n-channel GaN QW FETs on AlN, the p-channel HEFTs thus presented a compelling case for III-nitride complementary logic and high-power applications.

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