Quaternary Barrier InAlGaN HEMTs With $f_T/f_{\max}$ of 230/300 GHz

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***Abstract*—Depletion-mode quaternary barrier $In_{0.13}Al_{0.83}Ga_{0.04}N$ high-electron-mobility transistors (HEMTs) with regrown ohmic contacts and T-gates on a SiC substrate have been fabricated. Devices with 40-nm-long footprints show a maximum output current density of 1.8 A/mm, an extrinsic dc transconductance of 770 mS/mm, and cutoff frequencies $f_T/f_{\max}$ of 230/300 GHz at the same bias, which give a record-high value of $\sqrt{f_T \cdot f_{\max}} = 263$ GHz among all reported InAl(Ga)N barrier HEMTs. The device speed shows good scalability with gate length despite the onset of short-channel effects due to the lack of a back barrier. An effective electron velocity of 1.36×10^7 cm/s, which is comparable with that in the state-of-the-art deeply scaled AlN/GaN HEMTs, has been extracted from the gate-length dependence of f_T for gate lengths from 100 to 40 nm.**

***Index Terms*—Cutoff frequency, electron velocity, high-electron-mobility transistor (HEMT), HFET, mobility, quaternary, regrown ohmic contact, T-gate.**

I. Introduction

LATTICE-matched $In_{0.17}Al_{0.83}N$ barrier high-electron-mobility transistors (HEMTs) have been extensively studied as an alternative to AlGaN/GaN HEMTs for RF and millimeter-wave power applications. A 370-GHz current-gain cutoff frequency f_T has been recently demonstrated using rectangular cross-sectional gates as a means of revealing scalability with minimum total gate capacitance [1]. For practical device and circuit applications, particularly for power amplifications in the field of wireless communication, highly conductive T-gates are desired to achieve high power-gain cutoff frequency $f_{\max}$ as in AlGaN HEMTs [2] and N-polar GaN/InAlN HEMTs [3]. However, such a structure introduces additional gate parasitic capacitance, resulting in a decrease in f_T. One needs to balance the gate resistance and parasitic capacitance by optimizing the T-gate profile to achieve a high f_T and $f_{\max}$ simultaneously. To date, the best performing device with balanced $f_T/f_{\max}$ in InAlN HEMTs is 205/220 GHz, achieved with a 30-nm-long gate footprint L_g [4]. Quaternary barrier InAlGaN/GaN HEMTs with electron mobility up to 1900 $cm^2/V \cdot s$ [5]–[7], which is higher than the typical mobility of ∼1300 $cm^2/V \cdot s$ in ternary InAlN HEMTs [8], have been explored to obtain better speed performance. High-speed devices based on these structures have been demonstrated, achieving f_T up to 220 GHz with alloyed contacts (contact resistance $R_c = 0.36\ \Omega \cdot$ mm) and L_g of 66 nm [6], [7]. f_T's approaching 300 GHz were achieved by adopting regrown contacts ($R_c = 0.12\ \Omega \cdot$ mm) with L_g less than 30 nm [9]. These results suggest that InAlGaN barrier HEMTs may offer good scalability in terms of high-frequency operation; however, high-performance T-gate device results on this structure have not yet been reported.

In this letter, we report the performance of the state-of-the-art $In_{0.13}Al_{0.83}Ga_{0.04}N$/GaN HEMTs with regrown ohmics and T-gates and study the device scaling behavior with gate length. Depletion-mode (D-mode) HEMTs on a SiC substrate with 40-nm-long gate footprints and 12-nm-thick top barriers (corresponding to a gate-length-to-barrier-thickness aspect ratio $L_g/t_{\rm bar}$ of 3.2) showed record-high $f_T/f_{\max}$ of 230/300 GHz in the InAl(Ga)N/GaN HEMT material system.

II. Experiments

The quaternary HEMT structure consists of an 11-nm $In_{0.13}Al_{0.83}Ga_{0.04}N$ barrier, a 1-nm AlN spacer, a 55-nm unintentionally doped GaN channel, a 1.8-μm semi-insulating GaN buffer, and a 100-nm AlN nucleation layer on a SiC substrate grown by metal–organic chemical vapor deposition.

The device fabrication with regrown ohmic contacts follows a similar process flow to that described in [10], with a Ti/Au (20/100 nm) metal stack deposited on a 140-nm-thick Si-doped n-GaN, regrown by molecular beam epitaxy (MBE). The transmission-line method yielded a total metal-to-channel contact resistance of 0.27 $\Omega \cdot$ mm, of which 0.20 $\Omega \cdot$ mm is attributable to the metal/GaN interface because of a low Si doping level. T-gates were fabricated by electron-beam lithography (EBL) using a ZEP/PMGI/ZEP resist stack, followed by Ni/Au (20/400 nm) evaporation and liftoff, without surface passivation. On as-processed van der Pauw test structures, Hall effect measurements revealed a sheet resistance of 195 Ω/sq with $n_s = 1.8 \times 10^{13}$ cm^{-2} and $\mu = 1770$ $cm^2/V \cdot s$. The devices have a source–drain distance L_{sd} of 0.8 μm, a gate width of 2×25 μm, a T-gate stem height of ∼100 nm, nominal footprint lengths ranging from 40 to 100 nm, and a head size of

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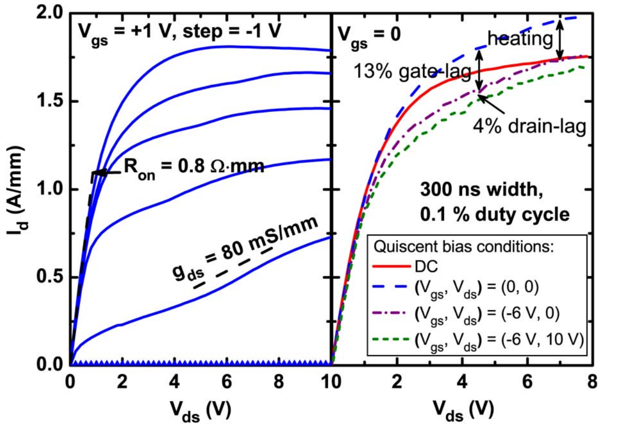

Fig. 1. (a) Common-source I–V's for a 40-nm-long InAlGaN HEMT measured from $V_{gs} = +1$ to -6 V in steps of -1 V. (b) Pulsed I–V measurements at $V_{gs} = 0$, with a 300-ns pulsewidth and 0.5-ms period.

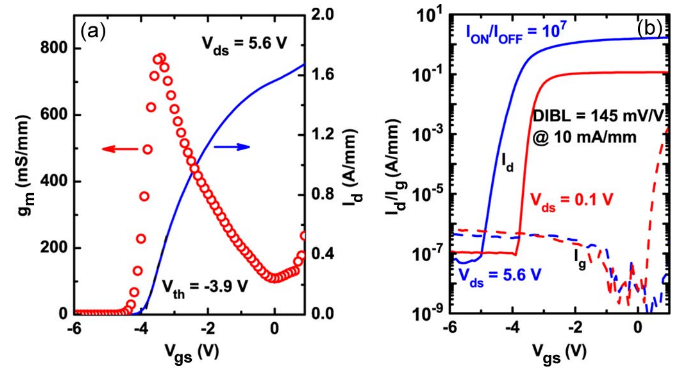

Fig. 2. Transfer characteristics of a 40-nm-long HEMT in both (a) linear scale and (b) logarithmic scale measured at $V_{ds} = 5.6$ and 0.1 V.

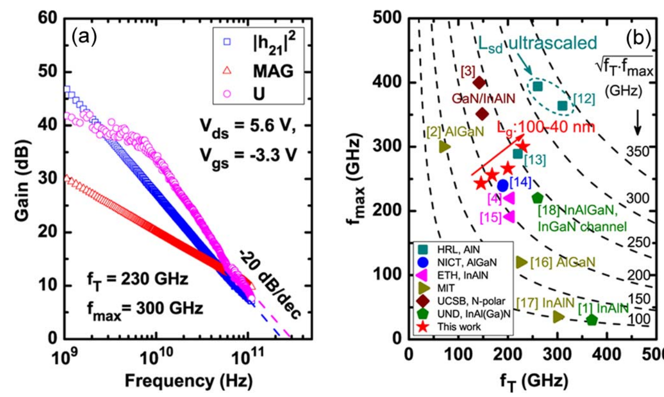

Fig. 3. (a) Small-signal RF performance of a 40-nm-long HEMT showing $f_T/f_{\max} = 230/300$ GHz. (b) Comparison of the measured f_T and $f_{\max}$ in this letter with the state-of-the-art D-mode GaN-based HEMTs from literature.

350–400 nm. The gate lengths were carefully estimated based on EBL dose test results on pieces from the same wafer with a consistent uncertainty less than ± 3 nm for all gate lengths.

III. Results and Discussion

Fig. 1(a) presents the common-source I–V's for a 40-nm-long InAlGaN HEMT. The gate–source bias V_{gs} was stepped from $+1$ to -6 V, and the gate–drain bias V_{ds} was swept from 0 to 10 V. At $V_{gs} = 1$ V, a maximum output current density $I_{d,\max}$ of 1.8 A/mm is reached, and the on-resistance R_{on} is calculated to be 0.8 $\Omega \cdot$ mm in the linear region. The dc output conductance g_{ds} is approximately 80 mS/mm at $V_{gs} = -3$ V and V_{ds} ranging from 5 to 8 V (near the peak f_T bias condition), implying moderate short-channel effects. The three-terminal OFF-state breakdown voltage was measured to be 14 V at $V_{gs} = -6$ V using the criterion of $I_d = 1$ mA/mm. Pulsed I–V measurements were performed in air on one of the 2×25 μm gate fingers using a 300-ns pulsewidth and a 0.5-ms pulse period from the following quiescent bias points: $(V_{gs}, V_{ds}) = (0, 0)$ as the cold pulse, $(-6$ V, 0), and $(-6$ V, 10 V). As shown in Fig. 1(b), the cold pulsed I–V did not exhibit saturation due to short-channel effects, and the higher current density than dc implies the presence of self-heating effects; gate lag and drain lag of 13% and 4%, respectively, were moderate and lower than that has been observed in similar unpassivated devices fabricated with alloyed contacts.

The 40-nm-long device transfer characteristics are plotted in both linear and logarithmic scales in Fig. 2. At $V_{ds} = 5.6$ V, a peak extrinsic dc transconductance $g_{m,\text{ext}}$ of 770 mS/mm and a threshold voltage V_{th} of -3.9 V (from linear extrapolation of I_d) are obtained. The transistors maintain a high output current on/off ratio of 10^7, and the drain-induced barrier lowering (DIBL) is calculated to be 145 mV/V at $I_d = 10$ mA/mm between $V_{ds} = 5.6$ and 0.1 V.

Small-signal RF measurements were taken from 100 MHz to 110 GHz with an Agilent N5250C vector network analyzer calibrated using Line-Reflect-Reflect-Match off-wafer impedance standards. Measured S-parameters were deembedded using on-wafer open and short structures to subtract pad parasitic capacitance and inductance. The deembedded current gain $|h_{21}|^2$, unilateral power-gain U, and maximum available power gain MAG are plotted in Fig. 3(a) as a function of frequency at the peak f_T bias condition of $V_{ds} = 5.6$ V and $V_{gs} = -3.3$ V. The extrapolation of $|h_{21}|^2$ and U at a -20-dB/dec slope gives $f_T/f_{\max}$ of 230/300 GHz, corresponding to $\sqrt{f_T \cdot f_{\max}} = 263$ GHz. The values before deembedding were 133/260 GHz. Since the equivalent circuit modeling showed HEMT capacitance $(C_{gs} + C_{gd})$ of $\sim$22 fF and pad capacitance C_{pgs} (C_{pds}) of $\sim$12 fF, the f_T increase after deembedding is reasonable. Fig. 3(b) compares the measured f_T and $f_{\max}$ in this letter with the state-of-the-art D-mode GaN-based HEMTs, suggesting that these results favorably compare among devices with an unscaled L_{sd} ($>$ 300 nm), achieving balanced f_T and $f_{\max}$.

Fig. 4 shows the device gate-length scaling behavior. DIBL of 75 mV/V, g_{ds} of 46 mS/mm, and V_{th} of -3.6 V are extracted for the 100-nm-long devices. With L_g scaled down to 40 nm, both DIBL and g_{ds} increase, and V_{th} becomes more negative, implying enhanced short-channel effects. The gate-length dependence of $f_T/f_{\max}$ in Fig. 4(b) shows an increase from 146/243 GHz with $L_g = 100$ nm to 230/300 GHz with $L_g = 40$ nm, suggesting good device scalability. A linear fit to the slope of the total delay time $\tau = 1/(2\pi \times f_T)$ as a function of L_g yields an effective electron velocity v_e of 1.36×10^7 cm/s, with an extrinsic parasitic delay time τ_{ext} of 0.35 ps from the intercept. For comparison, the measured delay time for InAlGaN HEMTs with rectangular gates is also presented in Fig. 4(c): $v_e = 1.33 \times 10^7$ cm/s and $\tau_{\text{ext}} = 0.20$ ps [11]. Since the HEMTs with T-gates and rectangular gates were fabricated on wafers with similar transport properties, the similar

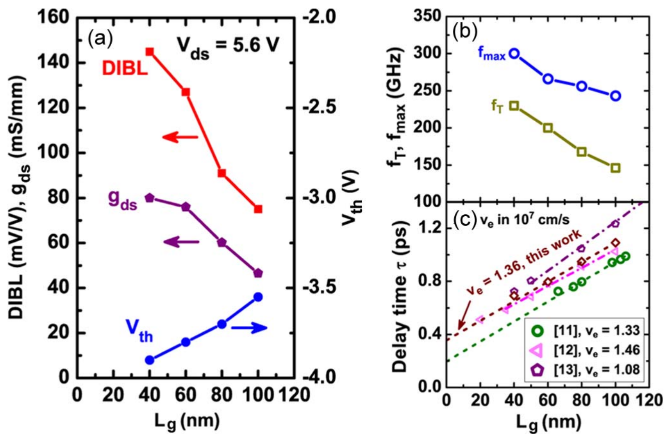

Fig. 4. DC and RF device performance scaled with the gate length ranging from 100 to 40 nm. (a) DIBL, g_{ds}, and $V_{\rm th}$. (b) $f_T/f_{\max}$. (c) Total delay time τ. The shortest gate lengths were excluded in the extraction of v_e from the linear fitting in (c) for this letter and [11]–[13].

extracted velocities are expected. It should be noted that these velocities are comparable to the effective velocity reported in the state-of-the-art deeply scaled AlN/GaN HEMTs ($v_e = 1.46 \times 10^7$ cm/s with $L_{sd} < 200$ nm) [12] and much higher than unscaled AlN/GaN HEMTs ($v_e = 1.08 \times 10^7$ cm/s with $L_{sd} = 1000$ nm) [13]. This is attributed to the high-electron mobility of $\sim$1800 cm^2/V $\cdot$ s in this letter and the reduction in gate-length extension [11], in contrast with a mobility value of 1200 cm^2/V $\cdot$ s in [12] and [13]. The larger extrinsic parasitic delay time in T-gate InAlGaN HEMTs compared with rectangular-gate devices is mainly associated with the additional parasitic gate capacitance arising from the mushroom head of the gate. Such a delay time component can be reduced by improving the T-gate aspect ratio, e.g., by increasing the stem height to be $>$ 200 nm [3], and by improving $g_{m,\rm int}$, e.g., by gate recessing. Furthermore, incorporation of regrown contacts with a lower R_c [1], [12] and use of shorter gate lengths in conjunction with back barriers (provided this is done without compromising the channel mobility) promise $f_T/f_{\max}$ near 350 GHz.

IV. Conclusion

D-mode $\rm In_{0.13}Al_{0.83}Ga_{0.04}N$/GaN HEMTs with MBE regrown ohmic contacts and T-gates have been fabricated. The 40-nm-long-gate device showed record-high $f_T/f_{\max}$ of 230/300 GHz and $\sqrt{f_T \cdot f_{\max}} = 263$ GHz in the InAl(Ga)N barrier HEMT family. A high effective electron velocity of 1.36×10^7 cm/s is believed to benefit from the excellent transport properties obtained in quaternary barrier InAlGaN HEMT structures.

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