Novel Logic Devices based on 2D Crystal Semiconductors: Opportunities and Challenges

(Invited Paper)

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Abstract

Two-dimensional crystal semiconductors such as graphene, BN, and the transition-metal dichalcogenides (TMDs) are perceived as attractive candidates for ultrascaled electronic devices. In this work, we discuss a few novel device concepts based on them. We discuss the challenges, as well as the opportunities for these materials in electronics.

I. Introduction

Traditional semiconductor materials such as Si, GaAs, and GaN are sp^3-bonded 3D crystals. Each of these three semiconductors is famously successful in delivering technology: Si for digital electronics, GaAs for communications, and GaN for solid-state lighting and power electronics.

As successive scaling generations of conventional CMOS nodes become increasingly challenging, a parallel search for a critical breakthrough is ongoing. A new crop of low-power switching transistors are being conceived by modifying the fundamental transport physics from electrons flowing over a gate-controlled potential barrier, to one where electrons quantum-mechanically tunnel through the bandgap in tunneling field-effect transistors (TFETs). Internal voltage gain is being investigated to leave the basic conduction mechanism of the FET intact, while empowering the gate dielectric by making it of an active material: such as ferro- and piezo-electric [1] layer to beat the Boltzmann limit of 60 mV/decade. One can even imagine combining these mechanisms to reduce the sub-threshold slope even further.

However, one of the major hurdles moving forward is that the semiconductor channel region is becoming very *small*. Thus every physical property we add to gain an advantage in performance must also scale. It is for this reason that the advent of 2D crystal semiconductors has caused excitement in the field [2]. These materials can be physically much thinner than sp^3 bonded materials, and perhaps enable scaling of FETs, and even TFETs to smaller dimensions [Fig 1]. The conduction and valence band electronic states of the transition metal dichalcogenide semiconductors have large contributions from d-orbitals, a feature that is absent in conventional semiconductors. Though the emergent properties may be found interesting for logic applications, we are at a very early stage of investigating these materials. There are significant challenges facing us in taking 2D crystal semiconductor materials towards electronic devices. The field is also replete with opportunities.

II. 2D Crystal FETs

TMDs channel FETs how appreciable switching [Fig 2] because of the presence of a bandgap – both in their single layer, and multilayer forms [3, 4]. The carrier transport properties in them do not appear to be far superior to Si at this stage [Fig 3]. If low-temperature large-area growth methods preserving ~50 cm^2/Vs mobilities could be developed for TMD crystals, they might find applications in thin-film transistors (TFTs) for displays. The challenges are in the material growth, controlled doping, and low-resistance ohmic contacts [5]. These are rather severe challenges, and are deeply interlinked. For example, "ohmic" contact resistances of ~10 Ω-mm or higher severely degrade FET performance of such FETs [Fig 3, Ref 5]. Moving forward, a possible route for TMD FETs may be to use heavily doped multilayer regions for low-resistance ohmic contacts, and few-layer regions for channels that can sustain electrostatic scaling. Possible FET advantages could be the absence of interface roughness issues, very low interface traps, and extended scalability. The gate insulator, and the semiconductor-insulator interface is the most critical junction of a FET. One can then consider 2D crystal insulators for this purpose - 2D BN has the potential to serve as a gate insulator without dangling bonds for FET-applications.

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III. Tunnel FETs

The TFET approach to low-power switching transistors is being explored extensively using 3D semiconductors with encouraging gains in the performance in a few short years. When 3D semiconductors used for TFETs are scaled down to nm-level dimensions, the energy bandgap increases by quantum confinement. Since tunneling currents depend exponentially on the bandgap, they can cause uncontrollable variation and low on-currents.

Appenzeller et al. observed sub-60 mV/decade switching in semiconducting carbon nanotubes (CNTs) [6]. The control of chirality and diameter of CNTs remains a challenge: these properties determine the energy bandgap, and the resulting tunneling currents. Significant progress has recently been reported in this arena for CNTs. With the discovery of graphene, it was conceived that lithographically patterned graphene nanoribbons could mimic the tunneling currents of, but with planar control, precise placement, and controlled bandgaps [7]. Furthermore, it is difficult to chemically dope CNTs because of the absence of dangling bonds. The bonds at the edges of an etched GNR allow chemical doping [8]. Heat dissipation out of GNR channels into the substrate is more efficient than CNTs. Since the energy bandgaps of GNRs go roughly as ~1.2/W eV where W is the width in nm, GNRs of ~5 nm width are desired. This is a significant challenge, and the line-edge roughness can be very detrimental to device performance. But progress is being made. Such dimensions may be achievable in the future by leveraging FinFET process technology. Fig 4 shows the projected performance of GNR TFETs [7], and a recent realization in our group. Here, instead of chemical doping for the p-n tunnel junction, electrostatic ionic-doping was used. The GNRs were of ~10 nm width, and clear room-temperature NDR and switching behavior was observed. At room temperature the switching is weak because of the small gap. However, this result indicates that in spite of all issues, the GNR TFET remains a highly attractive and viable approach for a high-performance TFET. The atomically thin body allows for the highest scaling, and the symmetric bandstructure allows for natural nTFET and pTFET realizations, properties that are missing in traditional semiconductors. In a recent industrial benchmark comparing various competing novel electronic and magnetic logic switches, the GNR TFET remains among the most attractive with the lowest energy-delay product for various digital operations [9].

Monolayer TMD crystals are sub-nm in thickness, and yet exhibit a robust bandgap. Thus, they offer the possibility of high-performance TFETs with high scalability [2]. In addition, the lower dimensions buy potential advantages in topology and coupling in of higher tunneling electric fields than is possible in conventional 3D semiconductors [Fig 5]. Futher gains in tunneling currents occur through transport physics by the collimation of electron momenta in the *k*-space [10]. These factors result in boosting the tunneling current drives for the on-state. Major challenges in material and process control, lithography, and doping, however, need to be addressed to make such interlayer tunneling devices with 2D crystals a reality.

IV. SymFETs

Based on the vertical TFET topology [Fig 5], a remarkable device functionality [11] emerges when the p- and n-semiconductor channels are replaced by graphene [Fig 6]. Single-particle tunneling is a robust phenomenon in semiconductor heterostructures. Because of the perfect symmetry of the bandstructure of graphene, the single-particle interlayer tunneling current undergoes a sharp maximum with a strong NDR as a function of both gate and drain voltage sweeps. The predicted SymFET behavior has recently been observed at room temperature and is the first truly novel device possible with 2D crystals [12]. The device is a single-particle counterpart of the BISFET [12]. One can foresee that this sort of switching behavior is not limited to graphene: for example, a vertically stacked MoS_2 p-n junction can deliver similar switching behavior. Such unconventional electronic devices resulting from 2D crystals hold much future promise.

V. Acknowledgements

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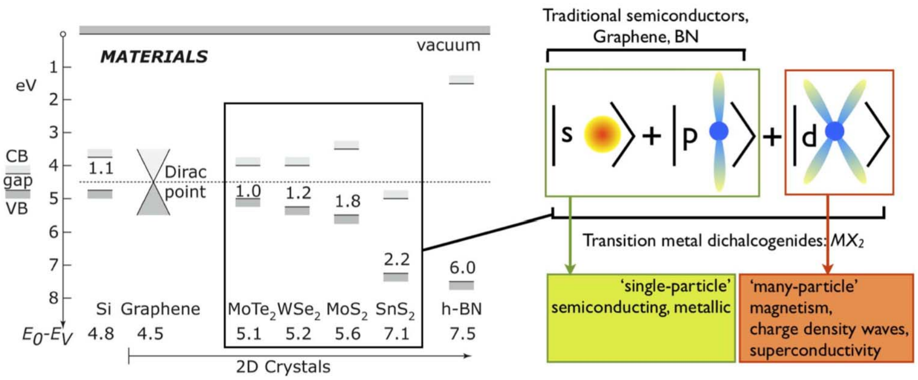

Figure 1: Energy bandgaps and lineups of 2D crystal materials in comparison to silicon. While the chemical bonds in graphene and BN are formed by sp^2 orbitals, those in the transition metal dichalcogenides involve d-orbitals. This is a departure from traditional 3D crystal semiconductors that are primarily sp^3-bonded [Ref 2].

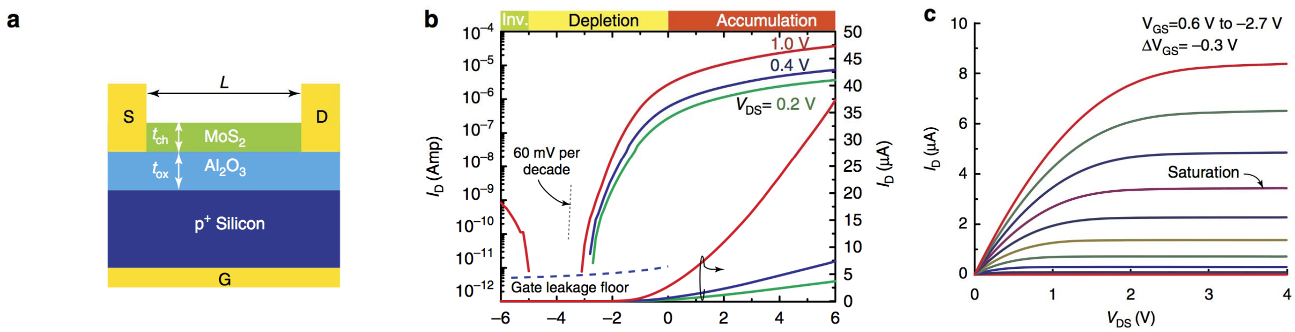

Figure 2: A traditional FET made from a multilayer MoS_2 crystal channel. The channel material is exfoliated from naturally occurring crystals and transferred to a back-gated substrate (a). Ohmic contacts are deposited, and the FET exhibits high current modulation (b) and current saturation (c). The existence of a bandgap results in an expected transistor behavior, but due to high-resistance ohmic contacts, the current drives are low [Ref 4].

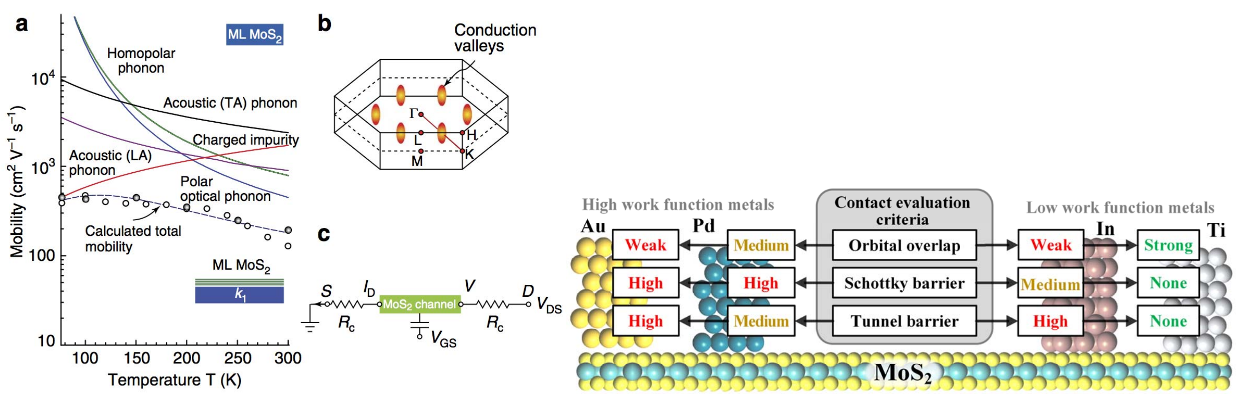

Figure 3: Electron mobility in multilayer MoS_2 channels at room temperature approaches few 100 cm^2/Vs limited by phonon scattering [Ref 4] in multivalley transport (a,b,c). Ohmic contacts must be considered to extract mobilities, and in-depth studies are necessary to achieve lower contact resistances [Ref 5].

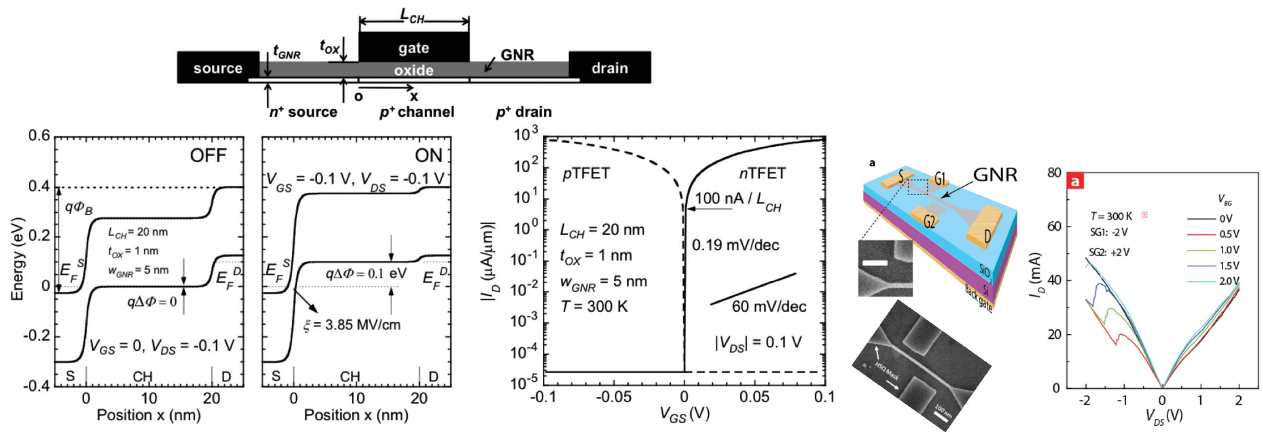

Figure 4: Projected performance of a graphene nanoribbon based tunneling field-effect transistors (TFET) [Ref 7]. The atomically thin nature allows for the maximum scaling, while delivering high currents at low applied voltages. The major challenges are in the fabrication and doping of the material. Experimental room-temperature gate-controlled NDR in side-gated GNR TFET structures.

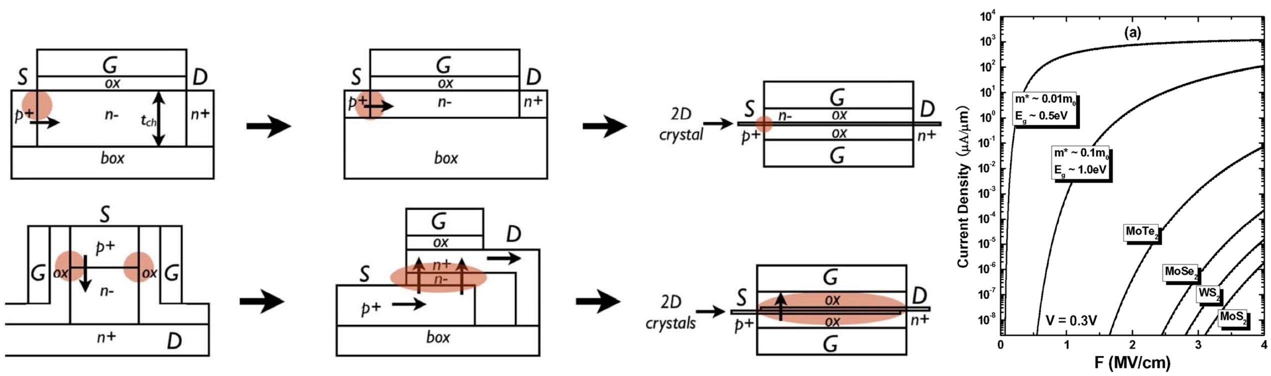

Figure 5: Various topologies of TFETs showing the scaling advantages of fabricating such devices with 2D crystal semiconductors [Ref 2]. The atomically thin nature of 2D crystal semiconductors allows scaling of TFETs to much smaller dimensions than 3D crystal semiconductors. Interband tunneling currents in TMDs [10].

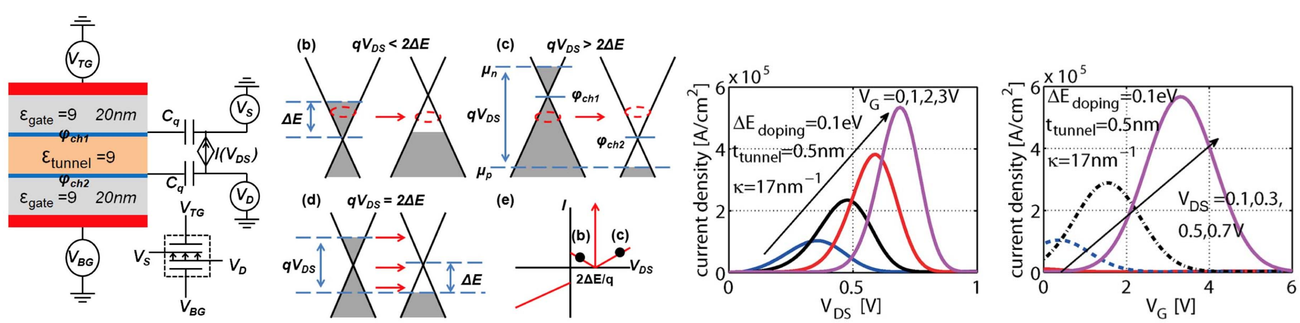

Figure 6: The Symmetric Field-Effect Transistor (SymFET) [Ref 11]. This variant of a TFET exploits the perfect symmetry of the electronic bandstructure of 2D graphene. The interlayer tunneling current between graphene sheets undergoes a sharp maximum when the Dirac points are aligned, leading to NDR behavior in both gate and drain biases. The projected behavior has been recently observed at room temperature and shows promise [Ref 12].