Dispersion-free operation in InAlN-based HEMTs with ultrathin or no passivation

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Abstract: The origin and management of DC-RF dispersion in InAlN-based GaN high electron mobility transistors (HEMTs) is examined, in conjunction with consideration of the implications for device speed. This study, in which GaN HEMTs with alloyed and non-alloyed ohmic contacts are compared, renders the following observations and hypotheses: 1) We show and explain that dispersion free operation can be achieved without passivation. 2) The root cause of dispersion associated with surface states is often introduced during device processing; in particular, unintentional or un-optimized oxidation of the HEMT surface. 3) These undesired surface states also lead to gate extension (virtual gate), which decreases device speed but increases the breakdown voltage. In addition, the function and efficacy of a plasma-based ultrathin passivation is evaluated.

Introduction: DC-RF dispersion in GaN millimeter wave transistors and dynamic R_{on} in GaN power switches are two key issues that must be resolved in the development of high-performance GaN electronics. The community has long speculated that surface states near the gate that trap and de-trap electrons are the origin of these phenomena [1]. These surface states are also often linked to the source of the 2D electron gas (2DEG) in the channel [2] and surface Fermi level pinning. A successful passivation scheme should result in minimal charge depletion in the channel due to surface states and provide protection from moisture and other adsorbates that could introduce dipoles on the surface or chemically alter the semiconductor surface, thus leading to device instability or dispersion. Typically, GaN HEMTs employ ohmic contacts alloyed at T > 800 ^oC and a plasma-enhanced chemical vapor deposition (PECVD) SiN_x passivation exceeding a critical thickness, e.g. 60 nm, to achieve satisfactorily low dispersion, e.g. < 5% degradation in I_{dmax} near 1 MHz. Ultrathin dielectric passivation schemes on GaN HEMTs with alloyed contacts have also been reported, including 3 nm catalytic chemical vapor deposition (Cat-CVD) SiN [3], 4 nm plasma-oxide [4,11], 4 nm atomic layer deposition (ALD) AlN [5] and 1.5 nm thermal oxide of InAlN [6], often accompanied by an appreciable increase in the channel 2DEG concentration n_s upon passivation.

Higashiwaki et al. reported [2] that the rather widely observed Fermi level (E_f) pinning in GaN HEMTs is induced by the ohmic alloying process at high temperatures while E_f is not pinned in the as-grown HEMTs. Since in the recent years we developed the non-alloyed MBE regrown ohmic contacts to pursue the highest speed in GaN HEMTs [7-11], we have had a unique opportunity to investigate the dispersion behavior in GaN HEMTs whose free surface is similar to the as-grown surface with minimal exposure to high temperature or plasma processes, which might introduce a large density of surface/border states near the mid bandgap of the barrier (or the often ill-defined term of Fermi level pinning). Nearly dispersion-free operation has been routinely observed in our unpassivated GaN HEMTs, confirming *the HEMT surface E_f is* <u>*well above midgap*</u>.

Experiments: Ternary barrier $In_{0.17}Al_{0.83}N$ and quaternary barrier $In_{0.13}Al_{0.83}Ga_{0.04}N$ HEMTs on SiC with a top barrier thickness of 4~11 nm and no back barrier have been evaluated. The devices with alloyed ohmic contacts were fabricated using a process similar to that detailed in [4] with a contact resistance R_c~0.38 ohm•mm while the devices with non-alloyed contacts were fabricated using a process similar to that detailed in [10, 12] with a contact resistance R_c~0.27 ohm•mm. The main difference in these alloyed and non-alloyed contacts devices is that the HEMT surfaces are directly subject to high temperature annealing process in the alloyed contact process, while in the non-alloyed contact process the surface is protected by the regrowth mask SiO_2 in the regrowth process around 650 ^oC and the surface did not directly exposed to any high temperature thereafter. The passivation schemes evaluated include PECVD SiN_x, atomic layer deposition (ALD) Al_2O_3, oxide formed by treating the InAl(Ga)N surface with O_2/Ar plasma (previously denoted as dielectric-free passivation or DFP) [4] and here referred to as plasma-oxide to be more accurate. Gate lengths from 30 to 250 nm with widths of 2 x 50 µm were used. The source drain distance for alloyed and non-alloyed device is ~1.6 µm and ~1 µm, respectively.

Results and Discussion: Three representative scenarios are illustrated in Figs.1-3. In Fig. 1, HEMTs with non-alloyed regrown contacts are shown. The as-fabricated devices <u>*without any passivation*</u> (plasma or dielectric based) exhibit essentially <u>*no dispersion*</u> (Fig.1e) and a high f_t of ~180 – 220 GHz for L_g ~60 – 100 nm (I-gate) (Fig.1f). Close examinations by transmission electron microscopy (TEM) revealed no discernable oxide on the InAlN barrier surface in either the access region or under the gate (Fig. 1b-c). In Fig.1d, HEMTs with L_g=60 nm show appreciable short channel effects (SCEs) which is expected since the top barrier is about 10 nm and there is no back barrier. After deposition of 6 nm ALD Al_2O_3, f_t reduced by ~10% (Fig. 1f), indicating the parasitic delay introduced by this ultrathin dielectric passivation is more significant than the possible reduction in gate extension. In addition, these devices exhibit dramatically increased dispersion (~50% shown in Fig. 1g) and a reduction in both f_t and SCEs (not shown) after being subject to a high temperature annealing. In contrast, minimal SCEs, large dispersion and a low f_t ~ 125 GHz for L_g ~ 60 nm were observed in as-processed HEMTs with alloyed ohmics (Fig. 2d-f), indicating a very strong virtual gate effect. With passivation (PECVD SiN_x, ALD Al_2O_3), f_t and SCEs increase and dispersion reduces, often gradually with increasing dielectric thickness (Fig. 2g). TEM revealed the presence of a thin layer (~1.5 – 2.0 nm) of largely crystalline InAlGaN oxide on the entire HEMT surface as shown in Fig. 2b and

Fig. 2c, a strong indication that this oxide was formed during the high temperature ohmic alloying process when the entire surface was exposed to the ambient.

Dielectric-based passivation presents a dilemma between minimizing dispersion and gate extension (typically demanding thick dielectrics with an equivalent oxide thickness EOT higher than 60 nm) and introducing minimal capacitive delay (demanding as thin dielectrics as possible). To address this tradeoff, we have explored the use of an O_2/Ar plasma (Fig. 3) to amorphorize the top InAlGaN barrier (~ 4 nm) at the access region into an Al-rich oxide passivation layer as shown in Fig. 3c without introducing extra parasitic capacitances. Though we have previously reported various resultant devices [4,8-11], here we present the comprehensive physical and chemical evidences that corroborate the observed electronic behavior. The plasma-oxide passivated devices show ideally intrinsic behaviors: strong SCEs, negligible dispersion and high f_t of 220 GHz [9]; similar to the HEMTs with non-alloyed ohmics in Fig. 1. Their characteristics stayed largely the same over months of study. To further improve the device stability, a low permittivity moisture barrier or hermetic packaging is needed. Hall-effect measurements have been used to monitor the transport characteristics in the access region. As shown in Fig. 3f, the channel resistance R_{sh} of 253 ohm/sq after ohmic alloying is higher than the value of the as-grown wafer determined by the contactless Hall-effect measurements. The charge increases after the plasma treatment and R_{sh} decreases to the as-grown value with the plasma treatment as short as 15 sec and remains the same for longer treatments. X-ray photoelectron spectroscopy (XPS) data shown in Fig. 3g confirms that the rapid thermal processing (RTP) treated device has higher oxygen content than control and BCl_3 treated samples, suggesting the surface oxide is formed during the high temperature ohmic annealing process.

Based on the collective observations above, we summarize our understanding on passivation in Fig. 4. A successful passivation (plasma and/or dielectric based treatments) results an increase or recovery in n_s in the access region, >2x higher than that under the gate at 0 V (Fig. 4a). The gate extension due to ohmic alloying in our InAlN HEMTs has been found to be >60 nm [4], in stark contrast to the expected value of ~10 nm near the peak f_t bias conditions. Such a long virtual gate corresponds to a low n_s at the access region, as illustrated in Fig. 4b-c. On the other hand, passivated device has a higher n_s at the access region, thus resulting in a much shorter virtual gate (~10 nm) as illustrated in Fig. 4d-e, which leads to nearly dispersion-free operation thanks to the poor electrostatics in the virtual gate region due to the extremely short virtual L_g. This physical picture is essentially consistent with what was demonstrated by R. Coffie et al. [13] and L. Shen et al. [14]. The insight gained on these high speed GaN HEMTs (thus highly sensitive to dispersion) might also help shed light on the previously reported dispersion-free operation without passivation [15-16].

Conclusion: Use of either non-alloyed ohmics or passivations (plasma or dielectric based) that lead to small gate extension enable nearly dispersion free operation in InAl(GaN)N HEMTs. **Acknowledgement**: This work was supported partly by the DARPA NEXT program, the AFOSR and AFRL/MDA.

References

[1] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, “The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs”, *IEEE Trans. Electron Devices*, vol. 48, pp. 560–566, Mar. 2001.

[2] M. Higashiwaki, S. Chowdhury, M.-S. Miao, B. L. Swenson, C. G. Van de Walle,and U. K. Mishra, "Distribution of donor states on etched surface of AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 108, pp. 063719, 2010

[3] M. Higashiwaki, T. Mimura and T. Matsui, "AlN/GaN insulated-gate HFETs using Cat-CVD SiN," *IEEE Elec. Dev. Lett.*, vol. 27, pp. 719, Sep 2006

[4] R. Wang, G. Li, O. Laboutin, Y. Cao, W. Johnson, G. Sinder, P. Fay, D. Jena, and H. Xing, “210 GHz InAlN HEMTs with Dielectric-Free Passivation,” *IEEE Elec. Dev. Lett.*, vol. 32, no. 7, pp. 892-894, Jul. 2011.

[5] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, “Effective passivation of AlGaN/GaN HEMTs by ALD-grown AlN thin film,” IEEE Electron Devices Lett., vol. 33, no. 4, pp. 516–518, Apr. 2012

[5] E. Kohn et al., “Ultrathin passivation of InAlN/GaN HEMT device structures,” *WOCSDICE* (2013).

[6] J. Guo, Y. Cao, C. Lian, T. Zimmermann, G. Li, J. Verma, X. Gao,S. Guo, P. Saunier, D. Jena, and H. Xing, “Metal-face InAlN/AlN/GaN high electron mobility transistors with regrown ohmic contacts by molecular beam epitaxy,” *Phys. Stat. Sol. (A)*, vol. 208, no. 7, pp. 1617–1619,Jul. 2011.

[7] J. Guo, G. Li, F. Faria, Y. Cao, R. Wang, J. Verma, X. Gao, S. Guo, E. Beam, A. Ketterson, M. Schuette, P. Saunier, M. Wistey, D. Jena and H. Xing, "MBE-Regrown Ohmics in InAlN HEMTs With a Regrowth Interface Resistance of 0.05 Ohm. mm," *IEEE Elec. Dev. Lett.*, vol. 33, pp. 525-527, Apr. 2012.

[8] R. Wang, G. Li, J. Verma, T. Zimmermann, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena and H. Xing, "Si-Containing Recessed Ohmic Contacts and 210 GHz Quaternary Barrier InAlGaN High-Electron-Mobility Transistors," *Appl. Phys. Express*, vol. 6, pp. 096502, 2011

[9] R. Wang, G. Li, J. Verma, B. Sensale-Rodriguez, T. Fang, J. Guo, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena and H. Xing, "220 GHz Quaternary Barrier InAlGaN HEMTs," *IEEE Elec. Dev. Lett.*, vol. 32, pp. 1215, 2011.

[10] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, H. Xing, “370 GHz InAlN/GaN HEMTs with Regrown Ohmic Contacts,” *IEEE Elec. Dev. Lett.*, vol. 33, no. 7, pp. 988-990, Jul. 2012

[11] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, H. Xing " Ultrascaled InAlN/GaN High Electron Mobility Transistors with Cutoff Frequency of 400 GHz," *Jpn. J. Appl. Phys*, vol. 52, no. 8, pp. 08JN14-1 - 08JN14-2, Aug. 2012

[12] R. Wang, G. Li, G. Karbasian, J. Guo, B. Song, Y. Yue, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. Xing, “Quaternary Barrier InAlGaN HEMTs With fT/fmax of 230/300 GHz,” *IEEE Elec. Dev. Lett.,* vol. 34, no. 3, pp. 378-380, Mar. 2013

[13] R. Coffie, D. Buttari, S. Heikman, S. Keller, A. Chini, L. Shen, and U. K. Mishra“p-Capped GaN–AlGaN–GaN High-Electron Mobility Transistors (HEMTs),” *IEEE Elec. Dev. Lett.,* vol. 24, no. 10, pp. 588-590, Oct. 2003

[14] L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. P. Denbaars, and U. K. Mishra, "Unpassivated GaN/AlGaN/GaN power high electron mobility transistors with dispersion controlled by epitaxial layer design," *J ELECTRON MATER,* vol. 33, pp. 422-425, 2004.

[15] S. Arulkumaran et al. “Current collapse-free i-GaN/AlGaN/GaN high-electron-mobility transistors with and without surface passivation.” Appl. Phys. Lett. Vol. 85, No. 23, pp.5745-7, Dec. 2004.

[16] N. G. Weimann et al. “Unpassivated AlGaN-GaN HEMTs with minimal RF dispersion grown by plasma-assisted MBE on semi-insulating 6H-SiC substrates”, *IEEE Elec. Dev. Lett.,* vol. 24, no. 2, pp. 57-59, Feb. 2003

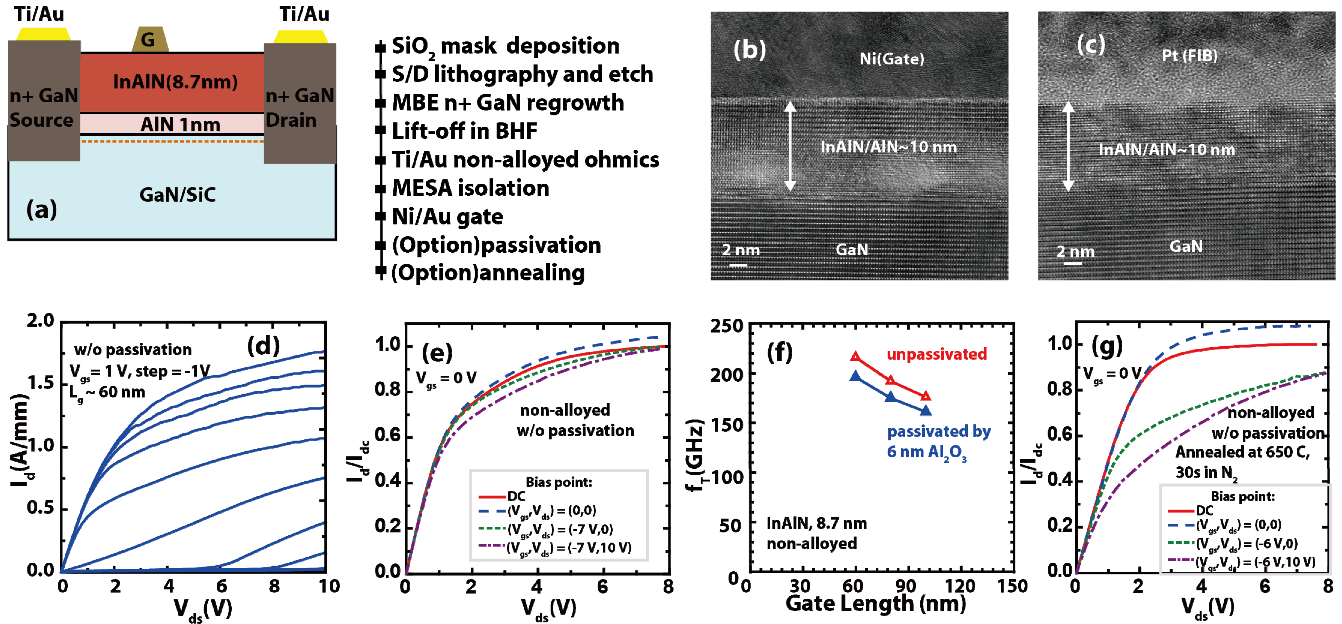

Fig. 1 InAlN-based HEMTs with non-alloyed regrown contacts. (a) Device schematics and process flow. The PECVD SiO_2 regrowth mask deposition was optimized to minimize damage to the InAlN HEMT (b-c) Cross section HRTEM images of the gated and access regions. The entire InAlN barrier was found to be crystalline and no discernable oxides were detected by EDX (not shown). The apparent contrast within the InAlN barrier resulted from the TEM sample preparation damage. (d) I_d-V_{ds} curves of a 60 nm HEMT, showing expected strong SCEs. (e) Pulsed I-Vs using 300 ns pulses and a duty cycle of 0.5 ms, showing nearly dispersion free operation without any passivation. (f) The passivated devices show ~ 10% reductions in f_t over the as-processed without any passivation. (g) Large dispersion is observed when subjecting the as-processed devices with no passivation to a high temperature annealing, indicating formation of undesired surface states leading to a large virtual gate. TEM (Fig. 2) and XPS (Fig. 3) confirmed oxide formation during the annealing. All device I-Vs shown here were taken in air at room temperature.

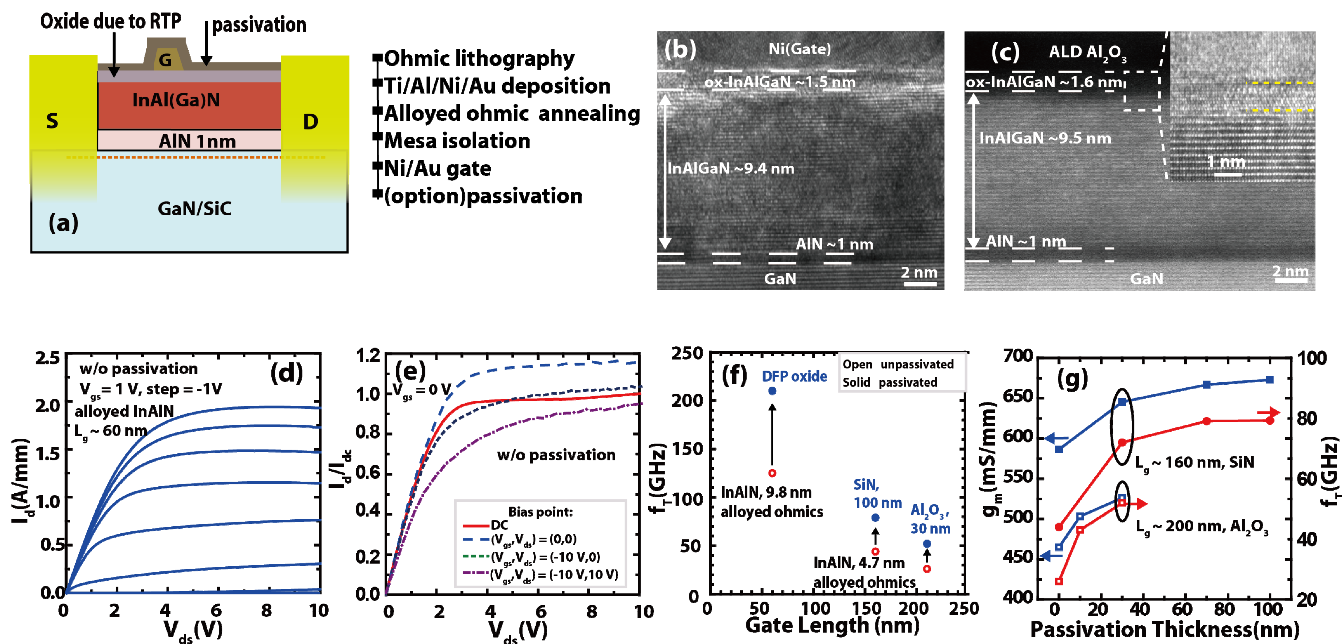

Fig. 2 InAlN-based HEMTs with alloyed ohmic contacts. (a) Device schematics and process flow. (b-c) STEM and HRTEM images showing the presence of a thin oxygen-rich layer on the surface of InAlGaN HEMTs under the gate and access region, formed during the ohmic annealing process. The inset shows this oxide layer is largely crystalline. (d-e) I_d-V_{ds} curves of as-processed HEMTs without passivation, showing a large DC-RF dispersion and minimal SCEs [4]. (f) f_t of various HEMTs with alloyed ohmic contacts before and after passivation. (g) Dependence of transconductance and f_t on the dielectric passivation thickness (PECVD SiN and ALD Al_2O_3 are shown). The increase in g_m/f_t results from an increase in the channel n_s of the access region and shortening of the gate extension. It is also worth noting that if the thermal oxide is optimized, it can serve as an effective passivation [6].

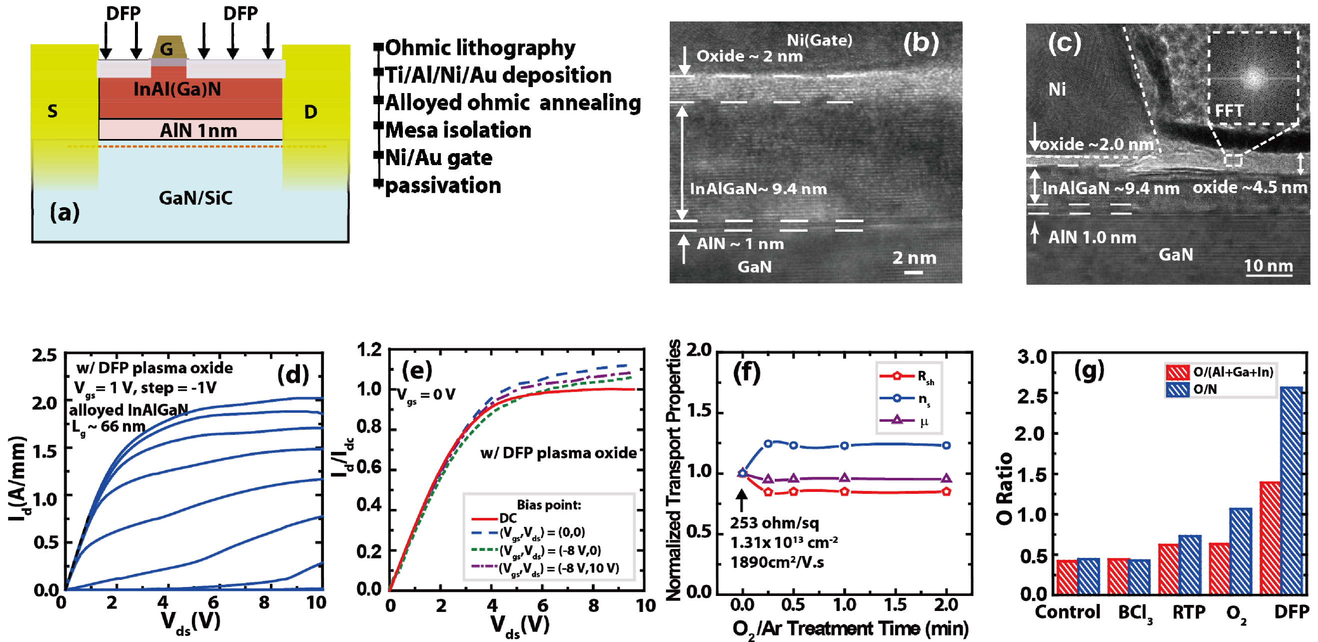

Fig. 3 InAlN-based HEMTs with alloyed ohmic contacts. The access region was treated with an O_2/Ar plasma and the resultant passivation is denoted as the plasma-oxide (DFP). (a) Device schematics and process flow. (b-c) HRTEM images showing the thermal oxide under the gate and the plasma oxide in the access region. The inset shows the FFT of the enclosed region of the plasma oxide, confirming it is amorphous. (d-e) I_d-V_{ds} curves and pulsed I-Vs of these HEMTs with plasma oxide passivation. Strong SCEs, negligible dispersion and high f_t (220 GHz [9]) were observed. (f) The 2DEG transport properties in the access region monitored by the Hall effect measurements. After ohmic alloying, the channel resistance R_{sh} of 253 ohm/sq is higher than the value of the as-grown wafer determined by the contactless Hall effect measurements. R_{sh} decreases to the as-grown value with the plasma treatment as short as 15 sec and remains the same for longer treatments. (g) The XPS scans show a higher oxygen level on the surface of the sample subjected to an ohmic annealing process (RTP), further confirming formation of the thermal oxide as seen in Fig. 2b-c.

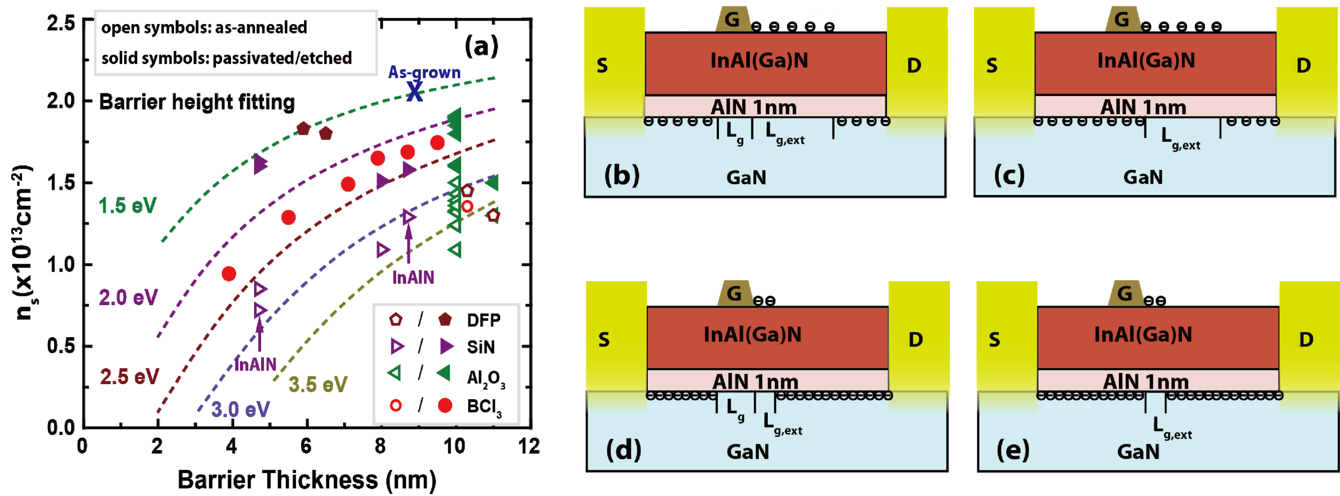

Fig. 4 (a) Summary of the effective barrier height at the InAlN barrier surface for various HEMT structures with different barrier thicknesses as well as plasma and dielectric based treatments. In passivated (solid symbols) and unpassivated HEMTs with non-alloyed contacts (same with the as-grown) a lower effective barrier height (i.e. a higher n_s) is observed, leading to a short $L_{g,ext}$. A proposed explanation on the dispersion behavior difference in GaN HEMTs with low and high n_s is also illustrated. (b-c) describe the HEMTs with a low n_s, e.g. the one in Fig. 2d-e. Under pinch off condition (b), the virtual gate forms since the surface states trap electrons injected from the gate and the electrons in the channel are depleted. Because of the low n_s, $L_{g,ext}$ is long. In pulsed I-V measurements, when quickly biased to open channel (c), this long gate extension acts as an effective gate under pinch off results in a significant decrease in current. The case for HEMTs with high n_s is illustrated in (d-e). Under pinchoff (d), electrons under the gate and virtual gate are depleted. When quickly biased to open channel (e), the poor electrostatics associated with the extremely short virtual gate prevents the virtual gate from modulating the current; as a result, dispersion is small.