

# Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe<sub>2</sub> Field Effect Transistors

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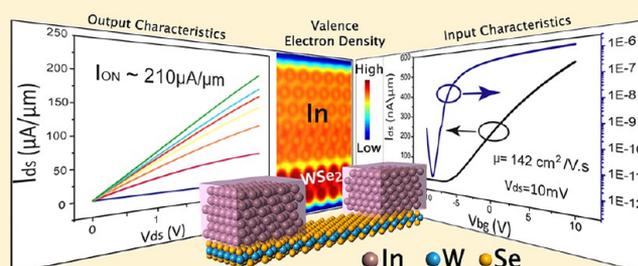
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## S Supporting Information

**ABSTRACT:** This work presents a systematic study toward the design and first demonstration of high-performance n-type monolayer tungsten diselenide (WSe<sub>2</sub>) field effect transistors (FET) by selecting the contact metal based on understanding the physics of contact between metal and monolayer WSe<sub>2</sub>. Device measurements supported by ab initio density functional theory (DFT) calculations indicate that the d-orbitals of the contact metal play a key role in forming low resistance ohmic contacts with monolayer WSe<sub>2</sub>. On the basis of this understanding, indium (In) leads to small ohmic contact resistance with WSe<sub>2</sub> and consequently, back-gated In–WSe<sub>2</sub> FETs attained a record ON-current of 210  $\mu\text{A}/\mu\text{m}$ , which is the highest value achieved in any monolayer transition-metal dichalcogenide- (TMD) based FET to date. An electron mobility of 142  $\text{cm}^2/\text{V}\cdot\text{s}$  (with an ON/OFF current ratio exceeding  $10^6$ ) is also achieved with In–WSe<sub>2</sub> FETs at room temperature. This is the highest electron mobility reported for any back gated monolayer TMD material till date. The performance of n-type monolayer WSe<sub>2</sub> FET was further improved by Al<sub>2</sub>O<sub>3</sub> deposition on top of WSe<sub>2</sub> to suppress the Coulomb scattering. Under the high- $\kappa$  dielectric environment, electron mobility of Ag–WSe<sub>2</sub> FET reached  $\sim 202 \text{ cm}^2/\text{V}\cdot\text{s}$  with an ON/OFF ratio of over  $10^6$  and a high ON-current of 205  $\mu\text{A}/\mu\text{m}$ . In tandem with a recent report of p-type monolayer WSe<sub>2</sub> FET (Fang, H. et al. *Nano Lett.* 2012, 12, (7), 3788–3792), this demonstration of a high-performance n-type monolayer WSe<sub>2</sub> FET corroborates the superb potential of WSe<sub>2</sub> for complementary digital logic applications.

**KEYWORDS:** 2D semiconductors, contact resistance, field-effect-transistor, monolayer, transition-metal dichalcogenides, tungsten diselenide



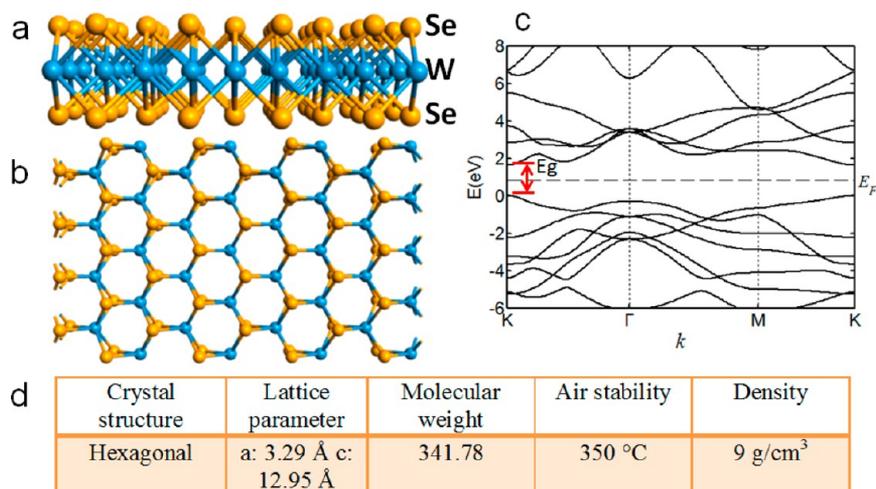
The first successful demonstration of a thermodynamically stable two-dimensional (2D) material in the form of graphene (a single sheet of hexagonally arranged carbon atoms) with its outstanding electrical, optical and thermo-mechanical properties has truly opened up a new era for a wide range of 2D materials and their electronic applications.<sup>1</sup> However, the zero band gap of graphene makes it difficult to turn off graphene-FETs and therefore is unsuitable for use in digital circuit applications, where high ON/OFF ratios are required.<sup>2</sup> Hence, as silicon-based complementary metal-oxide-semiconductor scaling approaches its limits ( $< 5 \text{ nm}$ ), it is highly desirable to explore alternative atomically thin 2D materials with large band gaps and high mobility.<sup>3</sup> Such ultrathin channel materials with relatively large band gaps can potentially minimize short channel effects owing to better electrostatics and reduce source–drain subthreshold leakage (thereby achieving higher ON/OFF ratio) for digital circuit applications. Recently, monolayer transition-metal dichalcogenides (TMD), a family of 2D semiconductor layers arranged in a hexagonal lattice (Figure 1a,b) have been produced by mechanical exfoliation<sup>4</sup> or grown by chemical vapor deposition.<sup>5,6</sup> Monolayer TMDs such as MoS<sub>2</sub> and WSe<sub>2</sub> (Figure 1c) are direct band gap semiconductors with bandgaps ( $E_g$ ) in the range of 1.2–1.8

eV.<sup>7</sup> Compared to traditional semiconducting materials such as silicon, Ge, or III–V materials, 2D TMD films have pristine surfaces free of dangling bonds. These pristine surfaces can reduce surface roughness scattering (leading to high mobilities) and also reduce interface traps resulting in low density of interface states on the semiconductor–dielectric interface. Another important feature of 2D TMD films is their atomic thickness that allows efficient electrostatics (easier control of channel charge by gate voltage) and high degree of vertical scaling. These outstanding properties of 2D TMDs that are known to be beneficial for designing ultrashort channel FETs, primarily arise due to the “layered” nature of the materials from which they derive, in which adjacent layers are held together by relatively weak van der Waals forces.

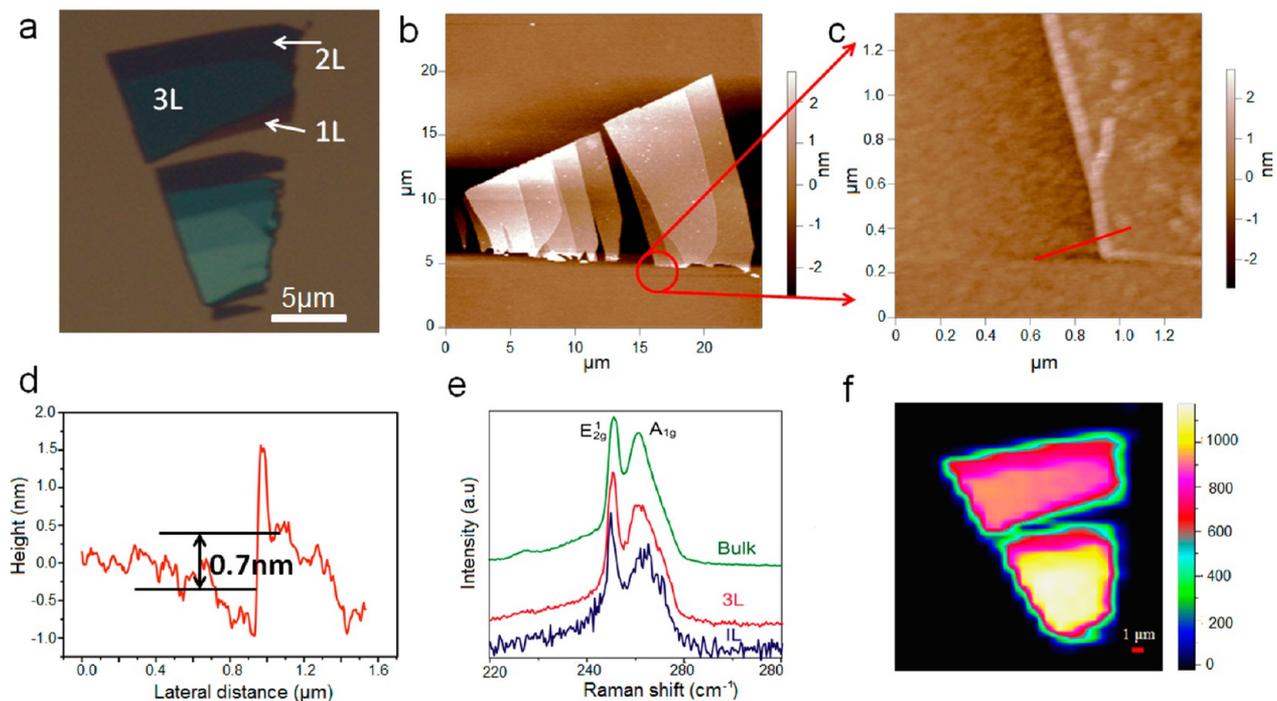
In comparison to the widely studied monolayer MoS<sub>2</sub>,<sup>7–13</sup> studies focusing on monolayer WSe<sub>2</sub> are still very limited. As a semiconductor material, bulk WSe<sub>2</sub> possesses good stability (Figure 1d) and is more resistant to oxidation in humid environments than sulphides.<sup>14</sup> Bulk WSe<sub>2</sub> crystal devices have

Received: December 27, 2012

Revised: March 11, 2013



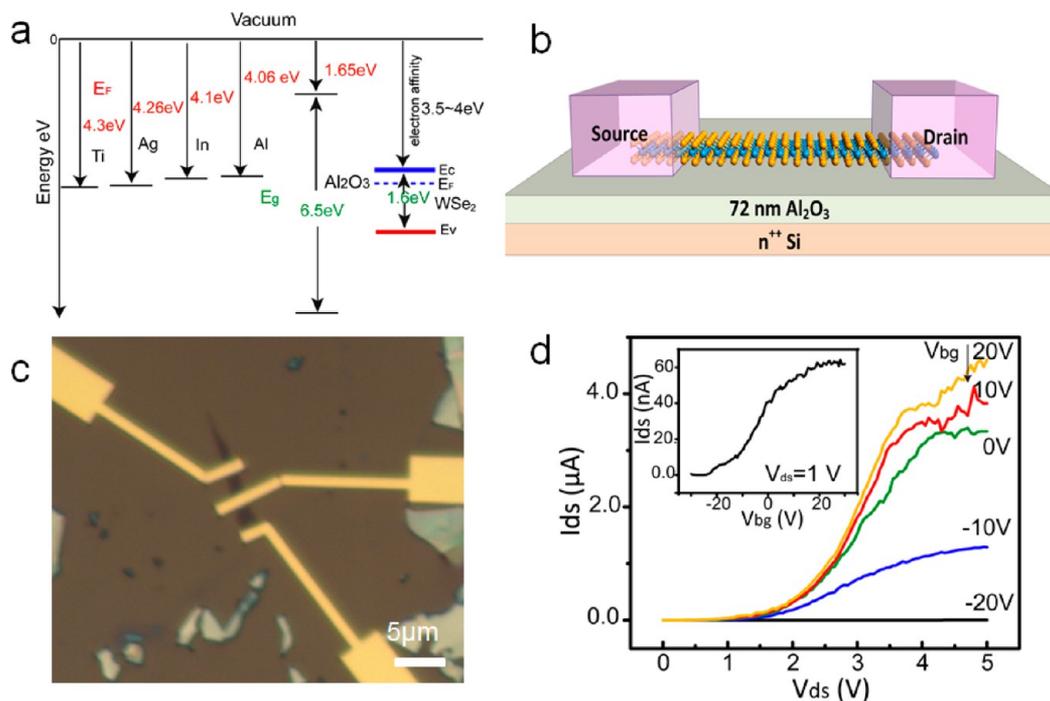
**Figure 1.** Schematic of the crystal structure of monolayer  $\text{WSe}_2$ , (a) side view and (b) top view. (c) Energy dispersions of monolayer  $\text{WSe}_2$ , indicating that monolayer  $\text{WSe}_2$  is a direct bandgap semiconductor with a bandgap of  $\sim 1.6$  eV. This diagram is calculated using the Atomistix Tool Kit (ATK) tool.<sup>18</sup> (d) Some basic physical properties of bulk  $\text{WSe}_2$ . Lattice constants  $a$  and  $c$  represent the side length (distance between two adjacent inplane selenium atoms) and the height of a unit cell in bulk  $\text{WSe}_2$ , respectively.



**Figure 2.** (a) Optical image of a  $\text{WSe}_2$  film showing monolayer (1L), bilayer (2L) and trilayer (3L) regions. (b) AFM image of the sample shown in (a). (c) AFM image of monolayer  $\text{WSe}_2$ . (d) Height profile of  $\text{WSe}_2$  measured along the red line in (c). (e) Raman mapping of the sample shown in (a). (f) Raman mapping image of the intensity of  $A_{1g}$  peak, color bar on the right shows the intensity of  $A_{1g}$  peak. Raman mapping was taken on the sample shown in (a). The wavelength of the laser used for Raman spectroscopy is 632 nm.

been studied with mobilities as high as  $500 \text{ cm}^2/\text{V}\cdot\text{s}$ <sup>15</sup> (extracted after deducting the contact resistance) exhibiting the excellent potential of  $\text{WSe}_2$  for device applications. More importantly, recent experimental<sup>16</sup> and theoretical<sup>17</sup> works have shown that monolayer  $\text{WSe}_2$  is the first TMD material in which p-type conducting behavior is observed by using high work function metal (Pd) as the contact (achieving a high FET mobility of around  $250 \text{ cm}^2/\text{V}\cdot\text{s}$ <sup>16</sup>). This important property of monolayer  $\text{WSe}_2$  provides a promising possibility to design and fabricate complementary digital logic circuits on the same monolayer  $\text{WSe}_2$  film if high-performance n-type monolayer  $\text{WSe}_2$  device can be simultaneously achieved by selecting the

proper contact metal. However, a high contact resistance has been found to be a key factor that can significantly influence device performance of bulk  $\text{WSe}_2$  FETs (extracted mobility is  $100 \text{ cm}^2/\text{V}\cdot\text{s}$  without contact corrections)<sup>15</sup> and monolayer  $\text{WSe}_2$  FETs.<sup>16</sup> Hence, it is necessary to explore methods to form low-resistance contacts to monolayer  $\text{WSe}_2$  to achieve high-performance  $\text{WSe}_2$  FETs. Our recent theoretical work has shown that it is possible to form n-type ohmic contact to monolayer  $\text{WSe}_2$  by suitable contact metals,<sup>17</sup> thereby providing guidance to experimental selection and exploration for achieving n-type  $\text{WSe}_2$  FETs. In this paper, we report high-performance n-type monolayer  $\text{WSe}_2$  back-gated FETs with



**Figure 3.** (a) Band alignments of some potential contact metals and  $\text{Al}_2\text{O}_3$  with respect to that of  $\text{WSe}_2$ .  $E_C$  and  $E_V$  represent the conduction and valence band edges of  $\text{WSe}_2$ , respectively. (b) Schematic of back-gated  $\text{WSe}_2$  monolayer FET, highly n-doped silicon serves as back gate. (c) Optical image of fabricated  $\text{WSe}_2$  monolayer FETs. (d) Output ( $I_{ds}-V_{ds}$ ) characteristics of back-gated FETs with Al (10 nm)/Au (100 nm) for different values of  $V_{bg}$ , inset shows input ( $I_{ds}-V_{bg}$ ) characteristics, this device was measured after annealing at 380 K for 1 h in vacuum, length and width of the device are 1.2 and 3  $\mu\text{m}$ , respectively. Back gate dielectric ( $\text{Al}_2\text{O}_3$ ) thickness = 72 nm and dielectric constant = 8.

ON-current of  $210 \mu\text{A}/\mu\text{m}$  at  $V_{ds} = 3 \text{ V}$  and  $I_{ON}/I_{OFF} > 10^6$  with an electron mobility of  $142 \text{ cm}^2/\text{V}\cdot\text{s}$ . The electron mobility is further enhanced to  $202 \text{ cm}^2/\text{V}\cdot\text{s}$  on a back-gated device with  $I_{ON}/I_{OFF} > 10^6$  and ON-current of  $205 \mu\text{A}/\mu\text{m}$  at  $V_{ds} = 3 \text{ V}$  by depositing a high- $\kappa$  dielectric ( $\text{Al}_2\text{O}_3$ ) layer over the channel region of the  $\text{WSe}_2$  FET.

$\text{WSe}_2$  thin films (Figure 2a) were prepared by mechanical exfoliation of bulk  $\text{WSe}_2$  (Nanoscience Instrument Inc. NS00182) on 72 nm  $\text{Al}_2\text{O}_3/\text{Si}$  (highly n-doped) substrates. The  $\text{Al}_2\text{O}_3$  film was deposited by plasma-enhanced atomic layer deposition (Oxford FlexAl) at 300  $^\circ\text{C}$ . Subsequently, the thickness of the  $\text{WSe}_2$  film was identified using optical microscope and atomic force microscope (AFM). It has been shown that optical interference allows one to discern the thickness and number of  $\text{WSe}_2$  layers from the intensity contrast under an optical microscope with visible light.<sup>19</sup> Figure 2b shows the AFM image of a  $\text{WSe}_2$  film corresponding to the sample shown in Figure 2a. Figure 2c shows the AFM image of the thin area (with the lightest optical contrast) as marked by the red circle in Figure 2b. Roughly, the thickness of this layer is around 0.7 nm, which is equal to the thickness of monolayer  $\text{WSe}_2$  (Figure 2d).<sup>16</sup> The correlation of the optical contrast and the number of  $\text{WSe}_2$  layers is marked in Figure 2a.

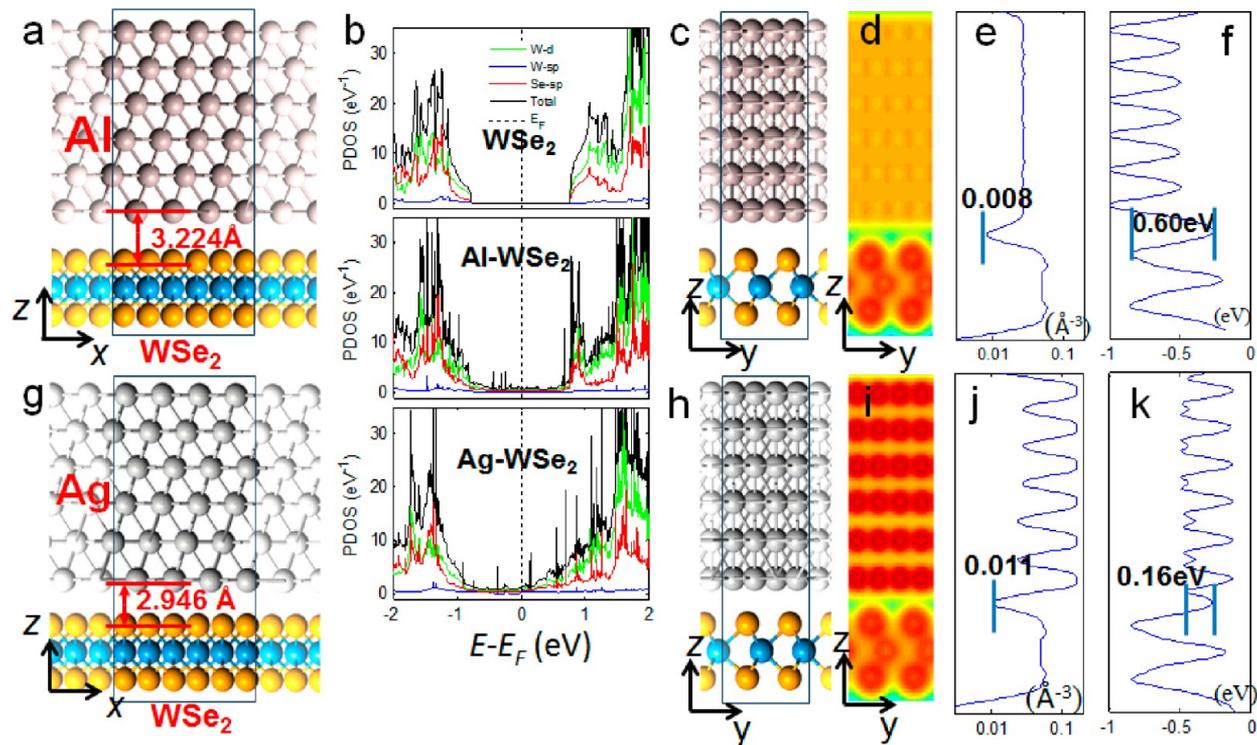
Within the TMD material family, bulk  $\text{WSe}_2$  and  $\text{MoS}_2$  have four nondegenerate Raman active modes,  $E_{2g}^2$ ,  $E_{2g}^1$ ,  $E_{1g}$  and  $A_{1g}$ .<sup>20</sup> It has been shown that both  $E_{2g}^1$  and  $A_{1g}$  modes have a thickness dependent behavior.<sup>21</sup> The in-plane  $E_{2g}^1$  mode is originally from the out-of-phase vibrations of the two chalcogenide atoms with respect to the metal atom. The  $A_{1g}$  mode corresponds to out-of-plane vibrations of the chalcogenide atoms in opposite directions. Raman spectra of thin  $\text{MoS}_2$  films have been well studied and help in identifying the thickness.<sup>21,22</sup> However, no such study exists for  $\text{WSe}_2$  thin

films that are thinner than three atomic layers. Figure 2e shows the Raman spectra of monolayer, trilayer and bulk  $\text{WSe}_2$  films. Unlike  $\text{MoS}_2$  thin films, the position of  $E_{2g}^1$  peak tends to remain constant while the  $A_{1g}$  peak position (Raman shift) decreases as the number of layer increases as shown in Figure 2e. Figure 2f shows a Raman map of the  $A_{1g}$  peak intensity. Combined with the optical image of  $\text{WSe}_2$  (Figure 2a), the intensity of  $A_{1g}$  (Figure 2f) reflects the thickness of the few layer  $\text{WSe}_2$  film, indicating that the peak intensity of  $A_{1g}$  can be used to estimate the thickness of few layer  $\text{WSe}_2$  films.

Our previous theoretical work has shown that low work function metals are desirable to achieve small n-type Schottky barrier (SB) heights with  $\text{WSe}_2$ .<sup>17</sup> Hence, Ti, Ag, In, and Al were selected as the potential contact metals for  $\text{WSe}_2$  due to their small work functions as shown in Figure 3a. Back-gated  $\text{WSe}_2$  FET devices were fabricated on 72 nm  $\text{Al}_2\text{O}_3/\text{Si}$  substrates. The source and drain regions were defined by electron-beam lithography followed by metallization. Figure 3b shows the schematic of a back-gated monolayer  $\text{WSe}_2$  FET. The optical microscope image of the fabricated back gate FET device is shown in Figure 3c.

In this study, all measurements were performed in vacuum ( $1 \times 10^{-6}$  mbar) at room temperature after annealing at 380 K for 1 h to remove absorbed moisture and solvent molecules. It has been reported that absorbed molecules on  $\text{MoS}_2$  surface can significantly decrease its device performance.<sup>23</sup> This phenomenon has also been confirmed on our  $\text{WSe}_2$  FET devices. The ON current was enhanced by at least  $\sim 100$  times after vacuum annealing as shown in the Supporting Information Figure S1.

Among Ti, Ag, Al, and In, Al has the smallest work function. On the basis of this argument alone, Al with a work function closest to the electron affinity of  $\text{WSe}_2$  would lead to the smallest Schottky barrier for electrons, thereby resulting in a



**Figure 4.** (a,c) and (g,h) Side views of the relaxed contact regions at the interface between WSe<sub>2</sub> and the Al (111) and Ag (111) surfaces, respectively; the (111) face of Ag and Al has the lowest energy. (b) PDOS (from top to bottom) of W and Se electron orbitals, for monolayer WSe<sub>2</sub>, Al–WSe<sub>2</sub>, and Ag–WSe<sub>2</sub> system, respectively. The green, blue, red, and black curves represent d-orbital of tungsten (W) atoms, sp-orbital of W atoms, sp-orbital of selenium (Se) atoms, and the total PDOS of WSe<sub>2</sub> as indicated by the legend inside the top plot. (d,i) Contour plots of the electron density in planes normal to the interface in (c,h), respectively. The contour plots represent the average electron density along the *x*-axis. (e,j) Plots of average electron density corresponding to Al–WSe<sub>2</sub> (d) and Ag–WSe<sub>2</sub> system (i). *X*- and *Y*-axis indicate average electron density and the “*z*-direction” in (d) and (i), respectively. (f,k) Plots of effective potential and the “*z*-direction” in (d) and (i), respectively. The detailed information on the DFT calculations is shown in the Supporting Information S2.

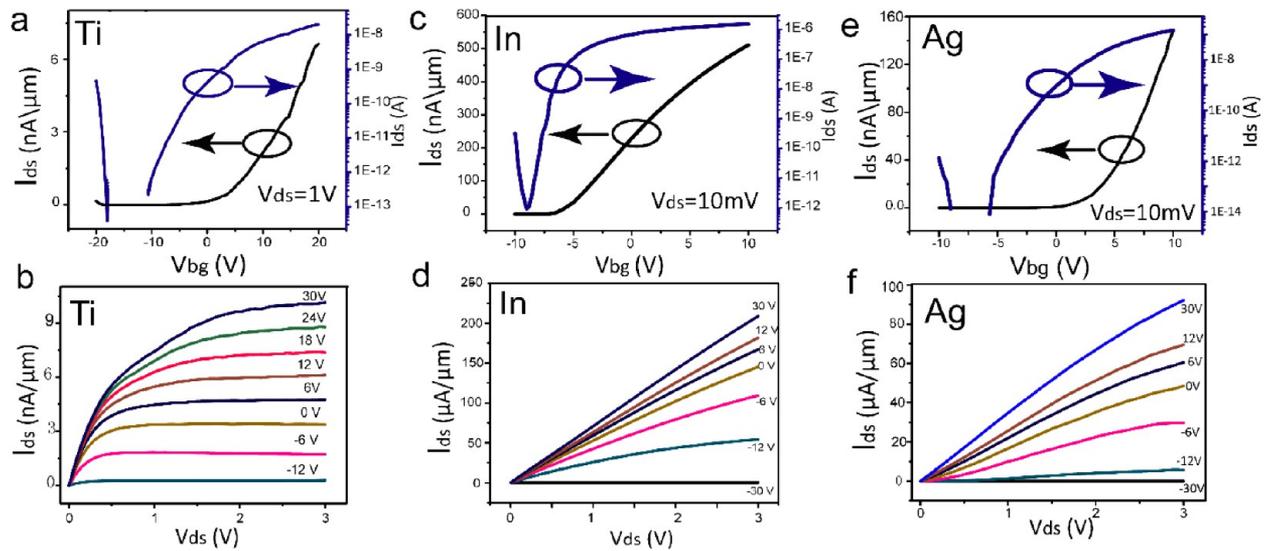
high-performance FET. As expected, the WSe<sub>2</sub> FET with an Al contact does exhibit n-channel transistor behavior as shown in Figure 3d, since the drain current increases at positive gate biases. However, the  $I_{ds}$ – $V_{ds}$  of Al–WSe<sub>2</sub> FET has a nonlinear behavior at  $V_{ds}$  values below 3 V. Moreover, application of large positive back gate biases ( $\sim 20$  V) cannot significantly modulate the  $I_{ds}$  at low  $V_{ds}$  (less than 3 V) implying the possible formation of a Schottky contact between Al and WSe<sub>2</sub>.

The field-effect carrier mobility of WSe<sub>2</sub> FET can be extracted from the linear region in  $I_{ds}$ – $V_{bg}$  (inset in Figure 3d) curve by using  $\mu = Lg_m/W(\epsilon_r\epsilon_0/d) V_{ds}$ , where  $L$  is the channel length,  $W$  is the channel width,  $\epsilon_0$  is  $8.854 \times 10^{-12}$  F·m<sup>-1</sup>,  $\epsilon_r$  for atomic layer deposition (ALD)-grown Al<sub>2</sub>O<sub>3</sub> is around 8, and  $d$  is the thickness of Al<sub>2</sub>O<sub>3</sub> (72 nm). The electron mobility calculated from each of the 10 Al–WSe<sub>2</sub> FETs is less than 0.1 cm<sup>2</sup>/V·s. However, this estimation neglects the significant voltage drops in the contacts, and thus is not a true measure of the mobility. For extracting the field-effect mobility, it is essential to form ohmic contacts. We show in the next section that such contacts are possible in Ti/In/Ag–WSe<sub>2</sub> FETs. From this study, we find that Al forms high-resistance Schottky contacts, contrary to what one would conclude from work-function argument alone. Thus, a more careful analysis of the problem can help design lower resistance contacts. Hence, it is necessary to analyze the physics of the metal–semiconductor interface to explore how metals influence the electronic structure of monolayer WSe<sub>2</sub>. Ab initio density

functional theory (DFT) calculations were employed to simulate the Al–WSe<sub>2</sub> system in a similar spirit as earlier studies in related TMD materials.<sup>17,24</sup>

For comparison with the Al–WSe<sub>2</sub> system, an Ag–WSe<sub>2</sub> system was also simulated in the same manner. Figure 4a,g shows side views of the relaxed contact regions (which have the lowest energy) at the interface between monolayer WSe<sub>2</sub> with Al(111) and Ag(111), respectively. These optimized interface structures are calculated using the commercial tool ATK.<sup>18</sup> Partial density of states (PDOS) projections onto selected W and Se orbitals for monolayer WSe<sub>2</sub> (Figure 4b) were calculated based on the structure shown in Figure 4a,g. As shown in Figure 4b (top), there are almost no states near the Fermi level of monolayer WSe<sub>2</sub>, indicating the intrinsic electronic property of undoped monolayer WSe<sub>2</sub>. However, after depositing Al or Ag onto monolayer WSe<sub>2</sub>, the  $E_F$  moves toward the conduction band (Figure 4b, middle and bottom) exhibiting that WSe<sub>2</sub> is n-doped by Al and Ag. However, compared to the Ag–WSe<sub>2</sub> system, the PDOS of Al–WSe<sub>2</sub> near  $E_F$  is much smaller, indicating that Al has weaker capability to dope monolayer WSe<sub>2</sub>, thereby leading to larger contact resistance.

The capability of metal doping of WSe<sub>2</sub> can also be gauged by observing the electron density at the metal–WSe<sub>2</sub> interface. The Al–WSe<sub>2</sub> contact region (in Figure 4d) has an electron density less than 0.01 Å<sup>-3</sup> as shown in Figure 4e, while Ag–WSe<sub>2</sub> (Figure 4i) has an electron density greater than 0.01 Å<sup>-3</sup>



**Figure 5.** Transfer characteristics of back-gated monolayer WSe<sub>2</sub> FETs with (a) Ti (10 nm)/Au (100 nm), (c) In (10 nm)/Au (100 nm), and (e) Ag (10 nm)/Au (100 nm). (b,d,f) Corresponding  $I_{ds}$ - $V_{ds}$  curve from device (a,c,e), respectively. Device sizes (length/width) are (a) 1  $\mu\text{m}/3 \mu\text{m}$ , (c) 3.5  $\mu\text{m}/3 \mu\text{m}$ , and (e) 1.5  $\mu\text{m}/1 \mu\text{m}$ .

as shown in Figure 4j. Compared to Ag-WSe<sub>2</sub> (electron configuration of Ag, [Kr] 5s<sup>1</sup> 4d<sup>10</sup>), the low electron density of Al-WSe<sub>2</sub> interface can be attributed to the lack of d-orbitals in Al (electron configuration of Al, [Ne] 3s<sup>2</sup> 3p<sup>1</sup>) leading to a small overlap of electronic orbitals with WSe<sub>2</sub>. The conduction band-edge states of single-layer TMD crystals derive primarily from the metal (W) d-orbitals. It is believed that d-orbitals in the contact metal Ag can hybridize with the d-orbitals in Se and W resulting in better electron injection, thereby forming lower contact resistance.<sup>17,24</sup> This d-orbital overlap is confirmed by plotting the electronic dispersion of WSe<sub>2</sub> with Ag as well as the PDOS of d-orbitals in Ag with the d-orbitals of W atoms, which are shown in the Supporting Information Figure S2. Ag-WSe<sub>2</sub> also has a smaller electron tunneling barrier (Figure 4k, 0.16 eV) compared to that of the Al-WSe<sub>2</sub> (Figure 4f, 0.6 eV), indicating that Ag-WSe<sub>2</sub> can form a better contact than Al-WSe<sub>2</sub>. The experimental study of Al/Ag contacts with WSe<sub>2</sub> and the complementary first-principles modeling study point toward the hypothesis that metals with d-orbitals (such as In, Ag and Ti) can help in forming ohmic contacts to monolayer WSe<sub>2</sub>. This hypothesis is confirmed by our experimental results as shown in the next section.

WSe<sub>2</sub> FET devices were fabricated with In, Ag, and Ti using the same process described in the previous section. Figure 5a,c,e shows the transfer curves of the back-gated WSe<sub>2</sub> FETs with Ti (10 nm)/Au (100 nm), In (10 nm)/Au (100 nm), and Ag (10 nm)/Au (100 nm) contacts, respectively. They clearly display n-type<sup>25</sup> behavior with large ON/OFF ratios exceeding 10<sup>6</sup>. It is worth noting that small hole currents (3–5 orders lower than electron current) at high negative voltages were observed on monolayer WSe<sub>2</sub> FETs as shown in Figure 5a,c,e. This phenomenon is explained in the Supporting Information Figure S3. The field-effect mobility of WSe<sub>2</sub> FET (Figure 5a) with Ti contact extracted without the contact corrections is in the range of 0.01–2 cm<sup>2</sup>/V·s, similar to the extracted mobility of MoS<sub>2</sub> with Ti contact FET (back gate device).<sup>8</sup> However, the current drives of WSe<sub>2</sub> FETs were significantly improved using In and Ag contacts as shown in Figure 5c,e, which is a result of low contact resistance. The contacts for all three metals Ti, In, and Ag were ohmic and quite distinct from the Schottky

contacts observed in case of Al. For the In-WSe<sub>2</sub> device, the ON-current is around 210  $\mu\text{A}/\mu\text{m}$  for  $V_{bg} = 30 \text{ V}$  and  $V_{ds} = 3 \text{ V}$  as shown in Figure 5d.

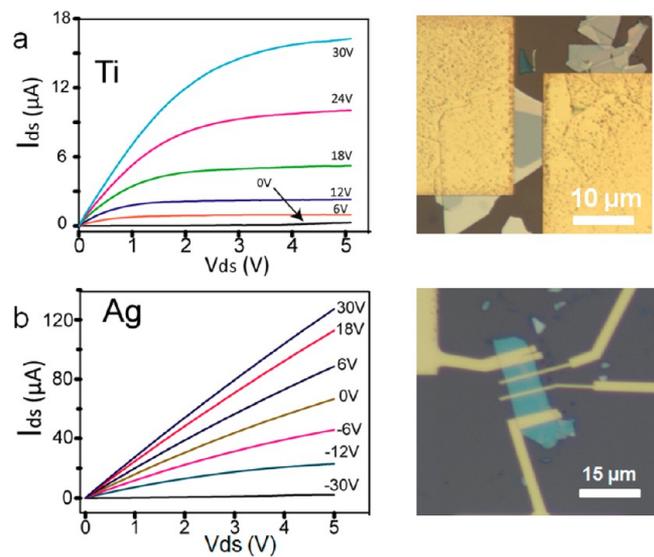
However, the ON current did not saturate even at  $V_{bg} = 30 \text{ V}$  and  $V_{ds} = 3 \text{ V}$ , indicating higher ON currents are possible. This value is even larger than the record ON-current of top-gated monolayer MoS<sub>2</sub> FET<sup>26</sup> ( $I_{ON} = 172 \mu\text{A}/\mu\text{m}$  for  $V_{tg} = 6 \text{ V}$  and  $V_{ds} = 3 \text{ V}$ ). This high ON current corresponds to a current density of  $3.25 \times 10^7 \text{ A}/\text{cm}^2$ , which is about 50–60 times larger than the maximum sustainable current density of copper interconnects employed in nanoscale integrated circuits,<sup>27</sup> and only about an order of magnitude below that of graphene.<sup>28</sup> As shown in Figure 5d, the  $I_{ds}$ - $V_{ds}$  curve of the same FET shows a linear behavior, which has commonly been observed on monolayer and bilayer MoS<sub>2</sub> FETs.<sup>29</sup> The linear behavior of  $I_{ds}$ - $V_{ds}$  curve of In-WSe<sub>2</sub> FET indicates that In-WSe<sub>2</sub> contact is ohmic in nature.

The field-effect (electron) mobility extracted without contact corrections for the In-WSe<sub>2</sub> (monolayer) FET is 142 cm<sup>2</sup>/V·s, which is due to the small contact resistance as well as the high- $\kappa$  dielectric substrate (Al<sub>2</sub>O<sub>3</sub>). This electron mobility value (142 cm<sup>2</sup>/V·s) of monolayer WSe<sub>2</sub> is comparable to that of the bulk WSe<sub>2</sub> (100 cm<sup>2</sup>/V·s) measured on two-terminal back gated FET device<sup>15</sup> and the hole mobility in NO<sub>2</sub>-doped p-type monolayer back-gated WSe<sub>2</sub> FETs (140 cm<sup>2</sup>/V·s), measured with Pd as the contact.<sup>16</sup> A good contact material should have a high electrical conductivity and must simultaneously be chemically and thermally stable. Though In exhibits low contact resistance with WSe<sub>2</sub>, it has a poor adhesion with the substrate as well as a low melting point (156 °C), which may limit its usage as a contact metal. Thus, it is desirable to explore other d-orbital contact metals, which possess additional process robustness.

As shown by atomistic simulations in Figure 4b, Ag can significantly dope WSe<sub>2</sub> with electrons due to the d-orbital mixing. Thereby, Ag is expected to form a low resistance ohmic contact with WSe<sub>2</sub>. Figure 5e shows the transfer curve of an Ag-WSe<sub>2</sub> FET device. The linear behavior of the output curve of Ag-WSe<sub>2</sub> FET in Figure 5f indicates that Ag forms an ohmic contact with WSe<sub>2</sub>. The extracted uncorrected field-effect

mobility of this device is in the range of 16–44  $\text{cm}^2/\text{V}\cdot\text{s}$ , which is higher than that of the Ti–WSe<sub>2</sub> FET devices. The ON current of Ag–WSe<sub>2</sub> FET is 2–4 times less than that of the In–WSe<sub>2</sub> FET due to the higher contact resistance. However, the ON/OFF ratio of the Ag–WSe<sub>2</sub> FET is greater than 10<sup>8</sup>. Hence, since Ag has a better thermal stability and adhesion with the substrate, Ag–WSe<sub>2</sub> FETs could also be useful in future 2D electronics based on WSe<sub>2</sub>. The mobility of Ag–WSe<sub>2</sub> FET can be further enhanced by the deposition of high- $\kappa$  dielectric on top of the WSe<sub>2</sub> to suppress Coulomb scattering as shown in the next section (Figure 7a). The lowest subthreshold swing (SS) of our measured back-gated Ag–WSe<sub>2</sub> FET is around 300 mV/dec. Although the SS is higher than the state-of-the-art top-gated monolayer MoS<sub>2</sub> FET,<sup>8</sup> it can be reduced by decreasing the thickness of the back gate dielectric film (Al<sub>2</sub>O<sub>3</sub> thickness is 72 nm in this work) or by fabricating top-gated WSe<sub>2</sub> FET with a thin high- $\kappa$  dielectric film. We attribute the high SS to defects/traps in the ALD layer and/or in the Si/ALD interface, it is not indicative of the TMD layer itself.

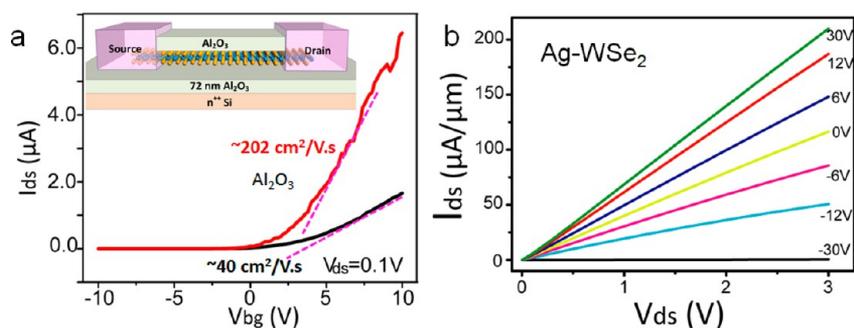
It is to be noted that while we have not observed current saturation on back-gated monolayer WSe<sub>2</sub> FET with In contact (Figure 5d) and only slight saturation in the case of Ag contact (Figure 5f), the  $I_{\text{ds}}-V_{\text{ds}}$  curve of Ti–WSe<sub>2</sub> FET (Figure 5b) shows a robust current saturation. Thus, this phenomenon indicates that the current saturation of monolayer WSe<sub>2</sub> back-gated FET device can be significantly influenced by the contact metal. It is highly desirable to study the mechanism of current saturation of monolayer WSe<sub>2</sub> since it is an important attribute for digital circuit applications. Using the method described by Kim,<sup>30</sup> the contact resistance can be roughly estimated at high positive gate biases in the linear region of the  $I_{\text{ds}}-V_{\text{ds}}$  curves. The contact resistance of the Ti–WSe<sub>2</sub>, In–WSe<sub>2</sub>, and Ag–WSe<sub>2</sub> FET are found to be  $3.6 \times 10^7$ ,  $7.5 \times 10^3$ , and  $1.5 \times 10^4$   $\Omega\cdot\mu\text{m}$ , respectively. Because of the parasitic series source/drain contact resistance ( $R_{\text{C}}$ ), the effective  $V_{\text{gs}}$  and  $V_{\text{ds}}$  are lowered and are given by  $V_{\text{gs, eff}} = V_{\text{gs}} - R_{\text{C}}I_{\text{ds}}$  and  $V_{\text{ds, eff}} = V_{\text{ds}} - 2R_{\text{C}}I_{\text{ds}}$ . Also, it can be observed from Figure 5a,c,e that the contact can significantly modulate the threshold voltage ( $V_{\text{t}}$ ) of the FETs. From Figure 5c, the  $V_{\text{t}}$  in the case of In is extracted to be  $-7$  V. Because of this negative  $V_{\text{t}}$ ,  $V_{\text{gs, eff}} - V_{\text{t}}$  for the case of In becomes greater than  $V_{\text{ds, eff}}$  and hence the device operates in the linear region. This explains the absence of saturation for  $I_{\text{ds}}-V_{\text{ds}}$  curves in case of In contact. The saturation mechanism in the case of Ti, which has the highest contact resistance out of the three metals, can be explained as follows. The very high value of  $R_{\text{C}}$  for Ti contact leads to much reduction in  $V_{\text{gs, eff}}$  and hence to an increase in the effective threshold voltage. This is clear from the  $I_{\text{ds}}-V_{\text{gs}}$  plots in Figure 5a,c as well as the transconductance ( $g_{\text{m}}$ ) plots in Figure S4 in the Supporting Information, as it is observed that while the maximum slope of  $I_{\text{ds}}-V_{\text{gs}}$  curve for In occurs at around  $-2.5$  V, the maximum slope for Ti is not reached even at  $V_{\text{gs}}$  of 20 V indicating very high threshold voltage for devices with Ti contact, thereby pushing the device to operate in the subthreshold region. In the subthreshold region of long-channel transistors, current has a weak dependence on the drain voltage and saturates for higher  $V_{\text{ds}}$  as is observed from the simulated  $I_{\text{ds}}-V_{\text{ds}}$  characteristics of a generic FET, taking into account the contact resistances (Figure S5 in Supporting Information). Both  $R_{\text{C}}$  and  $V_{\text{t}}$  in the case of Ag is lower than those in case of Ti. Hence, it shows only a slight saturation at higher  $V_{\text{ds}}$ . This contact dependent current saturation behavior has also been found in multilayer WSe<sub>2</sub> FETs as shown in Figure 6. With Ti contact (Figure 6a),



**Figure 6.** (a)  $I_{\text{ds}}-V_{\text{ds}}$  curves of a multilayer WSe<sub>2</sub> FET with Ti (20 nm)/Au (100 nm) contact. Picture on the right shows corresponding optical microscope image of a fabricated FET. The thickness of the multilayer WSe<sub>2</sub> is  $\sim 20$ –40 nm. (b)  $I_{\text{ds}}-V_{\text{ds}}$  curves of a multilayer WSe<sub>2</sub> FET with Ag (20 nm)/Au (100 nm) contact. Picture on the right shows the corresponding optical microscope image of the fabricated FET. The thickness of the multilayer WSe<sub>2</sub> is  $\sim 10$  nm. Device sizes (length/width) are  $7 \mu\text{m}/12 \mu\text{m}$  in (a), and  $6 \mu\text{m}/11 \mu\text{m}$  in (b) (measured between the inner two narrow electrodes shown in the optical micrograph in (b)), respectively.

the current exhibits saturation while the  $I_{\text{ds}}-V_{\text{ds}}$  curves of multilayer Ag–WSe<sub>2</sub> FET (Figure 6b) show a linear behavior with much higher ON current than that of Ti–WSe<sub>2</sub> FET (Figure 6a). The contact resistances of the Ti and Ag with multilayer WSe<sub>2</sub> FETs are estimated to be  $7 \times 10^5$  and  $6.5 \times 10^3$   $\Omega\cdot\mu\text{m}$ , respectively, which are around 1 order of magnitude smaller than the respective contact resistances of Ti and Ag with monolayer WSe<sub>2</sub> FETs.

We can now summarize our current understanding of the role of metal contacts in forming high-performance WSe<sub>2</sub> FETs as follows. Our previous theoretical work has already revealed the principles for making ideal contacts with TMDs.<sup>17</sup> First of all, it is desirable to have a metal with small work function to form a zero or negative Schottky barrier with TMDs, which is also important for achieving good contact between metals with bulk semiconductors.<sup>31</sup> Second, it requires a sufficient strength of orbital overlap (especially on d-orbitals) between metals and TMDs to form small interlayer distance, thereby leading to a zero tunnel barrier at the interface. Those principles were proved by our experimental demonstration in this study. Combining the results from the above studies such as band alignments of WSe<sub>2</sub> with contact metals (Figure 3a), DFT calculations (Figure 4) and device measurements (Figure 5), we can draw the conclusion that a contact metal with d-orbital and small work function (such as In whose work function is closest to the electron affinity of monolayer WSe<sub>2</sub>) can help in forming good n-type contacts to monolayer WSe<sub>2</sub>. However, the contact resistance between In and WSe<sub>2</sub> is still large (around  $7.5 \times 10^3$   $\Omega\cdot\mu\text{m}$ ) compared to silicon and III–V FET technologies, which consequently limits the performance of the WSe<sub>2</sub> devices. Hence, it is necessary to explore other techniques such as doping the source/drain regions to further



**Figure 7.** (a) Transfer characteristics of back-gated WSe<sub>2</sub> FETs with Ag (10 nm)/Au (100 nm) contact. The black curve corresponds to “before Al<sub>2</sub>O<sub>3</sub> deposition” and the red curve corresponds to “after Al<sub>2</sub>O<sub>3</sub> deposition”.  $V_{ds} = 0.1$  V. This device has a length and width of 1.5 and 1  $\mu\text{m}$ , respectively. After deposition of Al<sub>2</sub>O<sub>3</sub> on top of WSe<sub>2</sub>, the mobility of WSe<sub>2</sub> FET is increased by  $\sim 6$  times. (b) Corresponding  $I_{ds}$ – $V_{ds}$  curve of Ag–WSe<sub>2</sub> FET after ALD process.

reduce the contact resistance to open up the intrinsic device performance.

It has been demonstrated that the carrier mobility of monolayer TMD materials can be enhanced by depositing high- $\kappa$  dielectric films with certain thickness and dielectric constant (larger than that of the semiconductor).<sup>8,9,16,26</sup> The high- $\kappa$  environment is believed to suppress Coulomb scattering in 2D semiconductors by dielectric screening.<sup>32,33</sup> Hence, a high- $\kappa$  dielectric film was deposited on monolayer WSe<sub>2</sub> by ALD to explore its effect on the electrical property of WSe<sub>2</sub> FET. First, a 1 nm Ti seed layer was deposited (in the form of nanoparticles, and Ti oxidizes into TiO<sub>2</sub> with a dielectric constant of  $\sim 40$ –85 when exposed to air) onto WSe<sub>2</sub> to assist in the formation of nucleation centers for the subsequent high- $\kappa$  film because there are no dangling bonds on the WSe<sub>2</sub> surface. Subsequently, the sample was loaded into an ALD system for dielectric film deposition. We have observed that HfO<sub>2</sub> is not compatible with monolayer WSe<sub>2</sub>. HfO<sub>2</sub> films (25 nm) were deposited on the WSe<sub>2</sub> at 200, 150, and 120  $^{\circ}\text{C}$  by ALD, respectively. However, after HfO<sub>2</sub> deposition, the current drives of monolayer WSe<sub>2</sub> FET device were significantly decreased and only multilayer WSe<sub>2</sub> FET devices exhibited gate modulation. We also noticed that monolayer WSe<sub>2</sub> tends to degrade when its temperature is above 127  $^{\circ}\text{C}$  as shown in the Supporting Information (Figure S6), indicating that the passivation process (such as high- $\kappa$  dielectric film deposition) should be performed below 127  $^{\circ}\text{C}$ .

Compared to HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> deposited at 120  $^{\circ}\text{C}$  was found to be compatible with WSe<sub>2</sub> with 1 nm Ti seed layer on top. Figure 7a shows the transfer characteristics for back gated FETs with Ag (10 nm)/Au (100 nm) contact. After Al<sub>2</sub>O<sub>3</sub> deposition on top of WSe<sub>2</sub>, the mobility increased by 5–6 times (mobility numbers indicated inside Figure 7a were estimated from the transconductance (slopes of purple dash lines) values extracted from the  $I_{ds}$ – $V_{bg}$  curves in Figure 7a) compared with that of the original device and the electron mobility of monolayer WSe<sub>2</sub> FET increased to around 202  $\text{cm}^2/\text{V}\cdot\text{s}$ , which is comparable to that of back gated-MoS<sub>2</sub> FET with HfO<sub>2</sub> film on top<sup>8</sup> and to that of top-gated p-type monolayer WSe<sub>2</sub> FET with ZrO<sub>2</sub> on top.<sup>16</sup> After deposition of Al<sub>2</sub>O<sub>3</sub> on WSe<sub>2</sub>, the ON-current of Ag–WSe<sub>2</sub> FET (Figure 7b) reached around 205  $\mu\text{A}/\mu\text{m}$  for  $V_{bg} = 30$  V and  $V_{ds} = 3$  V. This ON current is comparable with that of the record ON current in In–WSe<sub>2</sub> FET discussed earlier.

Before Al<sub>2</sub>O<sub>3</sub> deposition, the monolayer WSe<sub>2</sub> FET was annealed at 120  $^{\circ}\text{C}$  for 12 h (same temperature as in the ALD process) to improve the contact and remove any absorbed

molecules. Hence, the increase of mobility in WSe<sub>2</sub> FET can be attributed to the Al<sub>2</sub>O<sub>3</sub> environment. However, Al<sub>2</sub>O<sub>3</sub> can only increase the mobility of monolayer WSe<sub>2</sub> by around 5–6 times (for our best case), which is much smaller than the reported impact of HfO<sub>2</sub> in MoS<sub>2</sub> FETs (at least over 12 $\times$  increase in mobility).<sup>8,34</sup> One possible reason for the apparent improvement in mobility could be because Al<sub>2</sub>O<sub>3</sub> has lower dielectric constant than HfO<sub>2</sub>, and the scattering time (and hence the mobility) goes as the square of the dielectric constant.<sup>33</sup> Although the high- $\kappa$  dielectric can enhance the mobility of monolayer TMD materials by reducing the Coulomb scattering, there are upper limits on the maximum achievable mobilities (for example, monolayer n-type MoS<sub>2</sub> has a maximum mobility of  $\sim 410$   $\text{cm}^2/\text{V}\cdot\text{s}$  predicted by theoretical calculation<sup>35</sup>). In addition, we also observed large variations in the effect of Al<sub>2</sub>O<sub>3</sub> film deposition on the mobility of WSe<sub>2</sub> FETs. Thus, it is desirable to understand the mobility boosting mechanism in monolayer TMD materials due to high- $\kappa$  dielectrics and identify the best high- $\kappa$  environment for WSe<sub>2</sub>.

In summary, WSe<sub>2</sub> based devices were fabricated, which exhibit the highest reported current. The high current is due to the improved understanding of the nature of metal contacts to WSe<sub>2</sub>. Device measurements supported by ab initio density functional theory (DFT) calculations exhibit that d-orbital of contact metal plays a key role in forming low contact resistance with monolayer WSe<sub>2</sub>. Devices fabricated with In, Ag, Al, and Ti as metal contacts were characterized. The In- and Ag-based contacts exhibit the smallest contact resistance and the highest drive current, which is in agreement with the DFT calculations. With In as the contact metal, monolayer WSe<sub>2</sub> FET exhibits a record ON-current of 210  $\mu\text{A}/\mu\text{m}$  (at  $V_{ds} = 3$  V), which is the highest ON-current achieved on any monolayer TMD FET to date. In–WSe<sub>2</sub> FET also shows a high electron mobility of 142  $\text{cm}^2/\text{V}\cdot\text{s}$ , which is the best mobility achieved on any back gated monolayer TMD-based FET to date. By Al<sub>2</sub>O<sub>3</sub> film deposition on WSe<sub>2</sub>, the mobility of monolayer WSe<sub>2</sub> FET with Ag contact can reach around 202  $\text{cm}^2/\text{V}\cdot\text{s}$  (with ON-current of 205  $\mu\text{A}/\mu\text{m}$  at  $V_{ds} = 3$  V), due to the high- $\kappa$  environment. Therefore, we have highlighted the importance of understanding the nature of metal contacts to 2D semiconductor materials in general for designing high-performance FETs and have demonstrated the efficacy of our contact evaluation methodology in designing n-type monolayer WSe<sub>2</sub> FETs with record ON currents. Together with the recently reported p-type monolayer WSe<sub>2</sub> FET, this demonstration of a high-performance n-type monolayer WSe<sub>2</sub>

FET presents new opportunities in the area of digital electronics.

## ■ ASSOCIATED CONTENT

### 📄 Supporting Information

Effect of annealing on the device characteristics of Ti–WSe<sub>2</sub>, detailed information of DFT calculations, electronic dispersion of WSe<sub>2</sub> and Ag–WSe<sub>2</sub> system, schematic of energy bands of metal–WSe<sub>2</sub> junction, transconductance of WSe<sub>2</sub> FETs, simulation of device characteristics of an FET with high contact resistance, effect of annealing on the  $I_{ds}$ – $V_{bg}$  characteristics of Ti–WSe<sub>2</sub> FET at 473 K. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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### Author Contributions

The manuscript was written through contributions from all authors. All authors have given approval to the final version of the manuscript.

### Notes

The authors declare no competing financial interest.

## ■ ACKNOWLEDGMENTS

This work was supported in part by the National Science Foundation under Grant CCF-1162633.

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