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On the possibility of sub-60 mV/decade subthreshold switching in piezoelectric gate barrier transistors

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A novel method for the reduction of subthreshold slope below the room-temperature Boltzmann limit of 60 mV/dec for a field-effect transistor based on negative differential capacitance is proposed. This effect uses electric field induced electrostriction of a piezoelectric gate barrier of the transistor. The mechanism amplifies the internal surface potential over the applied gate voltage. This internal voltage gain mechanism provides an opportunity for steep subthreshold slope switching below 60 mV/decade of the transistor current.

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1 Introduction The demand for integrated circuits in portable electronic applications requires energy-efficient low-power transistors. Scaling of field-effect transistors (FETs) has improved the device performance as measured by the switching speed and power consumption. It has sustained higher packing densities in integrated circuits (ICs) for many decades. Further scaling of transistor technology is increasingly stalled by the heat generated in logic switching, and the resulting high power dissipation density in ICs [1, 2].

The root of this problem lies in the inability to reduce the operating voltage of transistors. The operating voltage has not scaled in direct proportion with the feature size because of the need to maintain a minimal on/off ratio of the current of the transistor [1, 2]. The subthreshold slope (SS), expressed in mV/decade is the gate voltage required to change the drain current by an order of magnitude [2-4]. This is limited to SS=kTln(10)~60 mV/dec at room temperature in a traditional FET [3]. Thus, to clearly distinguish between the on and off states in a logic operation, a few orders of magnitude is required, which sets a minimum voltage requirement. If a means to lower the operating voltage is found while still allowing a large on/off ratio, the energy dissipation can be reduced.

A possible approach suggested that it might be possible to realize a negative differential capacitance (NDC) using a ferroelectric material as a gate insulator of a FET [4]. How does this change to the conventional passive gate insulator achieve a sub-60 mV/decade SS? A ferroelectric material has a regime of charge-vs-voltage behavior that when converted to a capacitance-vs-voltage curve, exhibits a negative differential capacitance (NDC). The physical origin of this behavior is the internal polarization in the ferroelectric. The collective alignment of the microscopic electric dipoles can amplify the gate potential that makes across the layer to the semiconductor channel. In circuit terms, this acts as a negative capacitance, which in series with the semiconductor capacitance leads to a larger capacitance [4]. A larger capacitance leads to a lower voltage requirement to create the same charge than a conventional FET with passive gate dielectrics. By implementing the negative differential capacitance in the gate region of an FET, it is then possible to amplify the internal channel potential, ψ_s (i.e. surface potential) induced by the applied gate voltage, V_g. This results in a reduction of subthreshold slope (SS) factor, $m = \partial V_g / \partial \psi_s < 1$, and hence the subthreshold slope (SS=m × 60 mV/dec) can be lowered than 60 mV/dec [4]. This was the basis of the proposal for ferroelectric gate dielectrics. A natural question is – are other active dielectric properties feasible for achieving NDC?

In this paper, we propose a novel method for realizing NDC by using a piezoelectric gate dielectric. A piezoelectric gate dielectric is technologically available today in III Nitride and ZnO-based heterostructure transistors, and will only become more available with the increasing interest in

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oxide heterostructures. How will a piezoelectric gate dielectric lead to a NDC?

Electrostriction is an electric field-induced reduction in the thickness of a dielectric – it is well studied, and robust. A brief description of the process is provided. The electrostatic attractive force between the opposite charges at the surfaces of a piezoelectric layer induces a compressive stress in the layer. Note that this property exists in a non-piezoelectric dielectric too, in a piezoelectric layer this strength is significantly amplified. The Coulomb attraction between the charges reduces the thickness of a layer and the strain creates more charge. This sets up a positive feedback between the thickness and the electric field through the change of polarization. This mechanism is responsible for the NDC in the piezoelectric layer. In the rest of this work, we quantify this qualitative idea in the III-nitride AlN/GaN heterostructure platform.

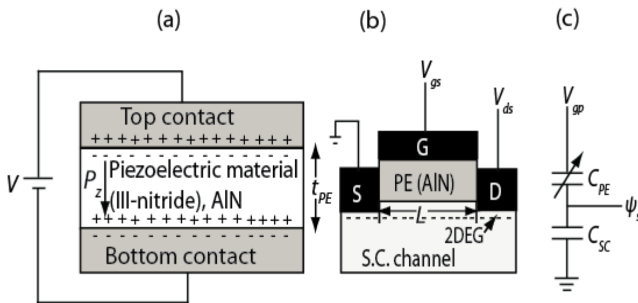

Figure 1 (a) Schematic of a piezoelectric (III-nitride) AlN layer, connected to two metallic contacts, (b) cross section of a GaN channel transistor with a piezoelectric gate insulator, (c) equivalent capacitive circuit model of the transistor where C_{PE} is a negative differential capacitance in the thin PE layer (t_{PE}< 5 nm), and C_{sc} is the semiconductor capacitance in the channel.

2 Device structure and negative differential capacitance (NDC)

Figure 1(a) depicts the schematic cross section of a piezoelectric AlN layer connected to two metallic electrodes. A voltage V is applied across this layer. The electrostatic force from the opposite charges at the surfaces of layer induces a compressive stress, reducing its thickness. Since the voltage is clamped, the internal electric field is amplified because the thickness is lower. The compressive stress along the thickness direction of the layer can be expressed as a quadratic relation of internal electric field or polarization [5-7, 10]. Based on the electromechanical coupling, the free energy density of the layer is [8, 9],

$$H = \tfrac{1}{2} C_{ijkl}\gamma_{ij}\gamma_{kl} - \tfrac{1}{2}\varepsilon_{ij}E_iE_j - e_{ijk}E_i\gamma_{jk} - E_i^{\text{ext}}P_i \ , \tag{1}$$

where C_{ijkl} is the elastic constant in tensor form, ε_{ij} is the dielectric constant, e_{ijk} is the piezoelectric constant of the material, and γ_{ij} and γ_{jk} are the strain components. E_i and E_j are the internal electric field in the layer, and P_i (in units of C/m^2) is the polarization due to the field-induced deformation in the piezoelectric layer. The indices *i, j, k,* and *l* run over the Cartesian coordinates *x*, *y*, and *z*. The first term in Eq. (1) is the internal stored elastic potential energy. The second and third terms are the electrostatic and electromechanical coupling energy terms due to internal electric fields and strain respectively. The fourth term is due to the energy contribution from the interaction of the external electric field E_i^{ext} and the internal polarization P_i in the material. Using the Voigt notation [10], we expand Eq. (1) along the thickness direction i.e. in the out-of plane z-direction [0001] direction of the wurtzite crystal, the change in the internal energy density in an isotropic piezoelectric material is

$$H = \tfrac{1}{2} C_{33}\gamma_{33}^2 - \tfrac{1}{2}\varepsilon_{33}E_z^2 - e_{33}E_z\gamma_{33} - E_{\text{ext}}P_z \ , \tag{2}$$

where e_{33} is the piezoelectric coefficient of the material along the *z*-direction, C_{33} and ε_{33} are the elastic and dielectric constant of the piezoelectric material along the *z*-direction. Considering the electrostatic force in the *z*-direction, the compressive strain is then $\gamma_{zz}= -P_z^2/(C_{33}\,\varepsilon_{33})$ [9], where the polarization P_z is related to the internal electric field E_z by $E_z= P_z/\varepsilon_{33}$. By substituting these relations into Eq. (2) and evaluating, the free energy density change in Eq. (2) due to external electric field, $E_{ext} = V/t_{PE}$ becomes

$$H_{PE} = \frac{1}{2}\frac{P_z^4}{C_{33}\varepsilon_{33}^2} - \frac{1}{2}\frac{P_z^2}{\varepsilon_{33}} - \frac{e_{33}P_z^3}{C_{33}\varepsilon_{33}^2} - E_{\text{ext}}P_z \ . \tag{3}$$

To calculate the polarization-induced charge density $P_z \sim \sigma_P$ at the interface between the barrier and the semiconductor, the free energy density should be minimized with respect to P_z in Eq. (3) in order to stabilize the whole system. By using the condition $dH_{PE}/dP_z = 0$, and substituting $E_{ext}=V/t_{PE}$ in Eq. (3), the equation for charge density ($P_z \sim \sigma_P$) is evaluated to

$$\left(\frac{2t_{PE}}{C_{33}\varepsilon_{33}^2}\right)\cdot\sigma_P^3 + \left(\frac{3e_{33}t_{PE}}{C_{33}\varepsilon_{33}^2}\right)\cdot\sigma_P^2 - \left(\frac{t_{PE}}{\varepsilon_{33}}\right)\cdot\sigma_P - V = 0. \tag{4}$$

The capacitance of the piezoelectric layer is $C_{PE}=d\sigma_P/dV$, where the charge density σ_P is obtained by solving the nonlinear Eq. (4). To obtain the sheet charge density at interface, we choose the AlN material parameters C_{33} = 373 GPa and $\varepsilon_{33} = 9\,\varepsilon_0$ with $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, e_{33} =1.55 C/m^2 [11]. The capacitance per unit area is plotted with the applied voltage V in Fig. 2. At V=0 V, the capacitance of the piezoelectric layer is then the geometric capacitance $C_{geo} = \varepsilon_{33}/t_{PE} = (9\times 8.85\times10^{-12})/(1\times10^{-9}) = 0.0796$ F/m^2 for t_{PE} =1 nm. The calculated result highlights the intuitive picture: it shows a negative differential capacitance, as the capacitance of the piezoelectric layer *decreases* with increasing applied voltage. This NDC behavior in piezoelectric AlN has already been observed in experiments (see Ref. [12]).

Can we use this effect for steep subthreshold slope transistor design? In the following section, we investigate the use of the thin piezoelectric layer as the active gate barrier of the transistor and show an amplified surface potential and a steep subthreshold slope.

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3 Surface potential and steep subthreshold slope

Figures 1(b) and (c) illustrate the cross section of the FET with the piezoelectric gate, and the equivalent capacitive circuit for calculation of surface potential ψ_s for the transistor. The capacitive circuit consists of a series connection of the barrier capacitance C_{PE} in the piezoelectric layer, and the semiconductor capacitance C_{sc} in the channel. For this series connection, the total charge density σ_P induced in the semiconductor channel can be written as $\sigma_P = C_{sc}\psi_s$, where ψ_s appears across the semiconductor channel with capacitance C_{sc} [4]. The rest of the voltage, $V_{gp} - \psi_s$, appears across the piezoelectric barrier layer, AlN. Here, V_{gp} is the effective gate voltage ($V_{gs} - V_p$), with V_p is the pinch-off or the threshold voltage of the transistor [13]. By substituting $\sigma_P = C_{sc}\psi_s$ and $V = V_{gp} - \psi_s$ in Eq. (4), the surface potential at the semiconductor channel is expressed in the following non-linear equation:

$$\left(\frac{2t_{PE}C_{sc}^3}{C_{33}\varepsilon_{33}^2}\right)\cdot\psi_s^3 + \left(\frac{3e_{33}t_{PE}C_{sc}^2}{C_{33}\varepsilon_{33}^2}\right)\cdot\psi_s^2 - \left(\frac{t_{PE}C_{sc}}{\varepsilon_{33}}\right)\cdot\psi_s - (V_{gp} - \psi_s) = 0. \quad (5)$$

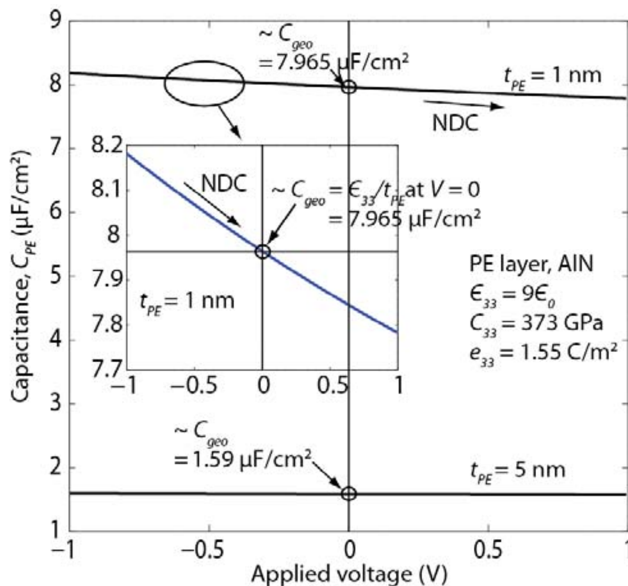

Figure 2 The calculated capacitance of the nanoscale piezoelectric layer (AlN) as a function of an applied voltage between two metallic contacts, for the thickness of the layer, t_{PE} =1 nm and 5 nm. Inset of figure shows a rescaled plot of the negative differential capacitance (NDC) for t_{PE}=1 nm.

The surface potential is calculated by solving Eq. (5) with the material parameters for AlN and GaN, and is plotted as a function of effective gate voltage V_{gp}, in Fig. 3. The result shows the amplification of the surface potential relative to the applied gate voltage (i.e. $\Delta\psi_s > \Delta V_{gp}$) due to NDC gate barrier integrated with the conducting channel of the semiconductor. A value of $C_{sc} = 0.01$ F/m^2 is used to show the internal voltage gain for $t_{PE} = 1$ nm in Fig. 3. The value of C_{sc} used here is 10X lower than the extracted value from experimental results [4]. For a GaN channel, the total semiconductor capacitance C_{sc} is a series connection of the quantum and 2DEG centroid capacitance. The quantum capacitance $C_q = q^2 \times m^*/(\pi\hbar^2) = 0.13$ F/m^2. The 2DEG centroid capacitance $C_{cent} = \varepsilon_{33}/\langle t_{cent}\rangle$, where $\langle t_{cent}\rangle$ is the centroid of the 2DEG penetration in the GaN channel from the interface ~ 1-3 nm [14, 15]. So, C_{cent} = 0.025 F/m^2. The semiconductor capacitance is then $C_{sc} = C_qC_{cent}/(C_q + C_{cent})$ = 0.03 F/m^2.

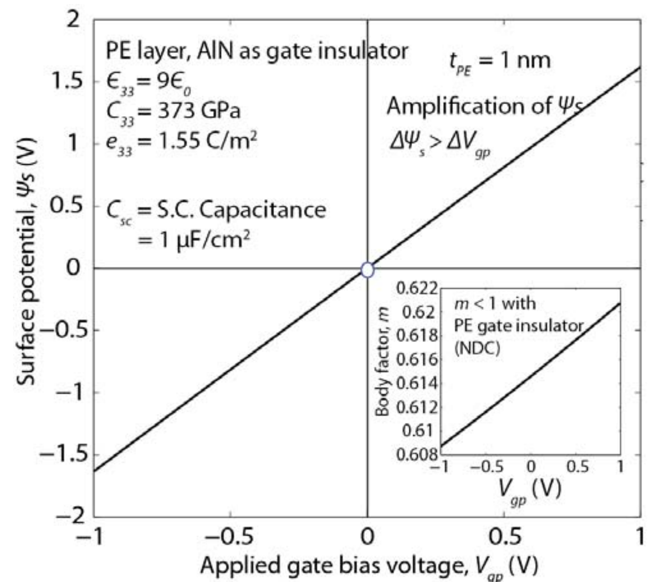

Figure 3 Amplified surface potential as a function of an effective gate voltage of the transistor. Inset of figure shows the body slope factor, m < 1, results in a steep subthreshold slope (SS < 60 mV/dec).

We also calculate the body factor, m, using Eq. (5) as shown in the inset of Fig. 3. Based on the $m < 1$, the subthreshold slope is reduced below 60 mV/dec using the relation SS = m× 60 mV/dec for FETs.

Here we discuss the impact of hysteresis in the device performance for the piezoelectric gate barrier transistor. The impact of hysteresis in the device performance using piezoelectric AlN gate barrier of the FET is negligible, since hysteresis is not present in a thin single crystal piezoelectric layer. The absence of hysteresis has been observed in many AlN/GaN high-electron-mobility transistors (HEMTs) already. The AlN gate barrier used in III-nitride GaN HEMTs is an epitaxially grown single crystal polar piezoelectric layer. Any hysteresis observed in piezoelectric materials result from defects, or polycrystalline domains. Hysteresis occurs in the polarization-vs.-electric field (P-E) in ferroelectrics and in the magnetization-vs.-magnetic field (M-H) characteristics in ferromagnets due to the formation of domains. This is a necessary consequence of the thermodynamics driven phase transition in such materials. There is no such driving force in piezoelectric materials: the strain is zero when the applied electric field is zero and thus the pie-

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zoelectric polarization-induced charge is zero at zero electric field.

We also discuss the effect of gate leakage current in thin gate barrier of the transistor. A thin gate barrier layer can result in large gate leakage currents. But AlN has a large bandgap of 6.2 eV, a dielectric constant of ~9, and a high breakdown field of > 10 MV/cm [11]. Thicker gate barriers of wider bandgap materials prevent gate leakage. Regarding thin AlN barriers, 1 nm thin AlN barriers have already been used in the fastest enhancement-mode (E-Mode) HEMTs. Experimentally, high on/off current ratios of $\sim 10^7$ and a very low leakage current $I_g \sim 10^{-7}$ A/mm in E-Mode GaN HEMT with 1 nm AlN gate barriers have been demonstrated [16]. Also using 1 nm AlN barrier, the equivalent oxide thickness (EOT) is EOT = $t_{PE} \times (\varepsilon_{SiO2}/\varepsilon_{AlN})$ = (1 nm) × (3.9/9) = 0.43 nm, which allows for excellent electrostatic control and scaling. The gate leakage current is typically exacerbated in ultrathin AlN/GaN HEMTs at very high drain voltages. However, since the NDC steep slope FET is suitable for low power switching applications, the operating drain voltage is expected to be < 1.0 V. Therefore, a ~1 nm thick barrier is sufficient for this operation regime.

Based on this study, it is feasible to attain sub-60 mV/decade using NDC in piezoelectric gated FETs. A more extensive publication will elaborate on the transistor device characteristics, its performance limitations, as well as benefits.

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