Sub-60 mV/decade Steep Transistors with Compliant Piezoelectric Gate Barriers

Raj K. Jana, Arvind Ajoy, Gregory Snider, and Debdeep Jena
Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN, 46556 USA
Email: rjana1@nd.edu

Abstract

A novel mechanism is proposed for transistors that exploits the negative differential capacitance of piezoelectric gate barriers. Electric field induced electrostriction modulates the thickness of a piezoelectric barrier. Piezoelectricity and electrostriction in a compliant piezoelectric barrier combine to provide negative differential capacitance (NDC) with internal charge amplification. The effect of the NDC in the gate capacitor of a FET is to boost the on-current, and to provide an opportunity for switching steeper than the 60 mV/decade Boltzmann limit, both highly desirable.

Introduction

Steep transistors with sub-60 mV/decade subthreshold slope are being actively pursued for ultra-low voltage and low-power nanoelectronic applications [1, 2]. Transistors with steep switching can be potentially achieved either by replacing the conventional drift-diffusion transport mechanism by interband tunneling [1, 2], or by replacing conventional passive gate dielectrics with *active* gate barrier materials such as ferroelectrics [3] and piezoelectrics [4-7]. A ferroelectric gate insulator can take advantage of negative capacitance in the gate stack to internally amplify the surface potential ψ_s induced by the applied gate voltage V_{gs}, leading to an internal voltage gain $1/m = \partial\psi_s/\partial V_{gs} > 1$ [3]. Hence the subthreshold slope SS=m×60 mV/decade can be lower than the Boltzmann limit [3]. Overcoming the subthreshold slope limit by NDC is possible because the net gate capacitance is effectively enhanced by adding a negative capacitance in series with a positive. Thus less voltage is necessary to induce the same channel charge as a conventional FET.

In this work, we first show that (a) negative differential capacitance (NDC) can potentially be achieved in a compliant *piezoelectric* gate barrier through the mechanism of electric-field-induced electrostriction [4, 5]. Then we investigate the behavior of a ballistic transistor, and show that (b) using a NDC gate stack enables higher on-currents. Finally, we discuss how one can potentially achieve sub-Boltzmann steep switching in a transistor using this NDC gate stack. We first study the behavior of an electromechanical capacitor, which is key to the problem.

Device Structure & Model Description

Fig. 1 (a) depicts the cross section of a parallel plate electromechanical capacitor. The 'dielectric' is a piezoelectric layer of dielectric constant ε_d and equilibrium thickness t_0 at V=0. What is the capacitance of the structure? We first show that the geometric capacitance $C_0 = \varepsilon_d / t_0$ is actually the low-voltage limit of a richer dependence of the charge on voltage. Application of a voltage V exerts an electromechanical pressure on the compliant piezoelectric layer, leading to a compressive strain, which reduces the thickness. The strain creates more charge at the surfaces of the piezoelectric layer: this is an internal charge amplification. The pressure exerted is $P = \sigma_m^2 / \varepsilon_d$, where σ_m is the sheet charge density on the metal. Gauss' law and linear electromechanical coupling coefficients provide the relation between the metal charge σ_m and applied voltage V:

$$C_0 V = \sigma_m - \sigma_{sp} + \left(\frac{\sigma_{sp} - e_{33}}{\varepsilon_d C_{33}}\right)\sigma_m^2 - \frac{1}{\varepsilon_d C_{33}}\sigma_m^3 + \frac{e_{33}}{(\varepsilon_d C_{33})^2}\sigma_m^4, \quad (1)$$

where C_{33} is the elastic stiffness coefficient (unit: Pascal), e_{33} is the piezoelectric coefficient (unit: C/m^2), and σ_{sp} is the charge density (unit: C/m^2) due to spontaneous polarization, if present. This unconventional dependence of charge on voltage is interpreted later; for here we note that for a non-compliant ($C_{33} \to \infty$) dielectric with no piezoelectric and spontaneous polarization ($e_{33} = \sigma_{sp} = 0$), we recover $\sigma_m = C_0 V$. We next investigate the impact of this charge-voltage dependence on a ballistic FET [Fig. 1 (b)] in the spirit of Natori's device model [8] adding the quantum contact resistances of 0.026kΩ.μm at the source and drain ends.

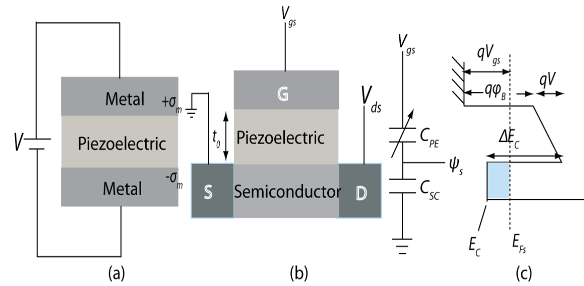

Fig. 1 – (a) A parallel-plate electromechanical capacitor with a piezoelectric (PE) barrier. (b) A piezoelectric gate transistor ("piezoFET") with a semiconductor channel and a piezoelectric gate barrier. The gate capacitance circuit is a series combination of the piezoelectric capacitance C_{PE} and the semiconductor capacitance C_{sc}. (c) The energy band diagram for the gate metal – piezoelectric - semiconductor channel stack of the transistor.

The carrier density in the semiconductor channel at the injection point induced by the gate $\sigma_m = qn_s$ is

$$qn_s = C_{SC} V_{th} \ln[1 + \exp[(E_{Fs} - E_C)/kT]], \quad (2)$$

where $C_{SC} = q^2 m^* g_s g_v / (2\pi\hbar^2)$ is the quantum capacitance, and $V_{th} = kT/q$ is the thermal voltage. From the energy band diagram in Fig 1(c), the relation between the applied V_{gs} and the voltage drop V across the piezoelectric barrier is $qV_{gs} = qV + (E_{Fs} - E_C)$. The gate-induced charge $\sigma_m = qn_s$ in the semiconductor channel is self-consistently calculated from Eqs 1 & 2. Finally, using this new dependence of charge on the voltages and the piezoelectric coefficients, the characteristic device parameters of piezoFETs are obtained from the ballistic transport model [8].

Results & Discussions

Using the model of Eq. 1, the characteristics of the electromechanical capacitor with different charge states and the resulting strain in the piezoelectric barrier are shown in Figs. 2, 3 & 4. The spontaneous polarization has been set to zero, and other parameters and indicated in these figures. At V=0 V, the piezoelectric layer is in equilibrium with no strain. The charge-voltage dependence then approaches the parallel-plate geometric capacitance $C_0 = \varepsilon_d / t_0$ shown in the green line in Fig 2. When $V > 0$, the strain in the layer increases and piezoelectricity induces higher charges as shown by the section of the $n_s - V$ curve labeled Q_2 in Fig. 2. At $V = V_{crit} <$ 1.1 V, the curve transitions into a *negative differential capacitance* branch ($Q_2 \rightarrow Q_3$ and $Q_1 \rightarrow Q_4$), where $C_{PE} = d\sigma_m / dV < 0$. This is highlighted in Figs 2 & 3, which show the flow of capacitance and strain with voltage. The resulting strain increases from ~ 4.6% at $V = V_{crit}$~1.2 V for the chosen parameters towards 100% by the time the $n_s - V$ curve hits V=0 beyond Q_3. This state is when the metal plates touch each other and short, meaning the compliant piezoelectric material has been 'squeezed' out, something that is not accessible in the solid state, but possible in gaseous plasmas. However, the NDC regime is accessible for lower strains and at lower voltages with high compliance piezoelectric barrier materials. The charge-voltage dependence has more curvature and the critical points can be accessed at smaller voltages for gate barriers with smaller stiffness coefficients (i.e., materials that are more compliant). For example, a material with stiffness coefficient C_{33}=1 GPa is compared to C_{33}=15 GPa in Figs. 2 and 4. For the dielectric constant and the piezoelectric coefficient, we use the material parameters of scandium aluminum nitride (ScAlN) barrier [9], but we let the elastic coefficient span a wider range to explore a wider range of the electromechanical phase space. The electromechanical effect is especially sensitive to C_{33}.

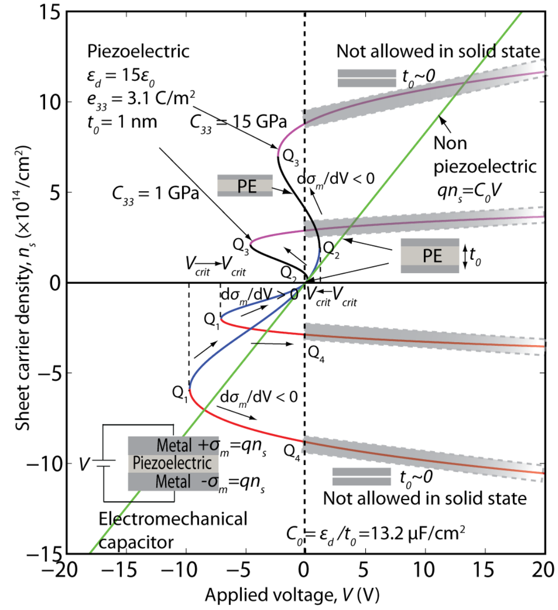

Fig. 2 – Charge-voltage (σ_m-V) characteristic of a piezoelectric (PE) electromechanical differential capacitor. It depicts the different charge states, such as positive capacitance branch $Q_1 \rightarrow Q_2$ where the slope $C_{PE} = d\sigma_m / dV > 0$ is positive, and negative capacitance branches branch $Q_2 \rightarrow Q_3$ and $Q_1 \rightarrow Q_4$ where $C_{PE} = d\sigma_m / dV < 0$. The green line is $qn_s = C_0 V$ for a passive capacitor.

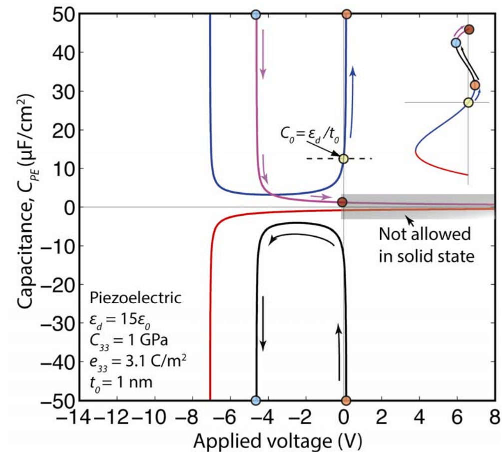

Fig. 3 – +ve & -ve differential capacitance branches of the electromechanical capacitor using a compliant piezoelectric barrier. At V=0 V, the electromechanical capacitance is $C_{PE} = C_0 = \varepsilon_d / t_0$ =13.2 μF/cm^2. The inset shows a section of the charge-voltage branch from Fig 2 with various points, with arrows showing the flow of charge with voltage, While Fig 3 shows the corresponding flow of capacitance with voltage. Note that the capacitance becomes infinite at points separating +ve and –ve differential capacitance branches.

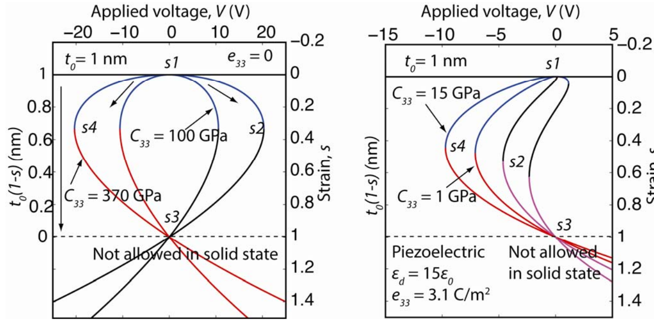

Fig. 4- Strain as a function of voltage in the piezoelectric layer. Under the applied voltage, electrostriction results in a strain $s = P / c_{33} \sim \sigma_m^2 / C_{33}\varepsilon_d$ [3, 4]. Physically accessible regime in solid state is $s_1 \rightarrow s_2 \rightarrow s_3 \rightarrow s_4$ where strain < 100%. Beyond this regime, the compressive strain along the thickness of the layer is > 100% [remaining layer thickness, t_0 (1 - s) ~ 0], which is not allowed in solid state materials.

Now by exploiting the non-linear charge-voltage characteristics of the compliant piezoelectric barrier in the gate stack of transistors, we calculate the gate capacitance C_g, the device characteristics (*I-Vs*), and the transconductance g_m of ballistic piezoFETs. The channel is chosen as GaN for Figs. 5-8, but the physics extends to any semiconductor channel material. An enhanced C_g due to the piezoelectric barrier compared to a passive dielectric in the on-state of the transistor is seen in Fig 5. This translates directly to a boost in the on-current (Figs 6, 7), which consequently improves the I_{on}/I_{off} ratio and provides a larger g_m (Fig 8). This is an attractive method to boost the on current of *any* transistor, including tunneling FETs that have low on-currents.

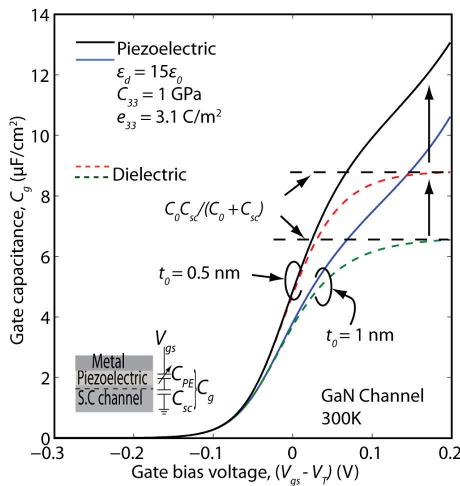

Fig. 5 – a) Gate capacitances $C_g = \partial(qn_s)/\partial V_{gs}$ versus $V_{gs} - V_T$ plot for transistors with a compliant piezoelectric (solid line) and rigid dielectric (dashed line) barriers. The charge induced in the channel is obtained by self-consistent solution of Eqs. 1-2. V_T is the threshold voltage. Higher C_g (~ 47% increase in C_g at V_{gs} -V_T= 0.2 V) occurs due to internal charge amplification than the dielectric-semiconductor gate stack. As a result of NDC using the compliant piezoelectric barriers the gate capacitance $C_g = C_{SC}C_{PE} / (C_{SC} + C_{PE})$ for a series piezoelectric/semiconductor stack is higher than $C_g = C_{SC}C_0 / (C_{SC} + C_0)$ for a series passive dielectric/semiconductor stack. Here C_{sc} is the density of states quantum capacitance, ~ 13.2 uF/cm^2 for GaN channel (electron effective mass, m^*=0.2m_0).

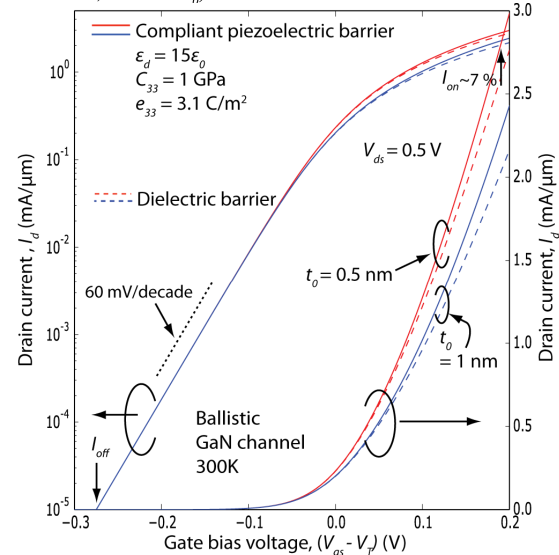

Fig. 6 – Transfer curves (I_d-V_{gs}) versus V_{gs} -V_T with logarithmic (left axis) and linear (right axis) scales at V_{ds}=0.5 V with t_0=0.5 nm, and 1 nm are shown. Higher I_{on} ~ 2.9 mA/μm at V_{gs} -V_T = 0.2 V & I_{on}/I_{off} ~ 10^5 are obtained for the transistor with piezoelectric barrier than the transistor (I_{on} ~ 2.7 mA/μm) with dielectric barrier of t_0=0.5 nm. We use electron effective mass $m^*=0.2m_0$, valley & spin degeneracy factors g_v= 1, g_s= 2 in GaN channel for calculation.

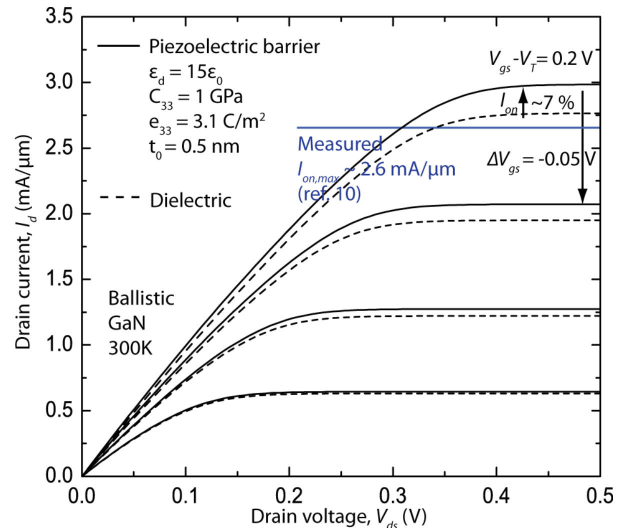

Fig. 7 – Output characteristics (I_d-V_{ds}) with different V_{gs} -V_T for GaN channel transistors are shown. Higher drain current (~ 7% increase in I_{on} at V_{gs} -V_T= 0.2 V) is resulted for the transistor with piezoelectric gate barrier (solid line) than the dielectric barrier (dashed line). Here, we indicate the measured maximum on-current $I_{on,max}$ ~ 2.6 mA/μm [10] for state-of-the art E-mode GaN HEMT device in the

figure. Therefore, there is a possibility for improving drive on-current using piezoelectric barriers in transistors.

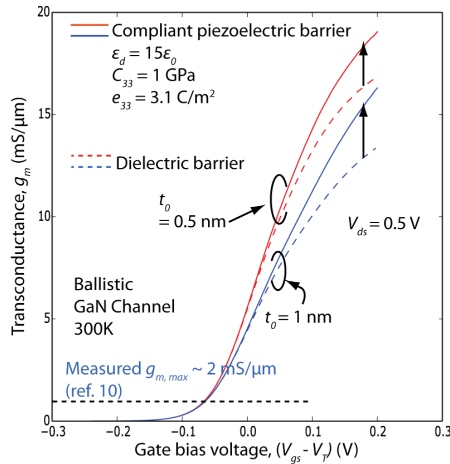

Fig. 8 – Transconductance, $g_m = \partial I_d/\partial V_{gs}$ versus gate bias voltage $V_{gs}-V_T$ at V_{ds}=0.5V is shown. Higher transconductance is resulted for the transistor with piezoelectric gate barrier (solid line) than the dielectric gate barrier (dashed line). Here, we indicate the measured maximum transconductance $g_{m,max}$ ~ 2 mS/μm [10] for state-of-the art E-mode GaN HEMT device in the figure. Thus, transconductance can also be improved using piezoelectric barriers in transistors.

To show the possibility of accessing the NDC regime, we plot the load line characteristics (Eq. 2) of the charge versus voltage relation of the piezoelectric (Eq. 1) for different V_{gs} in Fig 9. The locus of intersection points spans the allowed operating points of the transistor. The operation of the piezoelectric/semiconductor system for V_{gs}=0.2 V for example shows the internal amplification of charge at point (d) for the piezoelectric gate as compared to the passive gate charge at point (c). This is responsible for the boost in the on-state current. However, for the same material parameters, we obtain a subthreshold slope of 60 mV/decade. This is because of the inability to access the regime of NDC during the *off state operation* of transistor with the piezoelectric material properties used in the work. The steep switching behavior can be achieved if one can access the negative capacitance charge states during the off-state operation of the transistor, when $Vgs<V_T$. This may be possible by tuning the piezoelectric and compliant properties of the barrier material, and requires further study.

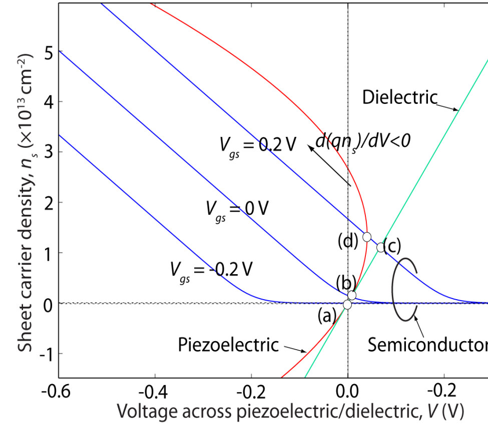

Fig. 9 – Load line analysis to obtain sheet carrier density n_s for different gate voltage, V_{gs}. Red(green) lines depict charge - voltage characteristics for piezoelectric(dielectric) capacitor. Blue curves show the semiconductor charge for different V_{gs}. Intersections of the above characteristic define the operating points of the system. At V_{gs} =0, -0.2 V, the operating points (a), (b) of the piezoelectric and dielectric barrier structures are identical, thereby giving similar currents and subthreshold slopes of 60 mV/decade. However, at V_{gs}=0.2 V, the operating point (d) lies in a regime of negative differential capacitance of the piezoelectric barrier structures. This provides an internal amplification of charge and a higher current (shown in Fig 6) as compared to point (c) of the dielectric barrier structure.

Conclusion

Transistors with compliant piezoelectric barriers based on NDC in the piezoelectric-semiconductor channel stack have been proposed. By using electrostriction and ballistic models, we show that compliant piezoelectric gate materials can boost the on current and the transconductance than conventional passive dielectric barriers. Steep switching of transistors may be possible if one can access negative capacitance regime in off-state operation of transistors by tuning the piezoelectric barrier properties. Therefore, the lower stiff, higher compliant piezoelectric barrier layers are favorable for realizing steep transistors with improved device performance.

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