Effect of Fringing Capacitances on the RF Performance of GaN HEMTs With T-Gates

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***Abstract*— The effects of fringing capacitances on the high-frequency performance of T-gate GaN high-electron mobility transistors (HEMTs) are investigated. Delay time components have been analyzed for gate-recessed InAlN/GaN HEMTs with a total gate length of 40 nm and $f_T/f_{\max}$ of 225/250 GHz. It is found that the gate extrinsic capacitance contributes significantly to the parasitic delay—approximately 50% of the total delay in these highly scaled devices. The gate extrinsic capacitance comprises two components: 1) parallel plate capacitances between the T-gate and the surrounding electrodes and 2) the fringing capacitance between the gate stem and the access regions. Detailed study of the gate electrostatics reveals that the later, the fringing capacitance between the T-gate stem and the device access region, ultimately determines the lower limit of the extrinsic capacitance C_{ext}; this minimum C_{ext} can be realized experimentally using a large gate stem height (>200 nm) and employing low-k passivation dielectric. Since the corresponding parasitic delay can be expressed as $C_{\text{ext}}/g_{m,\text{int}}$, this paper also highlights the importance of maximizing $g_{m,\text{int}}$ in ultrascaled HEMTs by adopting strategies to enhance carrier velocity.**

***Index Terms*— Cutoff frequency, electron velocity, fringing capacitance, GaN, high-electron mobility transistors (HEMT), InAlN, speed, T-gate.**

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I. Introduction

HIGH saturation velocity and breakdown electric field make GaN-based high electron mobility transistors (HEMTs) attractive for high-speed, high-power applications. Moreover, monolithically integrating enhancement-mode (E-mode) and depletion-mode (D-mode) devices can offer advantages such as fail-safe operation for power switches [1], straightforward implementation of direct coupled logic, and is attractive for mixed signal applications [2]. Impressive progress has been made on both high-speed GaN HEMTs [3]–[9] and E/D-mode integration using either selective-area epitaxial regrowth [10] or gate recess [11], [12]. To date high current-gain/power-gain cutoff frequencies ($f_T/f_{\max}$) have been achieved primarily by aggressive gate length scaling. In practice, when the gate length is reduced below 100 nm, the parasitic RC charging delay caused by source/drain (S/D) resistances and gate extrinsic capacitance can account for a significant fraction of the total delay [13]. This issue has been addressed by employing barriers, such as InAlN [3], [4] and InAlGaN [14], for high charge density (thereby reducing the access resistance), regrown n^+ GaN contacts for ultralow contact resistance [3]–[6], [15], gate stems with high aspect ratios to reduce extrinsic capacitance due to the T-gate cap [6], [7], and ultrathin passivation to reduce extrinsic capacitance [16]–[22]. The effect of the gate extrinsic capacitance on the RF performance of InP-based HEMTs has been widely reported [23], [24]; similar effects were also reported for rectangular gate GaN HEMTs [8]. However, these effects in the context of T-gate GaN HEMTs have not yet been carefully analyzed.

The extrinsic capacitance associated with a T-gate can be divided into two components: 1) parallel plate capacitances between the T-gate and the surrounding electrodes and 2) the fringing capacitance between the gate stem and the access regions. In this paper, the impact of fringing capacitance on the high-frequency performance of GaN HEMTs with T-gates is investigated. The devices analyzed are InAlN HEMTs with a total gate length of 40 nm and $f_T/f_{\max}$ ~225/250 GHz [11]. Careful analysis of the measured results, in conjunction with numerical simulation of the capacitances shows that the extrinsic capacitance associated with the gate accounts for

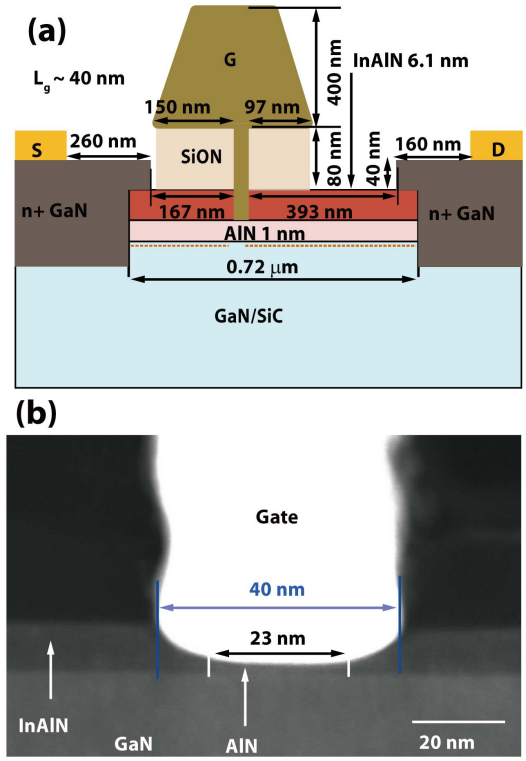

Fig. 1. (a) Schematic view of the T-gate HEMTs with recessed InAlN top barrier. (b) STEM image confirming the total L_g to be 40 nm.

>40% of the total gate capacitance in these HEMTs for gate lengths in the range of tens of nanometers. This results in an appreciable parasitic delay that limits the speed of these highly scaled devices. Based on this analysis, simulations with optimized electrode geometries indicate that f_T of these HEMTs with a total gate length of 40 nm could increase from 225 to ~270 GHz using an otherwise identical process flow; while if the process were changed to reduce R_c by 50%, the f_T could increase to ~285 GHz assuming the same intrinsic g_m (~1.68 S/mm); furthermore, with negligible short channel effects (SCEs) and negligible channel mobility degradation due to gate recess thus a higher g_m, the f_T can further reach 370 GHz.

More importantly, however, it is shown that the extrinsic capacitance of a planar HEMT is ultimately limited by the fringing capacitance between the gate stem and the access regions, which is intrinsic to the device layout and thus cannot be eliminated. This "intrinsic" extrinsic capacitance helps to illustrate why it is challenging to achieve >500 GHz $f_T/f_{\max}$ in GaN HEMTs.

II. Experiments

The $In_{0.17}Al_{0.83}N$/AlN/GaN HEMTs analyzed in this paper have an epitaxial structure consisting of a 6.1-nm InAlN barrier, a 1.0-nm AlN spacer, a 200-nm uninte ntionally-doped GaN channel, and a 1.6-μm Fe doped GaN buffer, which was grown by metal organic chemical vapor deposition on a SiC substrate. A schematic cross section of the fabricated InAlN HEMT with recessed gate is shown in Fig. 1 along with a scanning transmission electron microscopy (STEM) image showing the gate foot geometry and dimensions.

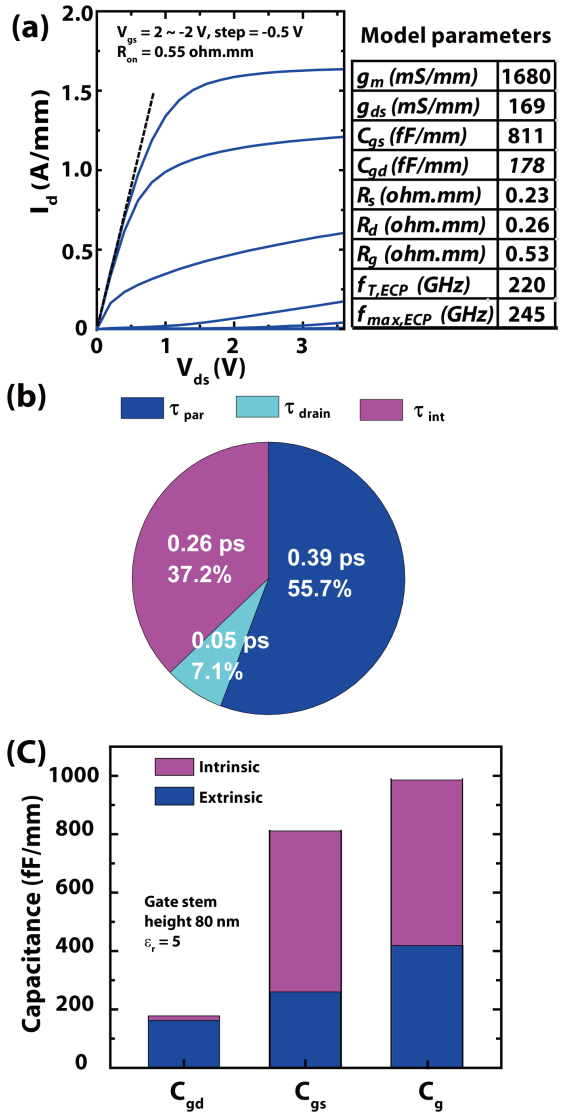

Fig. 2. (a) I_d–V_{ds} curves and the ECP values of the GaN HEMTs shown in Fig. 1, reproduced from [11]. (b) Delay time analysis results showing that the parasitic delay stemming from extrinsic components accounts for more than half of the total delay. (c) Extrinsic capacitances (extracted from COMSOL) and intrinsic capacitances (obtained by subtracting the COMSOL extrinsic capacitances from the ECP C_{gs} and C_{gd} values); the extrinsic capacitance is ~40% of the total gate capacitance.

The devices were processed at TriQuint, using graded n^+ InGaN/GaN regrown ohmic contacts [15] and a dielectric etch-back process to remove part of the SiON dielectric around the T-gate. The resultant T-gate profile is shown schematically in Fig. 1(a). The gate recess etch process is the same as reported in [25]. The total gate length L_g is ~40 nm, of which ~23 nm lies along on the bottom of the recessed region, flanked by two rounded, partially recessed areas (arc-shaped gate stem) [Fig. 1(b)]. The gate width is 2 × 25 μm and the source–drain distance L_{sd} is ~0.72 μm. Transmission line method measurements yielded contact resistance R_c and sheet resistance R_{sh} of 0.13 Ω· mm and 310 Ω/□, respectively.

III. Results and Discussion

The details of the device dc and small signal RF characteristics have been reported in [11]. The I_d–V_{ds} curves

and equivalent circuit parameters (ECPs) are reproduced in Fig. 2(a) to facilitate the analysis presented here.

Delay time analysis was performed following the method of SensaleRodriguez *et al.* [13], which is more suitable for field effect transistors with modest channel mobilities and a modification of the methods originally proposed in [26] and [27]. This method consists of two de-embedding steps: 1) de-embedding the probe pads' reactive effects—a standard procedure to measure the device speed f_T or the total delay $\tau_{\text{total}} = 1/(2\pi f_T)$ and 2) de-embedding the parasitic resistance (R_s+R_d) and extrinsic gate-source and gate-drain capacitances ($C_{\text{gs,ext}}$ and $C_{\text{gd,ext}}$) using the ColdFET measurement. After the second de-embedding, the extracted device delay is the total intrinsic device delay—comprised of the intrinsic gate delay τ_{int} and the drain delay τ_d. Subsequently, the parasitic delay time τ_{par} is computed by subtracting the total intrinsic device delay from the total delay, i.e. $\tau_{\text{par}} = \tau_{\text{total}} - \tau_{\text{int}} - \tau_d$. For the device analyzed here (Fig. 1), the resultant delay time components are $\tau_{\text{total}} = 0.7$ ps, $\tau_{\text{int}} = 0.26$ ps, $\tau_d = 0.05$ ps and $\tau_{\text{par}} = 0.39$ ps, respectively. From this analysis, it can be seen that in these devices the delay associated with charging the extrinsic capacitances accounts for >50% of the total delay time [Fig. 2(b)].

To gain insight into the physical origin of the significant parasitic delay, careful analysis and modeling of the parasitics (i.e. extrinsic components) are needed. From the analytic expression for f_T [24], the total parasitic delay can be expressed as

$$\tau_{\text{par}} = (C_{\text{gs,ext}} + C_{\text{gd,ext}})/g_m + C_{\text{gd}}(R_s + R_d) + (C_{\text{gs}} + C_{\text{gd}})(R_s + R_d)g_{\text{ds}}/g_m \quad (1)$$

where $C_{\text{gs,ext}}$ is the extrinsic gate-source capacitance, $C_{\text{gd,ext}}$ is the extrinsic gate-drain capacitance, and g_m is the intrinsic transconductance, i.e. $g_{m,\text{int}}$. Based on the ECP values, the third term in (1), $(C_{\text{gs}} + C_{\text{gd}})(R_s+ R_d)g_{\text{ds}}/g_m$ is 0.05 ps describing delay due to the SCEs. The second term, $C_{\text{gd}}(R_s + R_d)$, has a value of 0.09 ps, which corresponds to about one quarter of the total parasitic delay. Therefore, the dominant parasitic delay in this device is the first term, $(C_{\text{gs,ext}} + C_{\text{gd,ext}})/g_m$, which describes the delay due to charging of the extrinsic gate capacitance. This analysis depends critically on accurate and correct partitioning of the intrinsic and extrinsic capacitances values. To verify that the capacitances are accurate the extrinsic capacitances have been extracted from two independent methods: 1) electrostatic simulations using COMSOL [summarized in Fig. 2(c)] and 2) analysis of the S parameters from on-wafer ColdFET measurements. As will be shown, the good agreement between these two methods confirms that the dominant parasitic delay is associated with the extrinsic gate capacitance.

The geometry used in COMSOL simulations is shown in Fig. 3, largely based on the TEM image in Fig. 1(b). In order to model the 2DEG's lateral distribution, numerical TCAD simulations were performed to estimate the 2DEG lateral depletion in the channel under the ColdFET bias condition of $V_{\text{gs}} = -4$ V and $V_d = 2$ V used in the delay analysis; extensions of ~5 and 20 nm toward the source and drain were found, respectively. The undepleted 2DEG access regions are modeled as perfect conductors connected to the source and drain contacts, whereas the depleted region is treated as an insulating region. The barrier thickness t_{bar} under the gate is taken to be 4 nm, which consists of ~1 nm remaining InAlN, 1-nm AlN, and 2-nm GaN representing the separation of the 2DEG centroid from the AlN/GaN surface. The SiON relative permittivity ε_r is assumed to be 5 and the relative permittivity ε_r of AlN, InAlN, and GaN layers are all assumed to be 9. The extrinsic capacitance is extracted from the simulations using the following procedure: 1) the surface charges at the source contact and the drain contact are summed up separately (including the charge in the 2DEG access regions) and 2) the charge associated with the source is divided by the voltage difference between the gate and source to get $C_{\text{gs,ext}}$; an analogous approach is used with the drain contact to obtain $C_{\text{gd,ext}}$. The extrinsic capacitances $C_{\text{gs,ext}}/C_{\text{gd,ext}}$ were thus estimated from these simulations to be ~260/162 fF/mm, respectively.

The extrinsic capacitances were also extracted from measured $S-$parameters under ColdFET bias conditions, where the HEMT can be modeled as three capacitors between the source, gate, and drain terminals (inset of Fig. 4) since the channel is depleted under this bias. $C_{\text{gs,ext}}$ and $C_{\text{gd,ext}}$ can

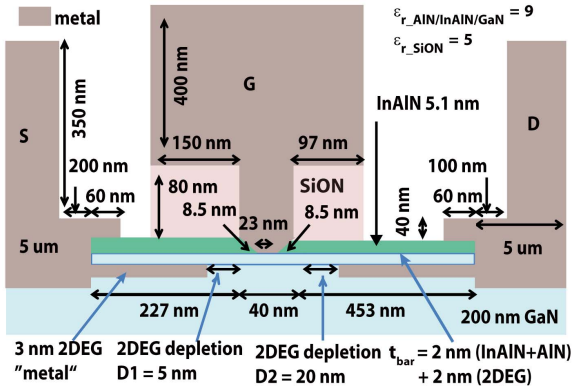

Fig. 3. COMSOL simulation setup based on the geometries obtained from the TEM image in Fig. 1(b) and the 2DEG lateral depletion widths obtained from TCAD simulations.

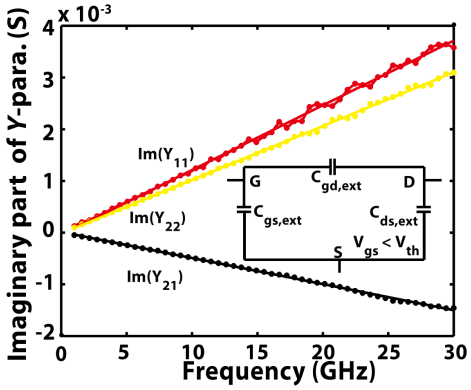

Fig. 4. Measured imaginary part of Y-parameters of the HEMT under the ColdFET bias condition with frequency ranging from 250 MHz to 30 GHz. The extrinsic capacitance can be extracted from the slope of the imaginary part of Y-parameters. Inset: equivalent circuit model of the HEMT when $V_{\text{gs}} < V_{\text{th}}$, where only the extrinsic capacitances are present since channel is fully depleted.

then be extracted using the following equations [28]:

$$\mathrm{Im}(Y_{11}) = \omega(C_{\mathrm{gs,ext}} + C_{\mathrm{gd,ext}}) \quad (2)$$

$$\mathrm{Im}(Y_{22}) = \omega(C_{\mathrm{ds,ext}} + C_{\mathrm{gd,ext}}) \quad (3)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -\omega C_{\mathrm{gd,ext.}} \quad (4)$$

In Fig. 4, the measured imaginary part of Y parameters are plotted as a function of frequency. Linear fits to the slopes in Fig. 4 were found to result in $C_{\mathrm{gs,ext}}/C_{\mathrm{gd,ext}}$ of 238/161 fF/mm, respectively, in a good agreement with the values of 260/162 fF/mm obtained from COMSOL simulations.

Assuming that the extrinsic capacitances under the peak f_T bias condition ($V_{\mathrm{gs}} = 0.9$ V and $V_d = 2$ V) are the same as those under the ColdFET bias condition [24], the intrinsic capacitances can be estimated by subtracting the extrinsic capacitances from the ECP C_{gs} and C_{gd} values obtained from measurements. The calculated intrinsic capacitances for the HEMT analyzed here are shown in Fig. 2(c). It is worth noting that this assumption of constant extrinsic capacitance with bias slightly underestimates C_{ext} since the 2DEG depletion extensions are shorter under the peak f_T bias than under the ColdFET bias conditions. Nevertheless, the extrinsic capacitance is found to account for ~40% of the total gate capacitance. This extrinsic capacitance yields a total parasitic delay time of ~ 0.37–0.39 ps, in a close agreement with the delay time analysis (0.39 ps) shown in Fig. 2(b).

IV. Optimization of the Extrinsic Capacitance

The substantial parasitic delay limits the improvement in f_T that can be achieved by further gate length scaling; further increases in device speed require reduction in these parasitic capacitances. Reduction of extrinsic capacitance can be achieved by raising the T-gate stem height, dielectric etch-back, ultrathin passivation schemes [19], and even eliminating the T-gate cap. The effectiveness of each of these approaches is discussed below.

The T-gate cap forms a parallel plate capacitance with the access regions. When the T-gate cap is raised further away from the channel, this parasitic capacitance should decrease. The key question is how large of a spacing is sufficient to maximize performance. To address this, COMSOL simulations based on the geometry shown in Fig. 3 were performed, but with key geometric parameters adjusted to show the trends. As shown in Fig. 5(a) and (b), the total fringing capacitances $C_{\mathrm{gs,ext}}/C_{\mathrm{gd,ext}}$ (with SiON) can be lowered to 231/150 fF/mm from 260/162 fF/mm if the gate stem and dielectric under gate cap height increases from 80 to 200 nm while keeping the rest of the device geometry the same. Increasing the gate stem to 300 nm does not result in any significant further reduction in capacitance. When the dielectric surrounding the gate is completely removed, the extrinsic capacitances can be reduced from 231/150 to ~160/101 fF/mm for a gate stem height of 200 nm. The extrinsic capacitances with (solid lines) and without (dash lines) a T-gate cap are also compared in Fig. 5(a) and (b) It can be seen that the parasitic capacitances $C_{\mathrm{gs,ext}}/C_{\mathrm{gd,ext}}$ associated the gate stem increase with increasing gate stem height, whereas the parasitic capacitance associated with the T-gate cap decreases. Beyond a gate stem height of 200 nm, the parasitic capacitance is completely dominated by the capacitance due to the gate stem alone. The small difference in $C_{\mathrm{gs,ext}}/C_{\mathrm{gd,ext}}$ between the solid and dashed lines, ~15 fF/mm at a gate stem of 300 nm, arises from the parasitic capacitance between the gate cap and the ohmic metal. Meanwhile, the angle of the stem sidewall would also affect the fringing capacitance. The simulation suggests the rectangular gate stem would lead to a higher extrinsic fringing capacitance than the arc-shaped gate stem due to stronger field coupling between the two sharp edges at the gate stem and the 2DEG metal. On the other hand, the optimization discussed here has the similar effect on the rectangular gate stem device.

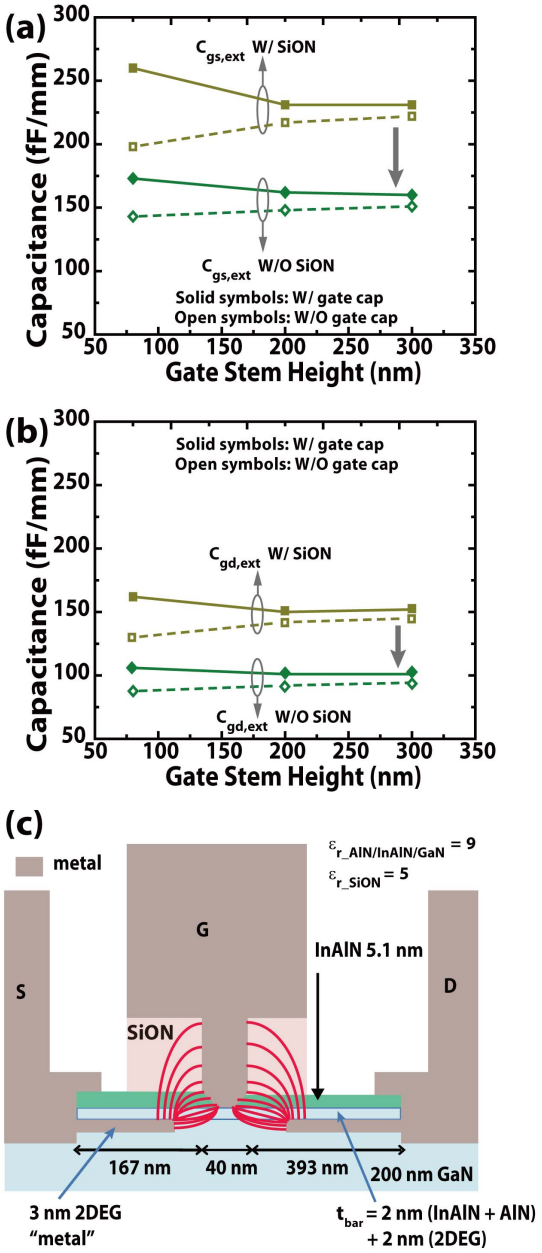

Fig. 5. (a) and (b) Simulated $C_{\mathrm{gs,ext}}$ and $C_{\mathrm{gd,ext}}$ using COMSOL as a function of gate stem height and dielectric surrounding the gate with (solid symbols) and without (open symbols) the T-gate cap. (c) Sketch to highlight the fringing capacitance between the gate stem and 2DEG access regions (red lines), which determines the minimum value of the extrinsic capacitance.

This analysis also suggests that the speed improvement observed in previously reported I-gate devices is largely due to the low parasitic capacitances associated with the short gate stem and with no T-cap (<50 nm) [3]–[5]. However, as is well-known, I-gate devices have poor $f_{\max}$ due to high gate resistance. This analysis shows that as the gate stem height is increased (to lower the gate resistance and improve $f_{\max}$), the advantage of the I-gate rapidly diminishes. The importance of low-k passivation is also apparent since the parasitic capacitance can be lowered by ~30% by eliminating the dielectric surrounding the gate.

Based on this analysis, simulations with optimized electrode geometries (a gate stem height of 200 nm and a gate-cap ohmic-post distance over 1.5 μm) indicate that f_T of the HEMT shown in Figs. 1–4 with a total gate length of 40 nm could increase from 225 to ~270 GHz using an otherwise identical process flow. While if the process were changed to further reduce R_c by 50%, the f_T could increase to ~285 GHz assuming the same intrinsic g_m (~1.68 S/mm).

V. Effect of Gate Recess

The lower bound on the extrinsic capacitance is established by the fringing electric field between the gate stem and the device access regions [Fig. 5(c)]. However, to enhance device transconductance g_m and shift threshold voltage, a gate recess process is commonly used. As the top barrier is recessed, the gate becomes closer to the access regions, and is also surrounded by the remaining semiconductor barrier with its relatively high permittivity; as a result, this lower bound for the gate fringing capacitance is expected to be higher for a recessed device compared with a device with the gate on the semiconductor surface. For example, in a conventional AlGaN/GaN HEMT, the top AlGaN barrier is typically ~30-nm thick and the remaining barrier after gate recess is ~10 nm; even without considering the dielectric passivation, the gate fringing capacitance from the recess can be significant due to the semiconductor surrounding the gate stem near the foot. On the other hand, the top barrier is generally thin (<10 nm) in InAlN HEMTs.

To illustrate the effect of gate recess on device speed, the calculated extrinsic capacitance for InAlN HEMTs with thin (6.1 nm) and thick (30 nm) top barriers and a series of recess depth under the gate are compared. In the COMSOL simulations, a gate stem height of 200 nm was used; all of the other parameters remain the same as in Fig. 3. For these simulations, the same 2DEG lateral depletion was used since the channel 2DEG concentration is nearly the same for an InAlN barrier thickness >5 nm, and the peak f_T typically occurs near the same 2DEG concentration under the gate [29]. The results are shown in Fig. 6. In addition, the capacitances with and without SiON passivation under the gate cap are included for comparison. In all cases, $C_{\mathrm{gs,ext}}$ and $C_{\mathrm{gd,ext}}$ increase with increasing recess depth (decreasing residual barrier thickness under the gate), as expected. The key observation is that $C_{\mathrm{gs,ext}}$ and $C_{\mathrm{gd,ext}}$ are smaller for the same remaining barrier thicknesses in the thin-barrier HEMTs in comparison with the thick barrier HEMTs. The thin-barrier

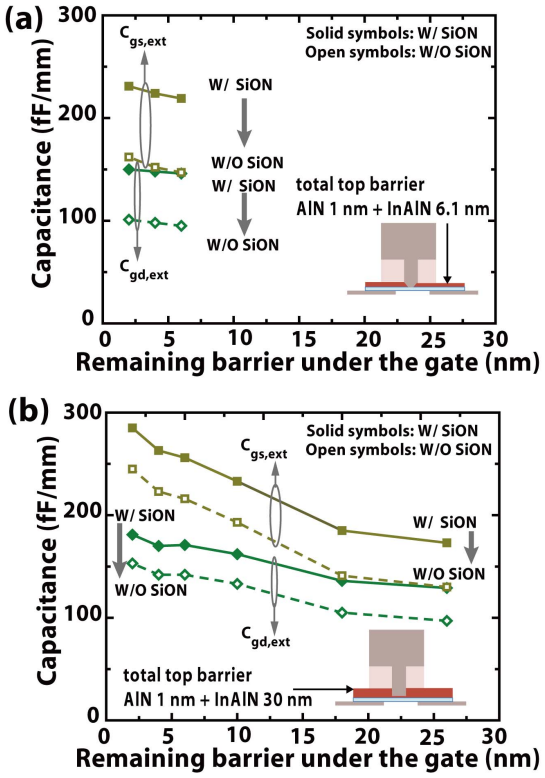

Fig. 6. Simulated extrinsic capacitances with a gate stem height of 200 nm as a function of the remaining barrier thickness under the recessed gate for HEMTs with (a) 6.1-nm total barrier and (b) 30-nm total barrier. Inset: geometry used in the COMSOL simulations.

HEMTs also show a more constant $C_{\mathrm{gs,ext}}$ and $C_{\mathrm{gd,ext}}$. These effects originate from the fact that the dielectric constant of the passivation has been assumed to be lower than that of the semiconductor. In addition, the extrinsic capacitance associated with the fringing field between the gate stem and the access regions is independent of the gate length (not shown). As a result, it is possible to experimentally extract the extrinsic capacitances by plotting the total gate capacitance versus the gate length, provided the SCEs do not significantly influence the extraction of the gate capacitance [8].

VI. Performance Projection

With C_{ext}, g_m, R_s, and R_d, one can calculate the expected f_T while neglecting the SCEs. According to [29], g_m can be expressed as

$$g_m = (\partial J/q\partial n_{s,0})C_{\mathrm{gs,int}} \tag{5}$$

$$v_{\mathrm{eff}} = \partial J/q\partial n_{s,0} \tag{6}$$

where $n_{s,0}$ is the 2DEG density at the source, v_{eff} is the effective injection velocity, $C_{\mathrm{gs,int}}$ is the intrinsic gate capacitance. $C_{\mathrm{gs,int}}$ can be obtained from 1D self-consistent Schrodinger–Poisson simulations for different remaining barrier thicknesses after gate recess. The results are shown in Fig. 7 for the 6.1-nm InAlN barrier case considered in Fig. 6(a), assuming a v_{eff} of 1.5×10^7 cm/s [29]. Since both $C_{\mathrm{gs,int}}$ and g_m scale inversely with the remaining recessed barrier thickness, the intrinsic delay is independent of recess

depth. On the other hand, the parasitic delay due to extrinsic capacitance decreases as the remaining barrier thickness is reduced since g_m increases while the parasitic capacitances depend only weakly on recess etch depth [Fig. 7(a)]. Thus, the device speed increases with decreasing remaining barrier thickness, i.e., more aggressive gate recess, provided the v_{eff} is not affected by the recess etch.

To predict the degree of improvement in f_T expected for the HEMTs shown in Fig. 1 using the otherwise same device parameters but with a v_{eff} of 1.5×10^7 cm/s, optimized gate stem height and contact resistance, lower values of $R_s/R_d =$ 0.11/0.18 Ω-mm [6], among the best reported in the literature, were used in Fig. 7(d). It is found that for the optimized 40-nm device, f_T ~370 GHz can be achieved, which is close to the best reported GaN HEMT device with T-gate [6], [12]. Since the intrinsic $C_{\text{gs,int}}$ scales with gate length, i.e., the intrinsic capacitance of the 20-nm gate length device is half that of the 40-nm device, the projected speed performance of a 20-nm device [Fig. 7(d)] can potentially reach 500 GHz with low-k passivation.

It should be noted that although InAlN barrier HEMTs have been used for the analysis presented here, this analysis applies more generally to all planar HEMTs independent of material system, since *the fringing capacitance between the gate stem and access region, together with g_m, ultimately limit the device speed even when the contact resistance is optimized to be zero and the electrodes are far from the gate.* Therefore, this paper suggests that maximizing g_m is the key to obtaining terahertz transistors. This is consistent with observations that InGaAs-channel HEMTs exhibit higher speed than GaN or Si-based FETs. To further improve the GaN HEMT speed, it is paramount to seek approaches that enhance injection velocity thus g_m, such as the use of InGaN [30] or isotope-disordered channels [31].

Finally, it is worth noting that the SCEs have been explicitly neglected in this analysis; since AlGaN [6] and InGaN [3] back barriers have been widely employed, the mitigation of SCEs is well-understood and straightforward. Furthermore, one of the ultimate embodiments on the SCE control is AlN/GaN/AlN quantum well HEMTs, which has been also recently demonstrated [32].

VII. Conclusion

The ultimate limitations on the speed of GaN HEMTs with T-gates have been investigated. The extrinsic delay is found to be a significant factor in limiting the speed in GaN HEMTs, and is fundamentally determined by the device intrinsic g_m and the fringing capacitance between the gate stem and the access regions. This result is intrinsic to all FETs with planar geometry, therefore, $(C_{\text{gs,fringing}} + C_{\text{gd,fringing}})/g_m$ could be considered as an intrinsic delay in high-frequency FETs since it cannot be eliminated by geometric optimization nor by reducing the access resistances to zero. The effect of gate recess on this fringing capacitance in the HEMTs with thin and thick top barriers was also investigated. The intrinsic delay is found to be independent of gate recess depth, whereas the extrinsic delay is reduced for deeper recesses, due to the increase in g_m, as long as the channel injection velocity is not compromised. Therefore, improving g_m, by enhancing injection velocity is the key in realizing high-speed FETs.

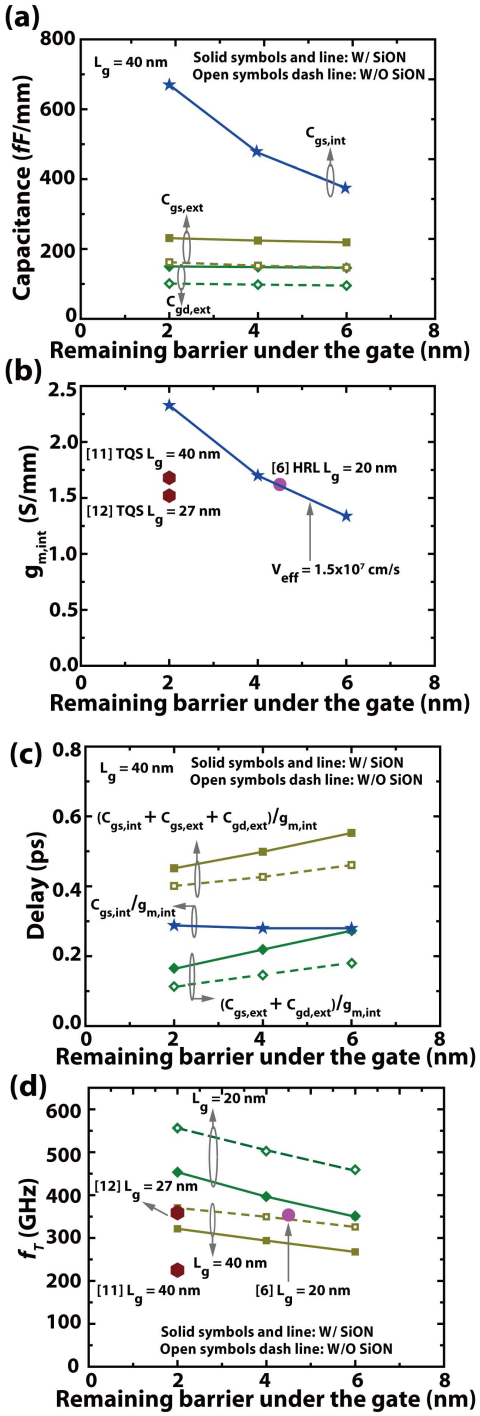

Fig. 7. Calculated performance of GaN HEMTs with a gate stem height of 200 nm, recessed gate and a thin barrier shown in Fig. 6(a). For a gate length of 40 nm (a) extrinsic and intrinsic capacitances (b) estimated intrinsic g_m and reported values and (c) delays. The intrinsic delay stays the same (SCEs neglected), the extrinsic delay decreases purely because of the enhancement in g_m. (d) Projected f_T for devices with R_s/R_d of 0.11/0.18 Ω.mm and two gate lengths: 20 and 40 nm. Also shown are $g_{m,\text{int}}$ and f_T values of several reported high performance E-mode GaN HEMTs with T-gate and f_T >200 GHz (large solid symbols).

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