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Polarization-Engineered III-Nitride Heterojunction Tunnel Field-Effect Transistors

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ABSTRACT The concept and simulated device characteristics of tunneling field-effect transistors (TFETs) based on III-nitride heterojunctions are presented for the first time. Through polarization engineering, interband tunneling can become significant in III-nitride heterojunctions, leading to the potential for a viable TFET technology. Two prototype device designs, inline and sidewall-gated TFETs, are discussed. Polarization-assisted p-type doping is used in the source region to mitigate the effect of the deep Mg acceptor level in p-type GaN. Simulations indicate that TFETs based on III-nitride heterojunctions can be expected to achieve ON/OFF ratios of 10^6 or more, with switching slopes well below 60 mV/decade, ON-current densities approaching 100 μA/μm, and energy delay products as low as 67 aJ-ps/μm.

INDEX TERMS III-nitride heterojunction, InN, polarization engineering, tunnel field-effect transistors (TFETs).

I. INTRODUCTION

TUNNEL field-effect transistors (TFETs) have been considered as a candidate to replace metal–oxide–semiconductor field-effect transistors (MOSFETs) in low-voltage, energy-efficient, and ultrascaled integrated circuits [1]. Using quantum-mechanical tunneling instead of thermionic emission, TFETs have the potential to achieve switching slopes (SSs) smaller than 60 mV/decade. To compete favorably with MOSFETs, TFETs must achieve high ON-current (I_{ON} approaching 1 mA/μm), high ON/OFF ratio ($I_{ON}/I_{OFF} > 10^5$), and small SS (SS $<$ 60 mV/decade) [2], [3]. Recently, TFETs based on narrow-gap semiconductors, such as III–V materials (e.g., InGaAs, InAs, and GaSb), have been demonstrated experimentally [4], [5]. Though achieving a high I_{ON}, these devices show a large I_{OFF}; those based on narrow effective bandgap materials exhibit severe ambipolar conduction (e.g., InAs and GaSb), due to the small bandgap [6]. To suppress I_{OFF}, wide-gap materials, like III-nitrides (such as GaN and AlN), can be used. However, the large bandgap makes it impractical to realize interband tunneling in III-nitride homojunctions. As an example, even with high impurity doping concentrations on both p- and n-type sides of a GaN homojunction (i.e., physical impurity concentrations $N_A = N_D = 3 \times 10^{19}$ cm^{-3}), the large bandgap of GaN results in a large tunneling barrier (i.e., 3.4 eV) and long tunneling distance (i.e., 15 nm), as shown in Fig. 1(a).

On the other hand, interband tunneling can be achieved in III-nitride heterojunctions through polarization engineering [7]. Due to the lack of inversion symmetry in wurtzite crystals, such as GaN, a polarization dipole is present

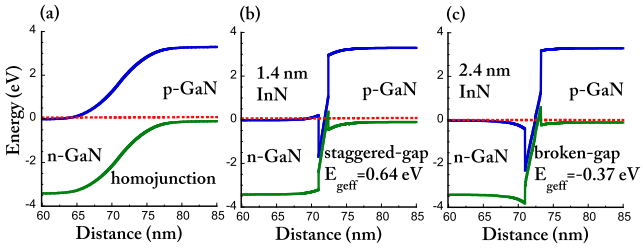

FIGURE 1. Computed band diagrams for (a) GaN homojunction, (b) staggered-gap GaN/InN/GaN heterojunction with 1.4-nm InN layer thickness, and (c) broken-gap GaN/InN/GaN heterojunction with 2.4-nm InN layer thickness.

along the *c*-axis. At heterointerfaces between materials with different internal polarizations, the discontinuity results in uncompensated sheet charge at the interface. In addition, the piezoelectric nature of these materials, combined with lattice mismatch, introduces an additional contribution to the polarization discontinuity. Through engineering of the heterostructure, the polarization-induced charge can be used to generate large internal electric fields; at sufficiently high fields, the interband tunneling can become significant even in large bandgap materials. These effects have been experimentally demonstrated for both GaN/AlN/GaN and GaN/InGaN/GaN junctions [8], [9].

To illustrate the concept of interband tunneling in III-nitride heterojunctions, Fig. 1 shows the computed band diagrams for a GaN homojunction and two GaN/InN/GaN heterostructures. For the heterojunctions in Fig. 1(b) and (c), the offset between the p-GaN valence band edge at the p-GaN/InN interface and the n-GaN conduction band edge at the n-GaN/InN interface can be considered as an effective bandgap E_{geff}. Unlike conventional heterostructures, for these III-nitride heterostructures, the effective bandgap is not fixed solely by the choice of materials; it can also be adjusted by changing the InN interlayer thickness. Alternatively, if a ternary, such as InGaN, is used as the interlayer, the selection of the In mole fraction can also be used to adjust the effective bandgap [7]. For the case of an InN interlayer shown in Fig. 1, as the InN layer thickness increases from 1.4 to 2.4 nm, the energy band diagram changes from a staggered to a broken gap alignment. This tunability of the band diagram in III-nitride heterojunctions provides the device designer with a significant additional degree of freedom.

On the basis of these heterojunctions, a range of diverse TFET designs can be contemplated. In this paper, two prototype device designs are studied by simulation to demonstrate the performance potential of III-nitride heterojunction TFETs.

II. DEVICE STRUCTURE AND SIMULATION APPROACH

Fig. 2 shows two n-channel TFET configurations. Fig. 2(a) shows an inline TFET in which the tunnel junction is parallel with the gate electrode, whereas Fig. 2(b) shows a sidewall double-gate TFET with tunnel junction

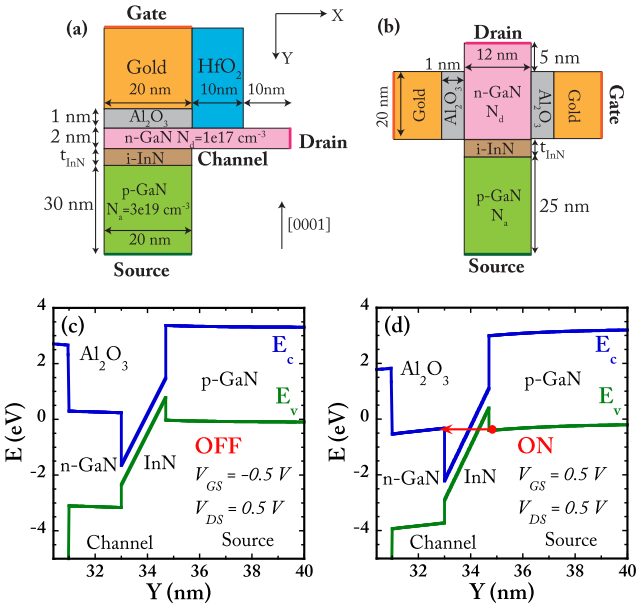

FIGURE 2. TFETs based on GaN/InN/GaN heterojunction. (a) Inline design, (b) sidewall-gated design, (c) OFF-state band diagram, and (d) ON-state band diagram for an inline TFET. The doping concentrations shown are the physical impurity concentrations.

perpendicular to the gate electrode. Both the inline and sidewall geometries have been explored theoretically and demonstrated experimentally in narrow-gap material systems; see [5] and [6] for inline designs and [4] for the sidewall-gated design. However, the implementation of these designs with wide bandgap materials has not been previously reported. In both embodiments reported here, Al_2O_3 is used as the gate oxide. For the inline structure, a high-*k* HfO_2 spacer and a drain underlap region are added between the gate and drain in order to electrostatically decouple the drain from the channel [6]. Fixed interface charge at the dielectric–semiconductor interfaces has been included in the simulation, based on the measured results reported in [10]. To illustrate the operational principle of the in-line III-nitride TFET, Fig. 2(c) and (d) shows tunnel junction band diagrams in the ON-state and the OFF-state. When the device is ON, electrons tunnel from the p-type GaN source to the n-type GaN channel, as shown in Fig. 2(d). The tunneling energy window over which tunneling can occur is controlled by the gate voltage; in the OFF-state in Fig. 2(c), the conduction band in the channel is pulled high enough in energy to preclude direct tunneling from source to channel. For the devices evaluated here, the source doping concentration N_a is set at 3×10^{19} cm^{-3}, while the channel doping concentration N_d is 10^{17} cm^{-3}. A relatively modest channel doping has been selected to facilitate gate electrostatic control of the channel.

The device structures have been simulated using two approaches: 1) a commercial drift-diffusion-based TCAD package (Synopsys Sentaurus) [11] and 2) a nonequilibrium Green's function (NEGF) simulator (NEMO5) [12], [13]. For the TCAD-based simulations,

the device electrostatics are simulated by solving Poisson's equation self-consistently with the electron and hole current continuity equations, while the interband tunneling process is treated by a Wentzel–Kramers–Brillouin (WKB)-based nonlocal band-to-band generation/recombination model. Radiative recombination and Shockley–Read–Hall recombination are also included. Since the p-type GaN dopant Mg has a deep acceptor level of 160 mV, incomplete acceptor ionization is included in the Poisson solution. Quantization effects are not considered in the TCAD simulations. This simplification results in an underestimation of the ON-current, since it ignores the possibility of tunneling from source into the quantized states in the triangular quantum well at the InN/n-GaN interface in Fig. 2(d). On the other hand, the TCAD simulation's neglect of quantum confinement may result in an overestimation of the thermionic OFF-state leakage, as quantization results in an increased effective InN bandgap. This deficiency, however, can be complemented by the second computing approach.

To address the quantum confinement and tunneling limitations of the TCAD-based simulations, NEGF-based simulations were also performed. The NEGF-based NEMO5 simulations use a finite-element nonlinear Poisson equation solver for device electrostatics and an atomistic tight-binding (TB) Hamiltonian with open boundary conditions represented by self-energies for quantum transport calculations [12], [13]. An sp^3 orbital nearest neighbor TB model is used to represent GaN and InN [14]. The model reproduces the lowest few conduction and valence bands accurately with bulk bandgaps and effective masses shown in Table 1. The combined pyroelectric and piezoelectric polarization charge is entered into the Poisson solver. The ballistic quantum transport simulations are performed by a method known as quantum transmitting boundary method [15] or the wave function formalism [16], which is an equivalent but computationally efficient formulation of NEGF for coherent ballistic transport. As discussed above, each of these simulation methods has independent strengths and weaknesses. The ballistic treatment of the NEGF simulation is expected to result in an underestimation of both the OFF-current and SS.

TABLE 1. Parameters used in the simulation.

Parameters	GaN	$In_xGa_{1-x}N$
Band gap E_g (eV)	3.4	$1.4x^2$-4.1x+3.4
Band offset ΔE_c (eV)	0	$0.98x^2$-2.87x
DOS electron effective mass (m_0)	0.2	0.2-0.13x
DOS hole effective mass (m_0)	2.08	2.08-0.67x
Conduction electron effective mass (m_0)	0.2	0.2-0.13x
Conduction hole effective mass (m_0)	0.46	0.46-0.22x
Static dielectric constant ε_r	10.5	10.5+3.0x
Electron mobility μ_e ($cm^2/V{\cdot}s$)	1050	1050
Hole mobility μ_h ($cm^2/V{\cdot}s$)	20	20
Polarization (C/m^2)	-0.029	$0.11x^2$+0.13x-0.029

For computational efficiency, TCAD has been used for most of the design optimization, with promising structures evaluated using the more physically rigorous NEGF approach. The parameters used in this paper are listed in Table 1 [17], [18]. Since strain-induced band structure modification is minor to the tunneling, parameters included in Table 1 are for the unstrained case. In Fig. 1(b) and (c), the compressively strained InN has a conduction band shift of ∼0.45 eV, while valence band shift averages to 0.28 eV based on linear deformation potential theory [19]. Since tunneling mostly happens between p- and n-GaN, the small bandgap change of InN hardly changes the effective bandgap or the tunneling probability.

III. RESULTS AND DISCUSSION

Fig. 3 shows the transfer and output characteristics for an inline GaN/InN/GaN TFET as computed using TCAD. In the common-source curves in Fig. 3(b), the device exhibits an offset voltage in V_{DS} of ∼0.15 V. This superlinear onset behavior is caused in part by incomplete ionization in the p-GaN region (the hole concentration in the quasi-neutral source is $\sim 4.2 \times 10^{17}$ cm^{-3}); the deep acceptors widen the depletion region and cause significant valence band bending in the source with increasing V_{DS}. In addition, significant occupancy function modulation with V_{DS} also contributes to the superlinear characteristics [20]. The resulting offset voltage in device output behavior is detrimental to sub-0.5 V operation. In part due to this offset, the ON-current density in this device is limited to ∼35 μA/μm.

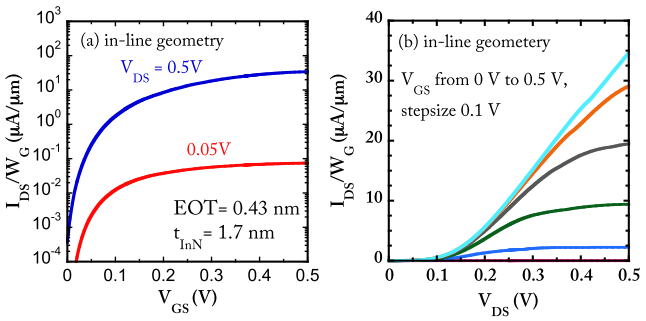

FIGURE 3. (a) Transfer and (b) output characteristics for an inline TFET based on an abrupt GaN/InN/GaN heterojunction.

To address this limitation, polarization-assisted p-type doping has been explored to facilitate deep acceptor ionization in the p-GaN source region [21]. A graded $In_xGa_{1-x}N$ layer, whose In mole fraction is linearly graded from 0 to 1, is added between the InN and p-GaN, as shown in Fig. 4(a). A comparison of the abrupt and graded junction band diagrams is shown in Fig. 4(b). As can be seen in these band diagrams, the fixed polarization charge in the graded InGaN (which is caused by the polarization grading through $\rho = -\nabla \cdot \vec{P}$) creates a built-in electric field and causes energy-band bending in the source region. As a consequence, the hole density in the ON-state at the source/InN interface is increased by nearly three orders of magnitude (i.e., effective degenerate doping in the p-GaN source) compared with the case of an abrupt GaN/InN/GaN heterojunction. Similar to degenerately doping the source region of the narrow

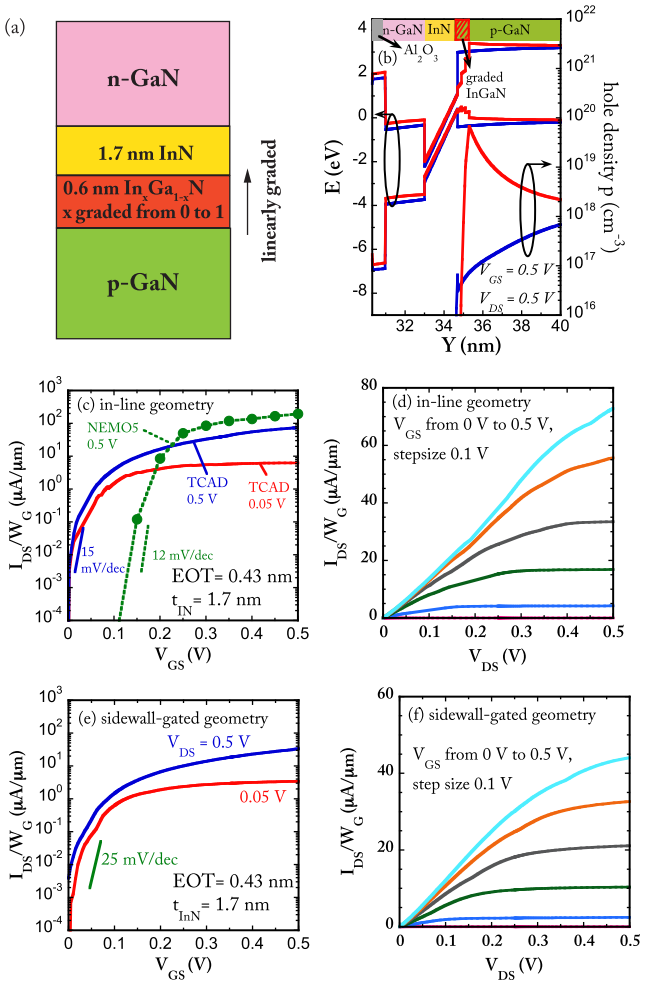

FIGURE 4. (a) Epitaxial structure and (b) computed band diagram and hole density (red line) of GaN/InN/graded-InGaN/GaN inline TFET heterostructures, where the InN thickness is 1.7 nm and graded InGaN is 0.6-nm thick. GaN/InN/GaN abrupt inline TFET band diagram and hole density (blue line) are also included for comparison. (c) Transfer and (d) output characteristics for a graded inline TFET. (e) Transfer and (f) output characteristics for a sidewall-gated TFET based on the epitaxial structure in (a). In (c), the solid lines are from TCAD simulations, while the dashed lines with dots are from NEMO5.

bandgap material-based TFET, the polarization-enhanced source doping reduces the depletion width in p-GaN, shortens the tunneling width, and enables high ON-current in III-nitride TFETs.

The transfer and output characteristic curves for TFETs based on a graded heterojunction, as shown in Fig. 4(a), are shown in Fig. 4(c)–(f). From the TCAD-calculated inline TFET transfer curve in Fig. 4(c), an ON-current of 73 μA/μm, ON/OFF ratio of 10^5, and SS of 15 mV/decade are determined. As can be seen in Fig. 4(d), the graded InGaN layer also mitigates the effect of the Mg deep acceptor in p-GaN; the offset V_{DS} in the output onset has been eliminated, and a sharp linear turn-ON characteristic is obtained. Current saturation with V_{DS} is observed at low V_{GS} in Fig. 4(d), as needed for logic and analog functions.

These promising performance metrics have been replicated with NEGF simulations, as shown in Fig. 4(c); an ON-current of 195 μA/μm, minimum SS of 12 mV/decade, and I_{ON}/I_{OFF} of 10^7 have been computed for the same device structure. It should be noted that the observed disparity in performance projections between NEGF and TCAD is not entirely unexpected. While NEGF treats the interband tunneling more rigorously than the WKB-based approach implemented in TCAD, including the effects of tunneling through quantized states near the heterointerface, the NEGF solver used for these projections does not include scattering. Thus, the NEGF simulation provides a rigorous estimate of the device ballistic limit, while the TCAD provides insight into the role of extrinsic parasitics such as source and drain access resistances on device performance. Slightly different threshold voltages (differing by ~0.1 V) are also predicted by the two simulators, as shown in Fig. 4(c). This is due to the differences between neglecting quantum confinement (TCAD) and including it (NEGF). As can be seen in Fig. 4(d), the output conductance degrades at large V_{GS}, due to drain-gate coupling (i.e., drain-induced barrier thinning). The access resistance contributes to the nonmonotonic transconductance behavior in Fig. 4(d). Since p-GaN has a small hole mobility, approximately 20 cm^2/V·s, and a modest hole density in the bulk source region due to incomplete ionization, the source series resistance is estimated to be 2.18 kΩ-μm. Due to the ultrathin n-GaN channel (2-nm thick) and its low doping concentration, the extrinsic access region of the drain contributes 1.52 kΩ-μm to the total access resistance. In the ON-state ($V_{GS} = V_{DS} = 0.5$ V), the voltage drop across the source bulk region is ~0.15 V, while the drain access resistance exhibits a drop of 0.1 V. Thus, for the design shown here, nearly half of the applied drain voltage is dropped in the access resistances, contributing to the limited ON-current and compromising the current saturation.

The sidewall-gated GaN/InN/graded-InGaN/GaN TFET is also simulated using TCAD, as shown in Fig. 4(e) and (f). Based on full-band atomistic TB calculations, the quantization-induced bandgap change for a 12-nm-thick InN body is ~28 meV (and smaller for GaN), due to their relatively large effective masses, indicating that lateral quantization effects can be neglected. In comparison to the in-line geometry, the sidewall TFET shows a modestly reduced I_{ON} and slightly higher SS. These differences have to do with choices made to improve the electrostatic gate control. For example, the channel thickness is set to be 12 nm to achieve good gate control of the channel. However, this also results in a smaller tunnel junction cross-sectional area and thus a smaller I_{ON} compared with the inline TFET (at the same gate length). To mitigate the tradeoff between electrostatic control and tunnel junction area, a gate-all-around nanowire TFET may be preferable to the double-gate structure evaluated here.

Due to challenges associated with the epitaxial growth of GaN/InN/GaN heterojunctions (originating principally from the significant difference in optimal growth temperature for InN and GaN by molecular beam epitaxy and

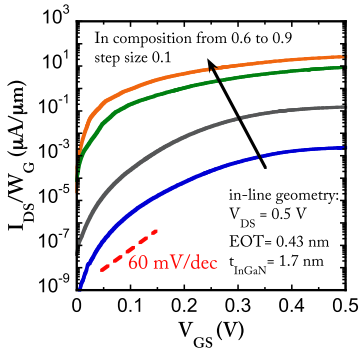

FIGURE 5. Transfer characteristics for inline TFET based on GaN/$In_xGa_{1-x}N$/graded-InGaN/GaN heterojunction, with In mole fraction from 0.6 to 0.9. The calculated results are from TCAD simulations.

their lattice mismatch), we have also investigated the performance achievable with lower In-content GaN/InGaN/graded InGaN/GaN heterojunctions. Tunnel diodes based on GaN/$In_{0.33}$GaN/GaN junctions have been demonstrated experimentally [9]. Fig. 5 shows the TCAD simulated transfer characteristics for inline GaN/InGaN/graded-InGaN/GaN TFETs with different In mole fractions in the InGaN interlayer. Steep SSs smaller than 60 mV/decade can be observed for In mole fraction from 0.6 to 0.9. Compared with the InN interlayer case, the reduced indium concentration results in larger effective bandgap and a smaller polarization charge at the heterointerface, primarily from the reduced piezoelectric contribution. This results in a smaller junction electric field and a reduced I_{ON}, as shown in Fig. 5. To analyze the dependence of the ON-current on InGaN interlayer In mole fraction, for a given interlayer thickness, the simulated ON-current is plotted for different In mole fractions as a function of supply voltage in Fig. 6(a); as expected, the ON-current monotonically increases with In mole fraction.

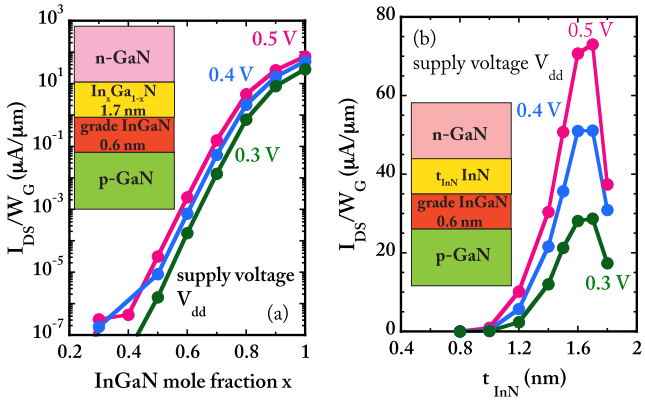

FIGURE 6. Inline TFET ON-current dependence on (a) InGaN interlayer In mole fraction and (b) InN layer thickness at supply voltages of 0.3, 0.4, and 0.5 V. Insets: corresponding heterojunction epitaxial structures. The calculated results shown in the figures are from TCAD simulations.

Another important variable in III-nitride TFET epitaxial design is the InN thickness. For GaN/InN/graded-InGaN/GaN heterojunctions, as the InN thickness increases, both the effective band offset and the tunneling distance increase. The resulting trend in ON-current is shown in Fig. 6(b). Over the 0–2-nm range of InN layer thicknesses, the heterojunction develops from staggered-gap alignment toward a broken-gap alignment with increasing t_{InN}, resulting in an appreciable increase in the output current. However, as the InN layer thickness increases beyond 1.7 nm, the tunneling current density decreases due to the longer tunneling distance. This characteristic tradeoff between tunneling distance and band offset gives an ON-current maximum at 1.7 nm [8].

To evaluate the III-nitride TFET energy efficiency for logic applications, one of the most important figures of merit is energy delay product (EDP). EDP is defined as the product of intrinsic switching energy (often approximated as $C_g V_{dd}^2$) and switching delay ($C_g V_{dd}/I_{ON}$), where V_{dd}, C_g, and I_{ON} are supply voltage, gate capacitance, and ON-current, respectively [22]. Since the gate-source and gate-drain capacitances in TFETs vary significantly with bias, the capacitive formulations can be replaced with equivalent charge-based definitions for the energy ($Q_g V_{dd}$) and delay (Q_g/I_{ON}), where Q_g is the total gate charge required to switch the device state. The EDP, which is then $Q_g^2 V_{dd}/I_{ON}$, can be directly calculated from the charge distributions in simulations. For the inline GaN/InN/graded-InGaN/GaN TFET whose characteristics are shown in Fig. 4(c) and (d), an EDP of 66.8 aJ-ps/μm at a supply voltage of 0.2 V is obtained from the TCAD results. These results compare favorably with incumbent CMOS, with EDPs well below that of either low-power 15-nm node CMOS (4860 aJ-ps/μm) at a supply voltage of 0.3 V or high-performance 15-nm node CMOS (77.6 aJ-ps/μm) at a supply voltage of 0.73 V [22]. The NEGF-based simulations are even more favorable, with ~2.5 times lower EDP (26.3 aJ-ps/μm) due to the larger ON-current (the gate charge exhibits only minor differences between NEGF and TCAD simulations). These results suggest that III-nitrides should be included as a possible viable material candidate for TFETs and, in particular, that reducing the parasitic resistance (the primary difference between the NEGF and TCAD simulations) is promising for further increasing device performance. A device benchmarking study, which includes a comparison of a wide range of device options (including III-nitride TFETs) for beyond-CMOS logic devices, can be found in [23].

IV. CONCLUSION

The concept, operational principles, and a simulation study of the expected performance for III-nitride heterojunction TFETs are presented for the first time. The potential benefits of these devices are illustrated through the numerical simulation. Though not fully optimized, simulations based on both drift-diffusion and NEGF formulations suggest that TFETs based on III-nitride heterojunctions can be expected to achieve ON-currents on the order of 100 μA/μm at the supply voltages of 0.5 V and below, while also achieving SSs below 20 mV/decade. They also show a low EDP of 66.8 aJ-ps/μm,

which makes them promising as energy-efficient switches. As the first report of performance projection for polarization-engineered III-nitride heterojunction TFETs, this paper is a starting point for further study.

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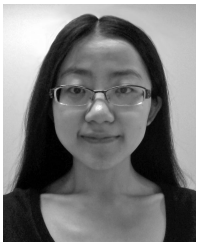

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