Ultralow-Leakage AlGaN/GaN High Electron Mobility Transistors on Si With Non-Alloyed Regrown Ohmic Contacts

Bo Song, Mingda Zhu, Zongyang Hu, Meng Qi, Kazuki Nomoto, Xiaodong Yan, Yu Cao, *Member, IEEE*, Debdeep Jena, *Senior Member, IEEE*, and Huili Grace Xing, *Senior Member, IEEE*

***Abstract*— Without employing gate dielectrics, AlGaN/GaN high-electron mobility transistors (HEMTs) on Si with non-alloyed regrown ohmic contacts exhibit record-low leakage currents $\sim 10^{-12}$ A/mm, high ON/OFF current ratios $>10^{11}$. Compared with HEMTs with conventional alloyed ohmic contacts, HEMTs with non-alloyed contacts show a reduction of 10^6 in leakage current, a steeper subthreshold slope, and >50% improvement in breakdown voltage. These observations indicate that avoiding high-temperature alloyed ohmic processes can lead to improved device performance.**

***Index Terms*— Leakage current, non-alloyed and alloyed ohmic contact, regrown contact, trap, GaN on Si, HEMT.**

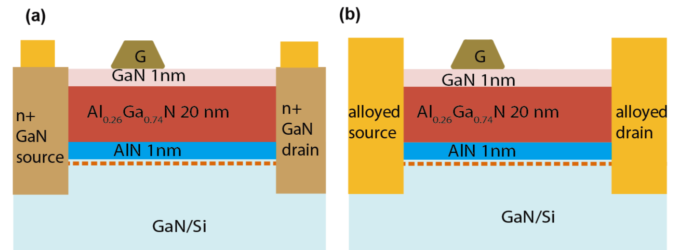

Fig. 1. Schematic cross section of AlGaN/GaN HEMT on Si with (a) non-alloyed contacts regrown by MBE and (b) alloyed contacts.

I. Introduction

GaN BASED high electron mobility transistors (HEMTs) have demonstrated great potential for high-speed, high-power RF applications [1], [2] and next-generation power electronics [3], [4]. In addition, the adoption of a Si substrate would pave the way for low cost and high-performance GaN electronics. However, the high leakage current often observed in GaN HEMTs causes extra noise in power amplifiers [5], additional loss in power converter [6], and current collapse [7]. Several approaches have been reported to address these problems, including: inserting a gate dielectric to form metal-insulator-semiconductor HEMTs [8], [9], O_2 [10] and CF_4 [11] plasma treatment underneath the gate and post-metal-annealing in forming gas [12]. These methods are able to reduce the gate leakage current thus improving the ON/OFF current ratio up to $10^8 - 10^{12}$. The sources of high leakage current have been reported to be traps situated at the interface, surface and bulk [7], [13]–[15]. However, the origins of these traps are still under debate. Higashiwaki et al. reported that the high-temperature alloyed ohmic process generates surface traps [16]. On the other hand, SiN_x and AlN passivation on GaN HEMTs have also been widely reported to effectively minimize current collapse (dynamic R_{on}) but often at the expense of an increase in leakage [17], [18].

In this letter, we report on ultralow-leakage GaN HEMTs on Si without employing any gate dielectrics that have non-alloyed regrown ohmic contacts, then compare them to HEMT devices with alloyed ohmics. By avoiding the high-temperature alloying process, HEMTs with non-alloyed ohmic contacts show a high ON/OFF current ratio $>10^{11}$ and a record low leakage $\sim 10^{-12}$ A/mm, about 10^6 lower than devices with alloyed contacts. A lower subthreshold slope and higher breakdown voltage have also been observed.

II. Experiments

Schematic cross-sections of HEMT devices with non-alloyed and alloyed ohmic contacts are shown in Fig. 1(a) and Fig. 1(b), respectively. The HEMT structure consists of a 1 nm GaN cap, a 20 nm $Al_{0.26}Ga_{0.74}N$ barrier, a 1 nm AlN spacer and a GaN channel on a 1.3 μm semi-insulating GaN buffer grown by metal organic chemical vapor deposition (MOCVD) on 6” Si substrates.

For the non-alloyed contacts, an n^+GaN regrowth process was employed using molecular beam epitaxy (MBE) to ensure contact with the 2D electron gas (2DEG) channel, which we have routinely employed for our GaN HEMT processes for

Manuscript received September 16, 2015; revised October 28, 2015; accepted October 30, 2015. Date of publication November 3, 2015; date of current version December 24, 2015. The review of this letter was arranged by Editor D.-H. Kim. *(Corresponding authors: Bo Song and Huili Grace Xing.)*

B. Song, M. Zhu, Z. Hu, and K. Nomoto are with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA (e-mail: bs728@cornell.edu).

M. Qi and X. Yan are with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA.

Y. Cao was with IQE Massachusetts, Taunton, MA 02780 USA. He is now with HRL Laboratories, LLC, Malibu, CA 90265 USA.

D. Jena and H. G. Xing are with the School of Electrical and Computer Engineering and the Department of Materials Science and Engineering, Cornell University, Ithaca, NY 14853 USA, and also with the Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: grace.xing@cornell.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2015.2497252

0741-3106 © 2015 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

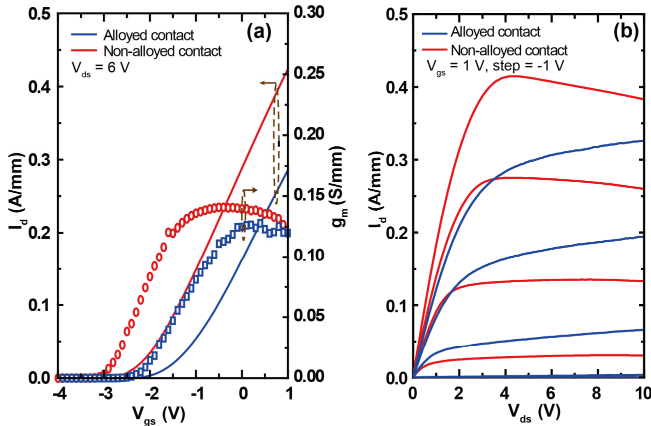

Fig. 2. (a) Linear-scale transfer curves at $V_{ds} = 6$ V by sweeping V_{gs} from 1 to −4 V and (b) common-source $I - V$ characteristics, of the HEMTs.

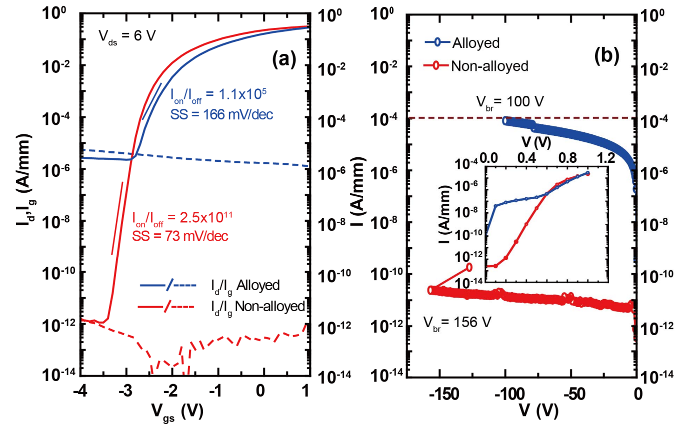

Fig. 3. (a) Semi-log-scale transfer curves at $V_{ds} = 6$ V and (b) gate stack diode I–V curves showing breakdown voltages, of the alloyed and non-alloyed devices.

high-speed transistors, p-channel transistors, AlN/GaN/AlN quantum well transistors as well as studying ohmic contact science [19]–[29]. A 200 nm thick SiO_2 mask was deposited on the sample using plasma-enhanced chemical vapor deposition (PECVD) and then patterned by reactive ion etching (RIE). The regrowth regions were etched to a depth of 40 nm using a low-damage BCl_3/Cl_2 inductively coupled plasma RIE (ICP-RIE) recipe. MBE regrowth of an 80 nm thick Si-doped ($\sim 10^{20}$ cm^{-3}) GaN layer was performed at 660 °C. Lift-off by buffered HF removed the polycrystalline GaN that was grown on SiO_2. It is worth noting that the device surface was protected by SiO_2 during the regrowth process, where temperature is also much lower than that of the contact alloying process (870 °C). Ohmic contacts to the regrowth region were formed by E-beam evaporation of 20/100 nm Ti/Au, resulting a contact resistance R_C of 0.1 Ω·mm. For the alloyed contact devices, a 20/100/40/50 nm of Ti/Al/Ni/Au stack annealed in N_2 ambient at 870 °C for 20 s was used, resulting in a R_C of 0.3 Ω·mm. Hall measurements on the non-alloyed (alloyed) devices revealed a 2DEG concentration of 7.63×10^{12} (4.57×10^{12}cm^{-2}) and mobility of 1620 (1420) cm^2/Vs at room temperature. A 2 μm × 50 μm ($L_g \times W_g$) gate was defined by optical photolithography, followed by a 40/100 nm Ni/Au gate metallization. The gate-to-drain spacing (L_{gd}) and the gate-to-source spacing (L_{gs}) are 4.75 and 2 μm, respectively. There was no passivation applied for any of the devices.

III. Results and Discussion

The linear-scale transfer curves and DC common source characteristics are shown in Fig. 2. The non-alloyed (alloyed) HEMTs show an output drain current density 0.42(0.29) A/mm at $V_{gs} = 1$ V and $V_{ds} = 6$ V and a peak extrinsic transconductance g_m 142(126) mS/mm, which is expected since the non-alloyed device has a lower contact resistance and sheet resistance. The threshold voltage extracted from linear extrapolation of the transfer curve at peak g_m (Fig. 2(a)) is −2(−1.4) V for non-alloyed (alloyed) HEMTs. Transmission electron microscopy imaging (not shown) revealed that under the gate metal no additional insulator formed in the non-alloyed device, which is different from Refs. [1] and [10]. The apparent drain conductance of the alloyed device is observed to be large under the measurement conditions used, which is attributed to the severe trapping effects (also see Fig. 4) and worthy of a separate study to gain a full understanding.

Figure 3(a) shows the semi-log-scale transfer curves for both HEMTs measured at $V_{ds} = 6$ V. The gate leakage current reduces from $\sim 10^{-6}$ to $\sim 10^{-12}$ A/mm at off state, which is close to the record-low leakage current in GaN HEMTs on any substrate [12]. Moreover, the subthreshold slope (SS) decreases from 166 to 73 mV/dec, approaching the theoretical limit at 300 K. The gate diode I-V characteristics are shown in Fig. 3(b). The alloyed HEMT shows a soft breakdown, approaching 100 V at 100 μA/mm (Fig. 3(b)). The current in the non-alloyed HEMT stays low ($< 10^{-10}$ A/mm) till 156 V where the current increases sharply due to field crowding near the gate edge since neither of the devices employed field plates. From the forward characteristics (shown in the inset of Fig.3 (b)), an apparent Schottky barrier height of 1.25(0.81) eV and the ideality factor 1.1(4.2) are extracted for the non-alloy (alloyed) devices. An ideality factor close to unity in the non-alloyed devices indicates the Schottky barrier height should be at least 1.25 eV between Ni and pristine (Al)GaN surface. The lower extracted barrier height along with a high ideality factor is a signature of high gate leakage.

Pulsed I–V measurements are commonly employed to probe electron trapping/emission; minimal current collapse corresponds to either no trapping/emission or extremely fast trapping/emission. The results performed in air are shown in Fig. 4, using a 300 ns pulse width and a 0.5 ms pulse period with the following quiescent bias points (V_{gs}, V_{ds}): (0 V, 0 V) as the cold pulse, (−6 V, 0 V) for gate lag, and (−6 V, 10 V) for drain lag. Gate lag reduces from 90% in the alloyed device to 19% in the non-alloyed device. The finite gate lag in the non-alloyed devices could stem from local air breakdown, residue traps, etc. Drain lag for the non-alloyed HEMTs was observed to be 4% while the lag in the alloyed HEMTs couldn't be determined due to its severe gate lag. The small current collapse in the non-alloyed devices correlates

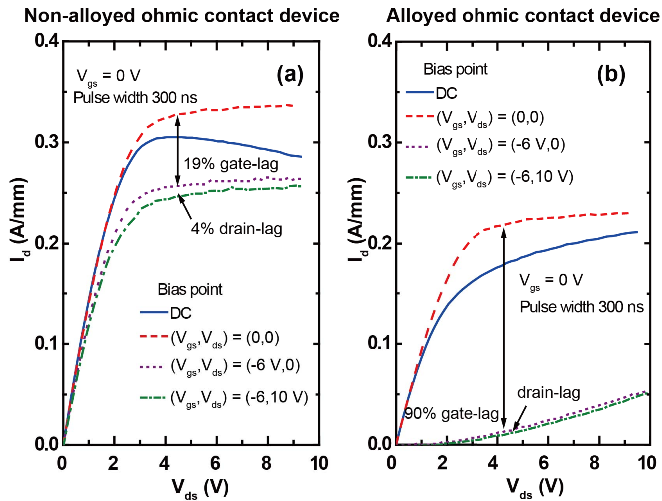

Fig. 4. Pulsed I–V measurements in air at $V_{gs} = 0$, with a 300 ns pulse width and 0.5 ms period for the (a) non-alloyed and (b) alloyed devices.

well with its low gate leakage: the low leakage prevents electrons being trapped within hundreds of microseconds when the device is held at the off state. On the other hand, the high leakage in the alloyed device facilitates electron trapping and the electron emission rates from the traps are too low to recover the current, thus a severe current collapse.

It is also interesting to compare the DC and cold pulse curves. Both devices exhibit well-behaved cold pulse I_d-V_{ds} curves: a linear increase in current followed by saturation with a negligible output conductance owing to the large L_g. In the non-alloyed devices, the apparent output conductance is negative, attributable to self-heating. However, in the alloyed devices, a positive output conductance is seen, consistent with the hypothesis that a large number of traps exist and communicate with the gate/channel within the time frame investigated in this work. Traps have complex distributions spatially as well as in the energy space, thus exhibiting complex dynamic behavior under different excitations (bias, temperature, photons). Understanding electron emission /trapping mechanisms merits another study.

The high temperature ohmic annealing process in AlGaN HEMTs (typically $> 800°$C) has been reported to be responsible for surface Fermi level pinning near mid-gap through traps arising from oxygen incorporation [16], [28]. Such traps can contribute to a high gate leakage by trap-assisted tunneling, hopping conduction [14] and surface barrier thinning [7], [30]. In our process, increase in oxygen at the HEMT surface was indeed confirmed by x-ray photoelectron spectroscopy (XPS) and a subsequent high-temperature annealing on unpassivated devices with non-alloyed contacts degraded the device performance in terms of dispersion and device speed [28]. HEMTs with non-alloyed contacts avoid unfavorable high temperature processes, thus effectively suppressing the leakage commonly observed in AlGaN HEMTs. Alternatively, a suitable capping material can be used during the contact alloying process to protect the HEMT surface. This work also suggests that the as-grown AlGaN barrier is reasonably insulating with favorably low trap densities. For real world applications, a moisture barrier/passivation layer is typically employed and such processes need to be carefully investigated similar to that of high-quality gate dielectrics. Extreme care needs to be taken during subsequent device process steps to minimize introduction of damage.

IV. Conclusion

In this letter, we report on AlGaN/GaN HEMTs on Si with non-alloyed regrown ohmic contacts showing a record-low leakage current, about six orders of magnitude smaller than that of the conventional devices with alloyed ohmics.

References

[1] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, T. Fang, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. G. Xing, "InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 988–990, Jul. 2012.

[2] D. Denninghoff, J. Lu, E. Ahmadi, S. Keller, and U. K. Mishra, "N-polar GaN/InAlN MIS-HEMT with 400-GHz f_{max}," in *Proc. 70th Annu. DRC*, 2012, pp. 151–152.

[3] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013.

[4] M. Zhu, B. Song, M. Qi, Z. Hu, K. Nomoto, X. Yan, Y. Cao, W. Johnson, E. Kohn, D. Jena, and H. G. Xing, "1.9-kV AlGaN/GaN lateral Schottky barrier diodes on silicon," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 375–377, Apr. 2015.

[5] C. Sanabria, A. Chakraborty, H. Xu, M. J. Rodwell, U. K. Mishra, and R. A. York, "The effect of gate leakage on the noise figure of AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 19–21, Jan. 2006.

[6] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "High breakdown voltage undoped AlGaN-GaN power HEMT on sapphire substrate and its demonstration for DC-DC converter application," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1913–1917, Nov. 2004.

[7] H. Hasegawa, T. Inagaki, S. Ootomo, and T. Hashizume, "Mechanisms of current collapse and gate leakage currents in AlGaN/GaN heterostructure field effect transistors," *J. Vac. Sci. Technol. B*, vol. 21, no. 4, pp. 1844–1855, Jul. 2003.

[8] M. Van Hove, S. Boulay, S. R. Bahl, S. Stoffels, K. Xuanwu, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere, "CMOS process-compatible high-power low-leakage AlGaN/GaN MISHEMT on silicon," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 667–669, May 2012.

[9] Z. Hu, Y. Yue, M. Zhu, B. Song, S. Ganguly, J. Bergman, D. Jena, and H. G. Xing, "Impact of CF_4 plasma treatment on threshold voltage and mobility in Al_2O_3/InAlN/GaN MOSHEMTs," *Appl. Phys. Exp.*, vol. 7, pp. 031002-1–031002-4, Feb. 2014.

[10] J. W. Chung, J. C. Roberts, E. L. Piner, and T. Palacios, "Effect of gate leakage in the subthreshold characteristics of AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1196–1198, Nov. 2008.

[11] R. Chu, L. Shen, N. Fichtenbaum, D. Brown, S. Keller, and U. K. Mishra, "Plasma treatment for leakage reduction in AlGaN/GaN and GaN Schottky contacts," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 297–299, Apr. 2008.

[12] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena, and H. G. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 309–311, Mar. 2011.

[13] J. C. Carrano, T. Li, P. A. Grudowski, C. J. Eiting, R. D. Dupuis, and J. C. Campbell, "Current transport mechanisms in GaN-based metal–semiconductor–metal photodetectors," *Appl. Phys. Lett.*, vol. 72, no. 5, p. 542, 1998.

[14] E. J. Miller, E. T. Yu, P. Waltereit, and J. S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 535–537, 2004.

[15] E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso, "AlGaN/GaN-based HEMTs failure physics and reliability: Mechanisms affecting gate edge and Schottky junction," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3119–3131, Nov. 2013.

[16] M. Higashiwaki, S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Effects of oxidation on surface chemical states and barrier height of AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 97, no. 22, pp. 222104-1–222104-3, 2010.

[17] H. Kim, R. M. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, and L. F. Eastman, "Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 421–423, Jul. 2003.

[18] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, "Effective passivation of AlGaN/GaN HEMTs by ALD-grown AlN thin film," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 516–518, Apr. 2012.

[19] J. Guo, Y. Cao, C. Lian, T. Zimmermann, G. Li, J. Verma, X. Gao, S. Guo, P. Saunier, M. Wistey, D. Jena, and H. G. Xing, "Metal-face InAlN/AlN/GaN high electron mobility transistors with regrown ohmic contacts by molecular beam epitaxy," *Phys. Status Solidi A*, vol. 208, no. 7, pp. 1617–1619, 2011.

[20] J. Guo, G. Li, F. Faria, Y. Cao, R. Wang, J. Verma, X. Gao, S. Guo, E. Beam, A. Ketterson, M. Schuette, P. Saunier, M. Wistey, D. Jena, and H. G. Xing, "MBE-regrown ohmics in InAlN HEMTs with a regrowth interface resistance of 0.05 $\Omega \cdot$mm," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 525–527, Apr. 2012.

[21] F. A. Faria, J. Guo, P. Zhao, G. Li, P. K. Kandaswamy, M. Wistey, H. G. Xing, and D. Jena, "Ultra-low resistance ohmic contacts to GaN with high Si doping concentrations grown by molecular beam epitaxy," *Appl. Phys. Lett.*, vol. 101, no. 3, p. 032109, 2012.

[22] G. Li, R. Wang, J. Guo, J. Verma, Z. Hu, Y. Yue, F. Faria, Y. Cao, M. Kelly, T. Kosel, H. G. Xing, and D. Jena, "Ultrathin body GaN-on-insulator quantum well FETs with regrown ohmic contacts," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 661–663, May 2012.

[23] G. Li, R. Wang, B. Song, J. Verma, Y. Cao, S. Ganguly, A. Verma, J. Guo, H. G. Xing, and D. Jena, "Polarization-induced GaN-on-insulator E/D Mode p-channel heterostructure FETs," *IEEE Electron Device Lett.*, vol. 34, no. 7, pp. 852–854, Jul. 2013.

[24] Y. Yue, Z. Hu, J. Guo, B. Sensale-Rodriguez, G. Li, R. Wang, F. Faria, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. G. Xing, "Ultrascaled InAlN/GaN high electron mobility transistors with cutoff frequency of 400 GHz," *Jpn. J. Appl. Phys.*, vol. 14, no. 8S, pp. 1–2, 2013.

[25] R. Wang, G. Li, G. Karbasian, J. Guo, B. Song, Y. Yue, Z. Hu, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. G. Xing, "Quaternary barrier InAlGaN HEMTs with $f_T/f_{\max}$ of 230/300 GHz," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 378–380, Mar. 2013.

[26] R. Wang, G. Li, G. Karbasian, J. Guo, F. Faria, Z. Hu, Y. Yue, J. Verma, O. Laboutin, Y. Cao, W. Johnson, G. Snider, P. Fay, D. Jena, and H. G. Xing, "InGaN channel high-electron-mobility transistors with InAlGaN barrier and $\mathrm{f_T}/f_{\max}$ of 260/220 GHz," *Appl. Phys. Exp.*, vol. 6, no. 1, p. 016503, 2013.

[27] S. Ganguly, B. Song, W. Hwang, Z. Hu, M. Zhu, J. Verma, H. G. Xing, and D. Jena, "AlGaN/GaN HEMTs on Si by MBE with regrown contacts and $\mathrm{f_T} = 153$ GHz," *Phys. Status Solidi C*, vol. 11, nos. 3–4, pp. 887–889, 2014.

[28] R. Wang, G. Li, J. Guo, B. Song, J. Verma, Z. Hu, Y. Yue, K. Nomoto, S. Ganguly, S. Rouvimov, X. Gao, O. Laboutin, Y. Cao, W. Johnson, P. Fay, D. Jena, and H. G. Xing, "Dispersion-free operation in InAlN-based HEMTs with ultrathin or no passivation," in *Proc. IEEE IEDM*, Dec. 2013, pp. 28.6.1–28.6.4.

[29] D. Jena, K. Banerjee, and H. G. Xing, "2D crystal semiconductors: Intimate contacts," *Nature Mater.*, vol. 13, pp. 1076–1078, Nov. 2014.

[30] T. Hashizume, J. Kotani, and H. Hasegawa, "Leakage mechanism in GaN and AlGaN Schottky interfaces," *Appl. Phys. Lett.*, vol. 84, no. 24, pp. 4884–4886, 2004.