1.7-kV and 0.55-m$\Omega \cdot cm^2$ GaN p-n Diodes on Bulk GaN Substrates With Avalanche Capability

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***Abstract*— We report vertical GaN-on-GaN p-n diodes with a breakdown voltage (BV) of 1.7 kV and a low differential specific ON-resistance R_{ON} of 0.55 m$\Omega \cdot cm^2$ with current spreading considered (or 0.4 m$\Omega \cdot cm^2$ using the diode bottom mesa size), resulting in a figure-of-merit (V_B^2/R_{ON}) of 5.3 GW/cm^2 (or 7.2 GW/cm^2). These devices exhibit a current swing over 14 orders of magnitude and a low ideality factor of 1.3. Temperature dependent *I–V* measurements show that the BV increases with increasing temperature, a signature of avalanche breakdown.**

***Index Terms*— p-n junction diodes, high breakdown voltage, avalanche breakdown, specific on-resistance, ideality factor, bulk gallium nitride (GaN).**

I. Introduction

GaN-BASED devices are attractive for high-frequency, high-power and high-efficiency applications due to a unique combination of high breakdown electric field, high saturation drift velocity, high electron mobility and high thermal conductivity [1], [2]. For power electronics, Si devices are approaching the material limit thus there is a growing effort in wide bandgap semiconductors, including SiC, GaN and Ga_2O_3, to continue improvements in terms of device size and efficiency [3]–[9]. The key advantages of GaN over SiC include a higher carrier mobility μ and a higher critical breakdown field (E_C) thus a more favorable Baliga figure-of-merit (BFOM) $\propto \mu E_C^3$; the key advantages of GaN over Ga_2O_3 to date include a higher carrier mobility μ, a higher thermal conductivity and the ability to achieve both p- and n-type doping. In the past few years, GaN-based lateral power switching transistors with breakdown voltage (*BV*) ratings >600 V have started being adopted in power systems. However, development of the GaN vertical power devices lagged behind due to the unavailability of high-quality and high-quantity GaN bulk substrates. This situation is being transformed dramatically in the recent years since both the GaN-based laser/lighting industry as well as the power industry demand GaN bulk substrates [9], [10]. GaN grown on sapphire, SiC or Si substrates, typically possesses a high density of defects thus leading to device performance far below expectation.

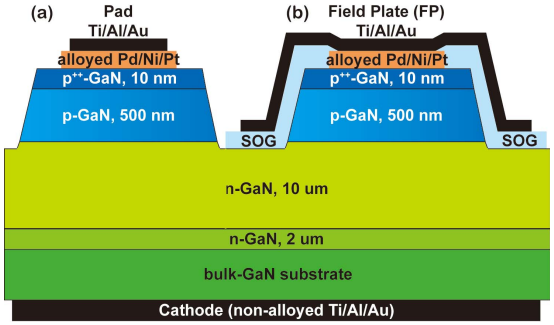

Fig. 1. Schematic cross-sections of the GaN-on-GaN p–n junction diodes (a) without (w/o) field plate (FP) and (b) with FP.

A p-n junction diode is the most fundamental device to demonstrate the capability and quality of a semiconductor material, serving as the basis for nearly all of the optoelectronic devices such as light emitting diodes, photodetectors, solar cells, as well as nearly all of the vertical power devices. To this end, we have been optimizing epitaxial growth on bulk GaN as well as device processing to achieve *BV* > 1200 V in GaN p-n diodes. In 2011 Nomoto et al. reported large area GaN-on-GaN p-n diodes with *BV* >450 V and a diameter of 3 mm [5]. Very recently, Kizilyalli et al. claimed 16 mm^2 p-n diodes with *BV*>1200 V and a yield approaching 70% [9]. GaN p-n diodes with *BV*>3 kV with low leakage have also been recently demonstrated by a number of groups [11], [12]. In this letter, we report vertical GaN p-n diodes on bulk GaN substrates with avalanche breakdown, a low differential specific on-resistance of 0.55 m$\Omega \cdot cm^2$ and a low ideality factor of 1.3, all achieved simultaneously, indicating the material quality of GaN p-n diodes are now on par with that of SiC.

II. Growth and Device Fabrication

The GaN p-n diodes shown in Fig. 1 consist of a 10 nm p^{++} GaN (Mg: $2 \times 10^{20} cm^{-3}$) contact layer, a 500 nm

Manuscript received November 16, 2015; revised December 4, 2015; accepted December 5, 2015. Date of publication December 8, 2015; date of current version January 25, 2016. This work was supported by the ARPA-E SWITCHES Program. The review of this letter was arranged by Editor A. Ortiz-Conde. *(Corresponding authors: Kazuki Nomoto and Huili Grace Xing.)*

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Digital Object Identifier 10.1109/LED.2015.2506638

p-GaN (Mg: 1×10^{18}cm^{-3}) layer, a 10 μm n-GaN drift region with a target Si doping concentration of 1-2 $\times$ 10^{16}cm^{-3} and reasonably low background impurity concentrations: C $\sim$1.2 $\times$ 10^{16} cm^{-3} and O $\sim$ 1.7 $\times$ 10^{16} cm^{-3}, and 2 μm n^{+} GaN buffer layer (Si: 2×10^{18}cm^{-3}) on a 2-inch 400 μm thick bulk GaN substrate, all grown by metalorganic vapor phase epitaxy. These target concentrations were deduced from secondary ion mass spectrometry measurements on calibration wafers grown under the same growth conditions. Plain-view cathodoluminescence reveals that the threading dislocation density (TDD) in the homoepitaxial GaN epilayers is low and uniform ($\sim 10^{6}$cm^{-2}), comparable to that of the bulk GaN substrates, which is at least two orders of magnitude lower than that of heteroepitaxial GaN. After growth, a thermal annealing was performed at 700 °C to activate Mg acceptors. The p-type GaN layer has a hole concentration of 7.4 $\times$ 10^{16} cm^{-3} with a mobility of 27 cm^2/V $\cdot$ s at 25 °C as determined by the Hall effect measurements.

The schematic cross-sections of the fabricated GaN diodes without (w/o) and with field plate (FP) are shown in Fig. 1. The FP is formed by extending a metal layer over the entire mesa of the diode covered by spin-on-glass (SOG), in order to reduce reverse leakage current thus improving breakdown voltage. The fabrication process starts with a thick SiO_2 deposition by plasma-enhanced chemical vapor deposition (PECVD), followed by lithography and a buffered oxide etch (BOE) to form a hard mask with slant sidewalls. A Cl_2 based inductively coupled plasma (ICP) dry etch at an ICP power of 250 W, an RIE power of 20 W and a pressure of 5 mTorr was used to define the mesa with slant sidewalls, which are transferred from the SiO_2 hard mask. The bottom diameter of the diode mesa ranges from 107 to 707 μm. The Pd/Ni/Pt (30/30/30 nm) circular anodes were formed on the p^{++} GaN layer, after which a SOG film of $\sim$200 nm was coated and cured at 425 °C for 30 mins. The anode electrodes were not alloyed purposely but the curing process for SOG affected the metal stack slightly. The transfer length measurement (TLM) shows that the contact resistance on p-GaN is about $1.6 \times 10^{-4}\Omega \cdot$cm^{-2}. Contact holes were subsequently formed by wet etch and a Ti/Al/Au stack was deposited to form the FP structure. Finally, a non-alloyed Ti/Al/Au (50/200/50 nm) electrode was formed on the rear surface of the GaN substrate.

For the device results shown in this letter, at least 3 devices of each type with BV>500 V were measured and the best device characteristics are shown since they best represent the potential of the GaN-on-GaN devices. *The bottom diameter of the mesa* is used to calculate the diode size unless otherwise noted. Substrates were not thinned.

III. Results and Discussion

Assuming a one-sided p+n junction since the Mg doping concentration in p-GaN is about 100$\times$ the Si doping concentration in n-GaN, the net doping concentration ($N_D - N_A$) in the n-GaN drift layer can be extracted from capacitance–voltage (C–V) measurements:

$$N_D - N_A = -\frac{2}{q\varepsilon_s} \frac{1}{d\left(1/C^2\right)/dV}, \quad (1)$$

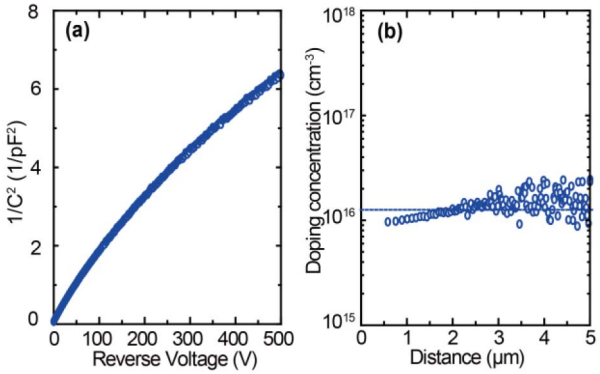

Fig. 2. (a) Measured $1/C^2$ versus reverse voltage up to 500 V in the GaN p-n diodes and (b) extracted carrier density profile in the n-GaN drift layer.

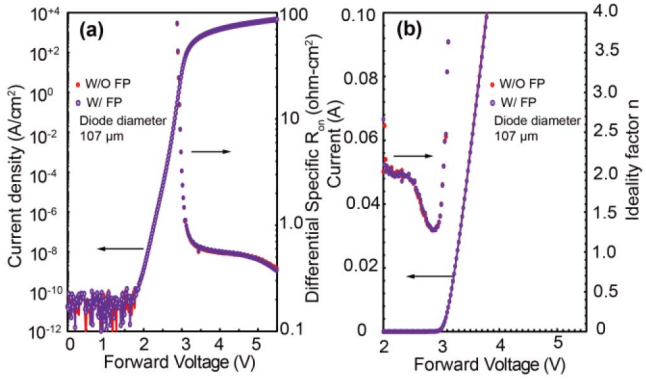

Fig. 3. Forward I-V characteristics of GaN p-n junction diodes w/ and w/o FP (a) in logarithm scale and R_{on} w/o considering lateral current spreading, and (b) in linear scale and the ideal factor of the diodes.

where N_D/N_A are donor/acceptor concentrations in n-GaN, q the electron charge and ε_s the permittivity of GaN. A representative plot of $1/C^2$ as a function of the reverse voltage up to 500 V on our p-n diodes is shown in Fig. 2(a) and the extracted net doping profile is shown in Fig. 2(b). In our n-GaN drift layer, $N_D - N_A$ is found to be around $1.0 \times 10^{16} \sim 1.2 \times 10^{16}$ cm^{-3}, which is comparable to the target Si concentration of 1-2 $\times$ 10^{16} cm^{-3}.

Figure 3 shows the representative forward I-V characteristics of the GaN p-n junction diodes with and w/o FP at room temperature, measured using a Keithley 4200 semiconductor analyzer. These GaN p-n diodes behave like a textbook p-n junction, sweeping a current range over 14 orders of magnitude. When V_f < 2 V, the diode current is too low to be measured by our equipment. For 2 V < V_f < 2.5 V, the diode ideality factor is nearly constant $\sim$2.0, suggesting a Shockley-Read-Hall (SRH) recombination dominated current. The ideality factor steadily drops to $\sim$1.3 near 2.8 V, signifying the ideal diode diffusion current overwhelms the SRH current in this bias window. The upturn of the ideality factor beyond 2.8 V is due to the effects of the diode series resistance. A careful analysis of temperature dependent I-Vs shows a SRH lifetime of $\sim$12 ns in our GaN p-n diodes [13]. The apparent turn-on voltage of the diodes is about 3.0 V, expected based on the GaN bandgap.

Using the mesa bottom-diameter of 107 μm, a differential specific on-resistance ($R_{on} = dV/dI$) of $\sim$0.4 m$\Omega \cdot$ cm^2

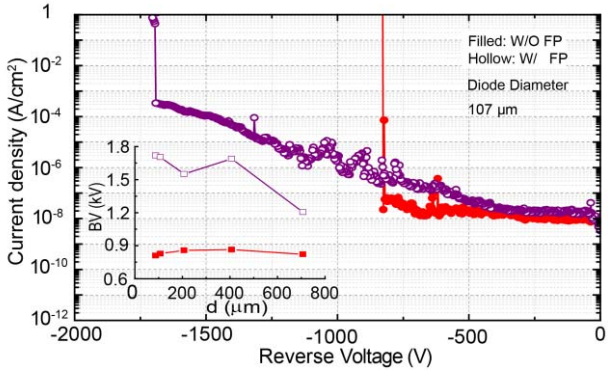

Fig. 4. Reverse *I-V* characteristics of GaN p-n diodes w/ and w/o FP.

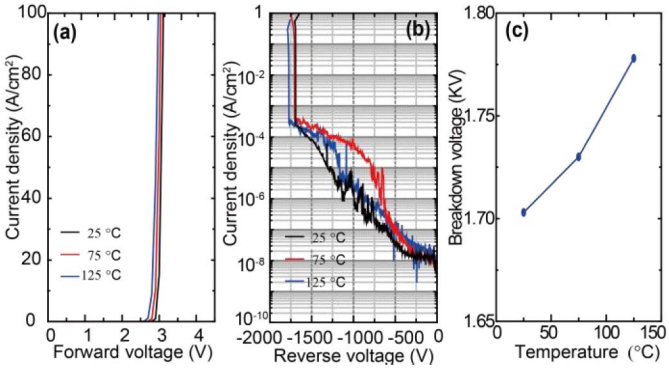

Fig. 5. (a) Forward, (b) reverse *I-V* characteristics and (c) *BV* as a function of temperature, all obtained on the same device, which can be measured repeatedly. The origin of the abnormal leakage current at 75 °C is yet unclear.

can be obtained at a current density ~3 kA/cm^2. TCAD simulations suggest a lateral current spreading up to 10 μm outward is possible in this current range [see similar results in Refs. [6], [9], [14]]. Considering a maximum radius increase by 10 μm due to current spreading, an effective diode diameter is thus 127 μm and the corresponding R_{on} is calculated to be 0.55 m$\Omega \cdot$cm^2. Using the TLM and Hall effect measurements on the p-GaN, the GaN substrate resistance and assuming an electron mobility of 1000 cm^2/V $\cdot$ s and a lateral current spreading of 10 μm in the n-GaN drift layer, all these resistance components sum up to be 0.64 m$\Omega \cdot$cm^2, which is slightly higher than the experimental value. The difference may be attributed to the underestimated electron mobility [9] or conduction modulation in p-n diodes [14], [15], demanding further studies.

Figure 4 shows the reverse *I-V* characteristics of the GaN p-n junction diodes w/ and w/o FP at room temperature, measured using Agilent B1505A power device analyzer with devices covered by Fluorinert. For diodes w/o FP, *BV* is ~830 V, showing a destructive failure near the mesa edge. For devices with FP, *BV* almost doubles, reaching 1706 V in diodes with a diameter of 107 μm. A slightly higher leakage at a higher reverse bias (>500 V) is most likely due to leakage path introduced by the FP process. The combination of *BV* of 1706 V and R_{on} of 0.55 m$\Omega \cdot$cm^2 leads to a high Baliga's figure of merit (V_B^2/R_{on}) of ~5.3 GW/cm^2 while taking into account of current spreading (~7.2 GW/cm^2 if the diode mesa size is used instead). This confirms that the field plate effectively suppresses the electric field crowding at the edge. It is interesting to notice in the Fig. 4 inset that the *BV* of devices w/o FP are nearly independent of the diode size while that of the devices with FP decreases with increasing diode diameter. This observation indicates that the dislocations present in these diodes (about 100/5,000 total in the 107/707 μm diodes) might be tolerable in delivering kV devices.

For an n-GaN drift layer with a thickness W of 10 μm and a net doping concentration $N_D - N_A$ of 1.2×10^{16} cm^{-3}, the *BV* and E_C of an ideal planar junction in this punch-through structure are related by

$$BV = E_c W - \frac{q(N_D - N_A)W^2}{2\varepsilon_s}. \quad (2)$$

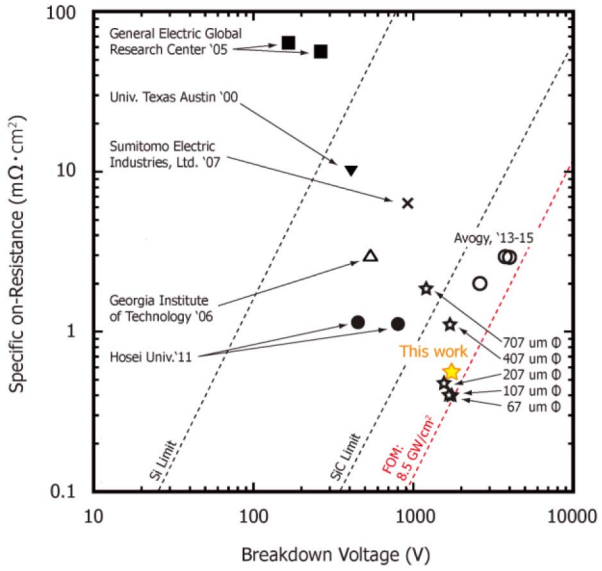

Fig. 6. Benchmark plot of *BV* versus R_{on} in reported GaN p-n diodes. The solid star is the result obtained in diodes with an effective diode diameter of 127 μm taking into account of the effect of current spreading. The hollow stars are the results using the diode mesa bottom-diameter to calculate R_{on}. The dotted lines are the unipolar limit, where a mobility of 1100 cm^2/Vs and E_C of 3.4 MV/cm are used for GaN.

Since it is impossible to reach the ideal breakdown of a planer junction without employing an ideal edge termination, we estimate the critical electric field using the same criteria reported in Ref. [6]. Assuming 75% of the entitled breakdown voltage is achieved in our devices, the critical electric field E_C is estimated to be >3.5 MV/cm, which is among the best of the reported GaN devices [1]–[9], [11]–[22].

Figure 5 shows the temperature dependent characteristics of the 107 μm GaN p-n diodes with FP. The forward turn-on voltage decreases with increasing temperature due to the exponentially increasing diffusion current with temperature. *BV* is observed to increase from ~1706 V at 25 °C to 1778 V at 125 °C, a signature of avalanche breakdown. The $R_{on} - BV$ benchmark plot for the reported GaN p–n diodes [5], [6], [9], [11], [17]–[22] is presented in Fig. 6. Similar to Ref. [14], a diode-size dependent R_{on} is observed, which merits further investigation.

IV. Conclusion

The textbook-like behavior in our GaN p-n power diodes, with avalanche capability demonstrated in this work, signifies the quality of epitaxial GaN is now on par with that of SiC while the performance and yield of large area power devices will most likely improve dramatically with further reduction of threading dislocations in bulk GaN substrates. Hence, this work places another landmark toward realizing true potentials of GaN-on-GaN for power electronics applications.

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