# Development of GaN Vertical Trench-MOSFET With MBE Regrown Channel

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***Abstract*— GaN vertical trench-MOSFETs incorporating molecular beam epitaxy (MBE) regrown channel are developed and investigated. The channel regrowth by MBE prevents repassivation of the p-type GaN body while promising higher channel mobility. Two different designs of the lateral portion of the regrown channel are compared: without or with an $n^+$-GaN buried layer. Without an $n^+$ buried layer, a respectable 600-V breakdown voltage (BV) is measured in the absence of edge termination, indicating a decent critical field strength (>1.6 MV/cm) of the regrown channel. However, the ON-resistance is limited by the highly resistive lateral channel due to Mg incorporation. With an $n^+$ buried layer, the limitation is removed. Excellent ON-current of 130 mA/mm and ON-resistivity of 6.4 $m\Omega \cdot cm^2$ are demonstrated. The BV is limited by high source–drain leakage current from the channel due to drain-induced barrier lowering (DIBL) effect. Device analysis together with TCAD simulations points out the major cause for the DIBL effect: the presence of interface charge beyond a critical value ($\sim 6 \times 10^{12}$ $cm^{-2}$) at the regrowth interface on etched sidewalls. This paper provides valuable insights into the design of GaN vertical trench-MOSFET with a regrown channel, where simultaneous achievement of low ON-resistivity and high BV is expected in devices with reduced interface charge density and improved channel design to eliminate DIBL.**

***Index Terms*— Drain-induced barrier lowering (DIBL), GaN, molecular beam epitaxy (MBE) regrowth, power electronics, regrown channel, trench-MOSFET, vertical power transistor.**

## I. Introduction

GaN is an attractive material for power electronic applications due to Baliga's figure of merit (BFOM) superior to SiC and Si. With the use of high-quality bulk GaN substrates in recent years, record high BFOM, fast switching speed and avalanche capability have been demonstrated in GaN vertical p-n diodes [1]–[7], suggesting high potential for three terminal power transistors. Compared with GaN lateral power HEMTs, vertical power transistors with p-type body have many advantages, such as higher power density, better device reliability, avalanche capability, and the presence of reduced surface field effect [8]. To date, vertical GaN power transistors in the literature can be characterized into two categories: gate-on-epi-surface (GoE) and gate-on-sidewall (GoS). In GoE devices, the gate is planar and parallel with the epitaxial surface, whereas in GoS devices, the gate conformally covers the trench sidewall where the channel is located. The GoE devices include current aperture vertical electron transistors (CAVETs) [9], [10] and vertical-diffused MOS (VDMOS)-like transistors [11], [12]. The GoS devices include UMOS or trench-MOSFETs with inversion channel [13]–[17] or regrown channel [18]–[22], as well as vertical fin MISFETs [23]–[25].

The vertical fin MISFET is relatively simple to fabricate. However, it does not have avalanche capabilities inherently due to the lack of a p-type GaN body. Besides, it is difficult to achieve sufficiently large threshold voltage ($V_{th}$). It is easier for UMOS to achieve normally-OFF operation, high breakdown voltage (BV), and small footprint without the need for selective-area doping. However, it is challenging to achieve high mobility in the inversion channel. In contrast, CAVETs, VDMOS-like transistors, and PolarMOS [9]–[12] utilize high mobility AlGaN/GaN channel to achieve low ON-resistivity ($R_{on}$) despite having an additional junction-gate-FET (JFET)-like drift region. However, the channel regrowth posts challenges in achieving low OFF-state leakage from the ungated regrowth junction interface. The absence of body contact as in CAVETs may avoid interface leakage but may also impact avalanche capability and $V_{th}$ stability.

Recently, a novel design based on trench-MOSFET is realized by metal-organic chemical vapor deposition (MOCVD) regrowth of a AlGaN/GaN or unintentionally doped (UID)-GaN channel conformally over the trench sidewall [18]–[21]. This concept promises higher channel mobility than traditional trench-MOSFETs due to less impurity scattering and smoother channel surface. Moreover, the GoS topology allows gate control of the regrowth interface, where high density of sheet charge $\sim 1 \times 10^{13}$ $cm^{-2}$ is typically found [15], [17], [20], likely due to etching damage and impurity gettering. The key issue with MOCVD

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regrown channel is that the buried p-GaN will be repassivated during the regrowth and needs to be reactivated; furthermore, in order to achieve an acceptable activation percentage of the acceptors, the buried p-GaN in the device active region needs to be exposed to the surface or at least within microns of an exposed surface during the high-temperature anneal. This leads to high thermal budget and limitations on device geometry. Furthermore, any incomplete activation of the buried p-GaN body leads to reduced BV.

Alternatively, if the channel is regrown by molecular beam epitaxy (MBE), no repassivation of buried p-GaN will happen in the absence of hydrogen-containing reactants. The lower growth temperature by MBE may also suppress Mg diffusion, which is observed in MOCVD regrown films [26]. Previously, we reported the first trench-MOSFET with MBE regrown UID-GaN channel, where a respectable BV of 600 V was demonstrated [22]. However, the ON-current ($I_{on}$) was relatively low and $V_{\text{th}}$ was unusually high (~18 V). In this paper, we seek to understand and resolve the previous issues of the MBE channel regrowth in the trench-MOSFETs while identifying new areas for improvement, by combining experiments and simulations. The previous limiting factor of the forward conduction is removed by the incorporation of an $n^+$-GaN buried layer under the lateral regrown channel, resulting in $>100\times$ improvement in $I_{on}$. Drain-induced barrier lowering (DIBL) effect is observed in the vertical regrown channel, which helps point to the significant influence of donorlike sheet charge on the regrowth interface. Finally, several approaches to reduce the interface charge are proposed.

## II. Device Fabrication

The starting epitaxial wafer is grown by MOCVD on a 2-in bulk n-type GaN substrate (SCIOCS COMPANY Ltd.,). It has a high-voltage p-n diode structure similar to our previous report [7], instead of an n-p-n structure to make sure the p-GaN can be readily activated. The p-GaN layer has a thickness of 400 nm and a Mg-doping concentration of $1 \times 10^{18}$ cm$^{-3}$, capped with a thin $p^{++}$ layer for p-type ohmic contact purpose. The 8-$\mu$m-thick $n^-$-GaN drift layer has a Si concentration of $\sim 1-2 \times 10^{16}$ cm$^{-3}$ and a net carrier concentration of $\sim 1 \times 10^{16}$ cm$^{-3}$ as determined from $C$–$V$ measurement. The p-GaN layer is activated *in situ* in the MOCVD chamber prior to device fabrication.

The schematic device cross sections are shown in Fig. 1. Two different designs of the lateral part of the channel with varying lengths $L_{\text{ch,lateral}} = 1-4$ $\mu$m are depicted: without [Fig. 1(a)] or with [Fig. 1(b)] an $n^+$-GaN buried layer underneath the UID regrown channel. The lateral channel portion exists due to the need to align the top ohmic contacts to the regrown channel and, ideally, should be eliminated to minimize the ON-resistivity of the device. In this paper, the lateral portion of the channel is also designed to enable the investigation on possible differences between regrowth on the c-plane in the lateral channel and regrowth on the etched semipolar plane in the vertical sidewall channel.

The process flow for the two designs without or with the $n^+$ buried layer differs only in the first step, where a 30-nm-thick

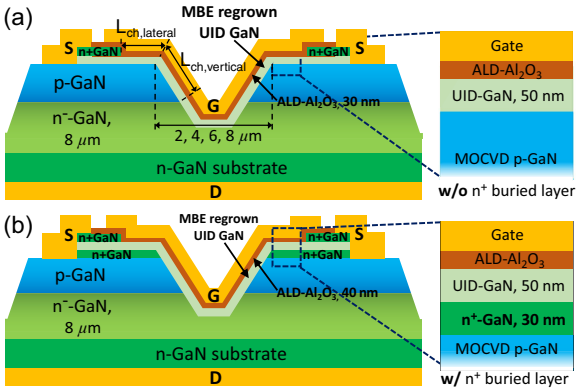



Fig. 1. Schematic cross section of two designs of the vertical GaN trench-MOSFETs incorporating MBE regrown UID-GaN channel. (a) Without and (b) with an $n^+$-GaN buried layer between the *lateral* part of the regrown UID-GaN channel and the p-GaN body.

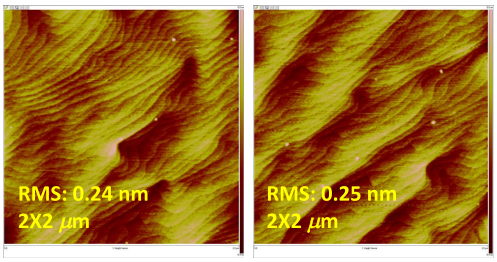



Fig. 2. AFM surface morphology of the MBE regrown UID-GaN channel on top of (left) epi surface (right) trench-bottom surface.

$n^+$-GaN is regrown by MBE on top of the p-GaN surface as the $n^+$ buried layer. The remaining processes are the same for both designs, as shown in [22]. The V-shaped trenches with designed widths of 2, 4, 6, and 8 $\mu$m are formed by our low damage inductively coupled plasma dry etch recipe [3] using a gas combination of Ar(10 sccm)/$BCl_3$(10 sccm)/$Cl_2$(20 sccm) and $SiO_2$ as mask. The etching depth is 250 nm into the drift layer and the sidewall angle is ~47° from the vertical as measured by atomic force microscopy (AFM). In order to reduce impurity concentration at the etched surface, a combination of UV-ozone cleaning and HF + HCl wet etch is performed before loading into the MBE chamber, where the UID-GaN channel layer with a nominal thickness of 50 nm is regrown. The V-shaped trench profile helps reduce shadowing effect during the channel regrowth, thus resulting in a rather uniform UID-GaN regrowth for both the lateral portion and the vertical portion of the device channel. As shown in Fig. 2, the MBE channel regrowth achieved smooth surface morphology with clear atomic steps on top of the epi surface as well as at the trench bottom. A patterned $n^+$-GaN regrowth is then performed for source ohmic contact purpose. In order to form body contact to the p-GaN, the regrown layers on top of the p-GaN are etched way, followed by device mesa isolation, all by the same trench etching recipe. After that, nonalloyed Pd/Au (50/50 nm) body contact and Ti/Au (50/100 nm) source ohmic contact metallization is realized by lift-off processes. The $Al_2O_3$ gate dielectric is deposited by atomic layer deposition, followed by Ni/Au (50/100 nm) gate electrode and nonalloyed Ti/Au (50/100 nm) drain electrode deposition.

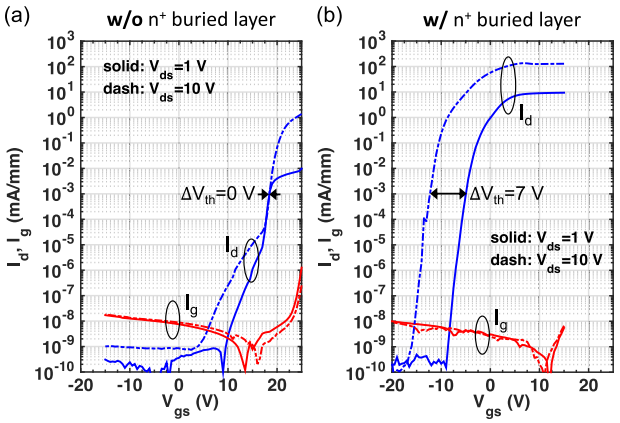



Fig. 3. Measured transfer $I$–$V$ characteristics of the trench-MOSFETs. (a) Without and (b) with the $n^+$ buried layer. The representative device in (a) has a trench width of 4 $\mu$m and $L_{ch,lateral} = 3$ $\mu$m. The representative device in (b) has a trench width of 8 $\mu$m and $L_{ch,lateral} = 1$ $\mu$m.

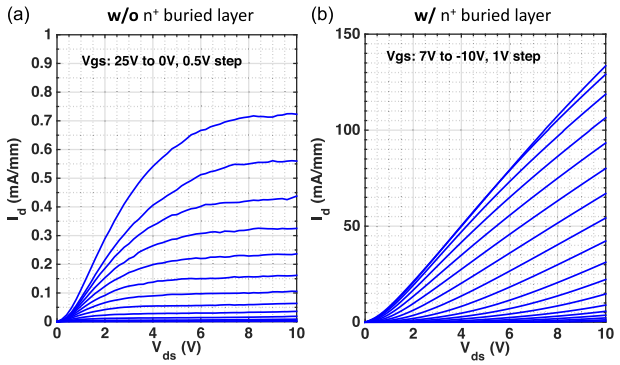



Fig. 4. Measured output $I$–$V$ characteristics of the trench-MOSFETs. (a) Without and (b) with the $n^+$ buried layer. The device dimensions are the same, as described in Fig. 3.

## III. Results and Discussion

The transfer $I$–$V$ characteristics and output $I$–$V$ characteristics of single gate-finger devices without or with the $n^+$ buried layer are shown in Figs. 3 and 4. The current is normalized by the finger/trench length, which is designed to be 50 $\mu$m. The device without the $n^+$ buried layer shows a decent ON–OFF ratio of $10^9$ at $V_{ds} = 10$ V and low source–drain and gate leakage current. A normally-OFF operation is observed with a threshold voltage of ~18 V defined at $I_d = 1$ $\mu$A/mm. No shift of the threshold voltage ($\Delta V_{th}$) with the increase of $V_{ds}$ is observed, indicating the absence of DIBL effect. The dispersion of low-level current below $3 \times 10^{-5}$ mA/mm is likely due to trapping effect in the channel. As shown in Fig. 4(a), a good saturation behavior is observed in the output characteristics. However, the ON-current ($I_{on}$) is lower than 1 mA/mm and the ON-resistivity ($R_{on}$) is extracted from the linear region to be 0.3 $\Omega \cdot$ cm$^2$ (normalized by the trench area), both of which are around two orders of magnitude inferior than the state-of-the-art performance.

As pointed out in our previous report [22], the relatively poor $I_{on}$ and $R_{on}$ were determined to be limited by the lateral part of the regrown UID channel, most likely due to Mg diffusion from the p-GaN underneath during the regrowth. The insertion of an $n^+$ buried layer underneath the lateral portion of the UID channel should help reduce the resistivity due to two reasons: 1) the added distance from the p-GaN to the regrown UID channel reduces the Mg incorporation into the UID film, due to the exponential decay of the Mg incorporation profile [26] and 2) the 30 nm $n^+$-GaN buried layer prevents the depletion of the UID channel due to the body p-GaN.

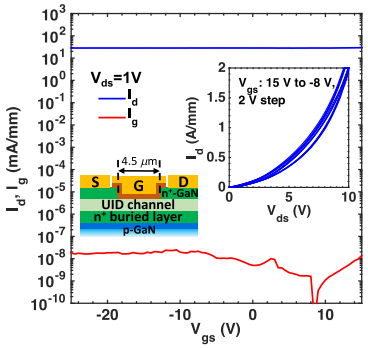



Fig. 5. Measured transfer and output $I$–$V$ characteristics of a planar test transistor fabricated on the same sample as the trench-MOSFETs with the $n^+$ buried layer. Inset: schematic device cross section.

Indeed, as shown in the transfer curves in Fig. 3(b), the device with the $n^+$ buried layer shows ~100× increase in the ON-current, resulting in an excellent ON–OFF ratio of $>10^{11}$ at $V_{ds} = 10$ V. A clockwise hysteresis of less than 2 V is observed. As shown in the family curves in Fig. 4(b), $I_{on}$ is 130 mA/mm at $V_{ds} = 10$ V and $R_{on}$ is extracted to be 6.4 m$\Omega \cdot$ cm$^2$ as normalized by the trench area, which are on par with the state-of-the-art performance. The nonlinearity at low $V_{ds}$ indicates that the source ohmic behavior is nonideal, although an excellent source metal contact resistance of 0.05 $\Omega \cdot$ mm is extracted from transmission line measurements. Detailed investigation of the nonlinearity is beyond the scope of this paper, but preliminary results from simulation show that the nonlinearity is due to a combination of Mg incorporation in the UID channel and the interface charge at the regrowth interface on the sidewall.

To verify that the lateral portion of the channel is indeed not limiting the ON-current, a planar test transistor with the same lateral channel design is measured on the same sample, as shown in Fig. 5. Although also limited by the imperfect source ohmic characteristics, the planar transistor shows much higher current than the trench-MOSFET, indicating that the lateral channel is not limiting the current of the trench-MOSFET. The planar transistor also shows an always on behavior with no clear gate modulation under the tested bias range. This is due to the high sheet charge density of the $n^+$ buried layer. It is estimated that the lateral channel and the source contact combined only contribute to ~5% of the total $R_{on}$ of the device, while the vertical channel contributes to ~90%.

In both designs, the lateral regrown channel is connected *in series* with the vertical regrown channel, and thus the overall $V_{th}$ is determined by the channel with higher $V_{th}$. In the device with the $n^+$ buried layer, the lateral channel is always on, and thus $V_{th}$ is determined by the vertical channel. At $V_{ds} = 1$ V, $V_{th} \sim -5$ V is extracted for the vertical channel. In the device

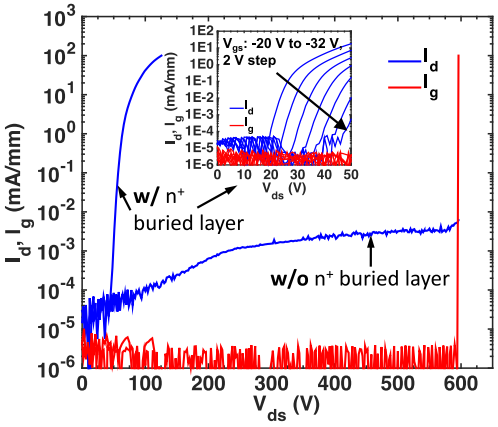



Fig. 6. Measured three-terminal breakdown characteristics of the regrown channel trench-MOSFETs; ~600-V BV and low drain leakage current are measured on the device without the $n^+$ buried layer at $V_{gs} = -15$ V. Soft breakdown behavior at ~130 V limited by drain leakage current is observed for the device with the $n^+$ buried layer. Inset: $V_{gs}$ dependence of the drain leakage current in the device with the $n^+$ buried layer.

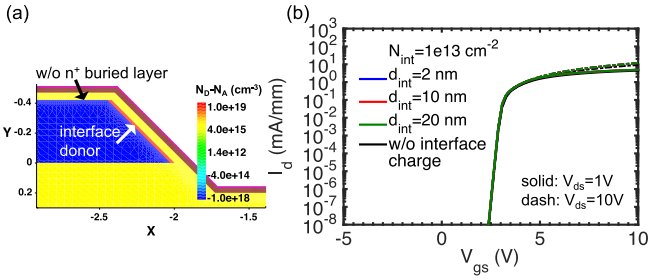



Fig. 7. (a) Simulation structure and net doping concentration of the device *without* the $n^+$ buried layer in the presence of interface donor sheet density. (b) Simulated transfer $I$–$V$ characteristics with $N_{int} = 1 \times 10^{13}$ cm$^{-2}$. Three different thicknesses of the interface donor region ($d_{int}$) are simulated: $d_{int} = 2, 10$, and 20 nm. Trench width = 4 $\mu$m. $L_{ch,\ lateral} = 1$ $\mu$m. Dielectric thickness = 40 nm. UID-GaN channel thickness: $d_{ch} = 50$ nm.

without the $n^+$ buried layer, the vertical channel should be the same as the other design, and thus $V_{th}$ of ~18 V must be determined by the lateral channel. The negative $V_{th}$ of the vertical regrown channel indicates the presence of extra donorlike states, most likely at the regrowth interface [27], since the ideal $V_{th}$ of the UID channel is ~3 V according to TCAD simulation [see Fig. 8(b)]. The higher than ideal $V_{th}$ in the lateral regrown channel means the presence of extra acceptors in the UID-GaN. Assuming no interface charge at the lateral regrowth interface on the c-plane, the acceptor concentration in the lateral regrown channel is estimated to be $\sim 2 \times 10^{19}$ cm$^{-3}$ from the analytical calculation of $V_{th}$. This is likely due to a high number of Mg atoms incorporated into the lateral channel during the regrowth on the top of the $p^{++}$-GaN layer [26], which has a Mg concentration of $> 1 \times 10^{20}$ cm$^{-3}$, as determined by secondary ion mass spectroscopy. If the $p^{++}$ layer is etched off before the channel regrowth, much lower Mg incorporation can be expected, which should allow a more reasonable $V_{th}$ and improved ON-current without using the $n^+$ buried layer design.

Two issues are observed in the ON-state characteristics of the device with the $n^+$ buried layer. First, a pronounced DIBL effect is shown in the transfer $I$–$V$ characteristics. The DIBL can be calculated by: DIBL $= \Delta V_{th}/\Delta V_{ds} = 0.8$ V/V. Second, there is no clear saturation behavior in the output characteristics, which is attributed to the combination of the nonlinear source ohmic characteristics and the DIBL effect. Since the hysteresis is much smaller than the observed $V_{th}$, the charging and discharging of trap states should not be the main cause of the DIBL. In Section IV, TCAD simulation is performed in order to investigate the causes of the DIBL effect.

The three-terminal breakdown characteristics are shown in Fig. 6. A respectable BV of ~600 V and low drain leakage are measured in the device without the $n^+$ buried layer, indicating good critical electrical field strength of the regrown channel ($> 1.6$ MV/cm) and the effective gate control over the interface charge at the vertical regrowth channel, thanks to the GoS design. During the measurement, $V_{gs} = -15$ V is applied to completely pinch off the vertical portion of the regrown channel, which has a lower threshold voltage than the lateral channel due to the presence of interface charge. In the device with the $n^+$ buried layer, soft breakdown behavior is observed due to the fast increasing drain leakage current, resulting in the limited BV of ~130 V. The inset shows the dependence of the drain leakage on $V_{gs}$. As the gate bias becomes more negative, the drain leakage reduces and the current profile shifts to the right. This is another indication of DIBL effect. The extracted DIBL is ~0.4 V/V at $I_{ds} = 1$ $\mu$A/mm, which is similar with the extraction from the transfer characteristics.

## IV. Simulation Study

In order to understand the causes of the DIBL effect observed in the device with the $n^+$ buried layer, simulation of the devices with or without the $n^+$ buried layer is performed in TCAD Sentaurus. Similar geometry along the critical current path as the fabricated devices is used in the simulator. The MBE-regrown UID channel is modeled as an ideal $n^-$-GaN film with a donor concentration of $1 \times 10^{16}$ cm$^{-3}$. The incorporation of Mg is not considered, since it will not contribute to the DIBL effect. The interface charge in the vertical channel is modeled as a thin sheet of interface donor [27], as shown in Figs. 7(a) and 8(a). The interface charge in the lateral channel on c-plane is not considered in this paper, since there is no clear evidence of its presence from the experimental results, and the concentration should be reasonably low [27]. Electron mobility of 30 cm$^2$/V · s is assigned to the UID channel considering the carrier scattering augmented by Mg incorporation in the regrown UID channel. This value is also consistent with the reported lower limit of the electron mobility in a similar regrown channel by Gupta *et al.* [28]. Electron mobility of 1500 cm$^2$/V · s is used in other n-type GaN regions.

Fig. 7(b) shows the simulated transfer $I$–$V$ characteristics of the device *without* the $n^+$ buried layer assuming a typical interface donor sheet density ($N_{int}$) of $1 \times 10^{13}$ cm$^{-2}$. As the depth of the crystal damage due to dry etch can extend to tens of nanometers, three different thicknesses of the interface donor

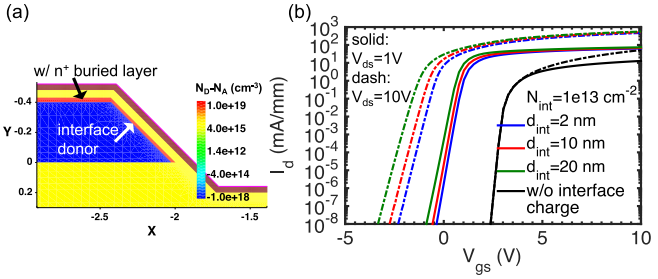



Fig. 8. (a) Simulation structure and net doping concentration of the device *with* the $n^+$ buried layer in the presence of interface donor sheet density. (b) Simulated transfer *I–V* characteristics with $N_{int} = 1 \times 10^{13}$ cm$^{-2}$. Three different thicknesses of the interface donor region ($d_{int}$) are simulated: $d_{int}$ = 2, 10, and 20 nm. ($n^+$ buried layer thickness = 30 nm; other dimensions are the same as the structure without $n^+$ buried layer. )

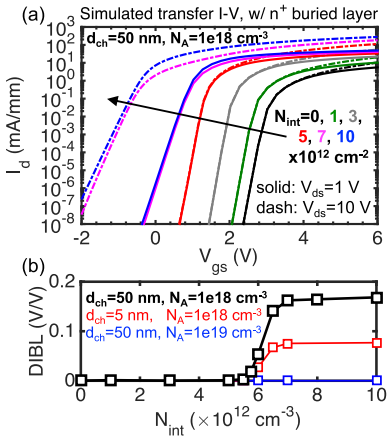



Fig. 9. (a) Simulated transfer *I–V* characteristics in device *with* the $n^+$ buried layer under different $N_{int}$ values. $d_{int}$ = 2 nm. UID-GaN channel thickness: $d_{ch}$ = 50 nm. Acceptor concentration in p-GaN: $N_A = 1 \times 10^{18}$ cm$^{-3}$. (b) Extracted DIBL versus $N_{int}$ under different $d_{ch}$ and $N_A$ values in p-GaN.

region ($d_{int}$) are simulated: $d_{int} = 2, 10, 20$ nm. In comparison with the device with no interface charge, the inclusion of $1 \times 10^{13}$ cm$^{-2}$ interface donor does not change $V_{th}$, regardless of $d_{int}$. The "local" $V_{th}$ of the vertical sidewall channel should be lowered by the interface charge; however, the observed $V_{th}$ of the whole device does not change. This means the threshold voltage of the whole device is determined by the lateral part of the channel, irrespective of the interface charge in the vertical channel. As a result, no DIBL effect is observed, in agreement with experimental measurements on the device without the $n^+$ buried layer. The lower $V_{th}$ in the simulation compared with experimental value is attributed to the absence of Mg incorporation into the UID channel in the simulated device.

Fig. 8(b) shows the simulated transfer *I–V* characteristics of the device *with* the $n^+$ buried layer under $N_{int} = 1 \times 10^{13}$ cm$^{-2}$. In comparison with the device with no interface charge, the inclusion of $1 \times 10^{13}$ cm$^{-2}$ interface donor shifts $V_{th}$ to lower values and increases the ON-current significantly. DIBL effect is clearly noticeable and increases with $d_{int}$. For $d_{int} = 2$ nm, $\Delta V_{th}$ of 1.5 V under $\Delta V_{ds} = 9$ V is extracted, corresponding to DIBL = 0.2 V/V. Since DIBL is absent when no interface charge density is present and increases with increasing $N_{int}$, the interface charge is identified as the major cause of the DIBL effect in the simulated devices with the $n^+$ buried layer.

Fig. 9(a) shows the simulated transfer *I–V* characteristics of the device *with* the $n^+$ buried layer under different $N_{int}$ values. The extracted DIBL values are plotted against $N_{int}$ in Fig. 9(b). The onset of DIBL is observed at $N_{int} \sim 6 \times 10^{12}$ cm$^{-2}$, where a sharp increase of DIBL is observed. Note that the active acceptor concentration ($N_A$) in Fig. 9(a) is set to be $1 \times 10^{18}$ cm$^{-3}$. If $N_A$ is lowered to $2 \times 10^{17}$ cm$^{-3}$, the DIBL increases from 0.17 to 0.41 V/V under $N_{int} = 1 \times 10^{13}$ cm$^{-2}$. On the other hand, if $N_A$ is increased to $1 \times 10^{19}$ cm$^{-3}$, the DIBL is no longer present. Alternatively, if the regrown channel thickness ($d_{ch}$) is reduced to 5 nm while keeping $N_A$ to be $1 \times 10^{18}$ cm$^{-3}$, the DIBL also decreases by more than 50%.

Physically, the interface charge weakens the channel back barrier provided by the p-GaN and introduces a parasitic channel under the UID channel, making the device more prone to DIBL effect especially when the channel length is not long enough in comparison with the channel-to-gate distance. If the back barrier is made stronger by higher $N_A$ in the p-GaN or the channel-to-gate distance is reduced by a thinner channel/gate dielectric, the DIBL effect due to the interface charge can be effectively suppressed, as shown in Fig. 9(b).

Based on the simulation results, the DIBL effect in the fabricated device incorporating the $n^+$ buried layer can be attributed to the presence of interface charge beyond a critical value ($\sim 6 \times 10^{12}$ cm$^{-2}$) at the regrowth interface on the vertical sidewall. The interface charge density is estimated to be $(1 \pm 0.3) \times 10^{13}$ cm$^{-2}$ based on the simulation results in Fig. 9(b) and the $V_{gs}$ swing required to completely pinch off the vertical channel [see Fig. 3(b)]. The simulated DIBL effect in the device with the $n^+$ buried layer is not as pronounced as observed in the experiments. One of the possible reasons is a lower active acceptor concentration than the apparent Mg concentration in MOCVD grown p-type GaN due to incomplete activation of the p-GaN or other compensation mechanisms. Another possible reason is a deeper and more extended interface charge region in the fabricated device than considered in the simulation ($d_{int} = 2 \sim 20$ nm). Other factors, such as trapping effect and body potential instability due to poor ohmic contact to the p-GaN [29], may also enhance the apparent measured DIBL.

The experiments and simulations suggest that the key to realizing normally-OFF and DIBL-free vertical regrown channel in trench-MOSFETs is the reduction of interface charge density at the regrowth interface. $N_{int}$ could potentially be reduced by the removal of surface damage due to dry etching by a hot tetramethylammonium hydroxide treatment [23], [30], [31]. High temperature annealing in $N_2/NH_3$ could also help reduce the interface donor density [20]. Even with a moderate amount of interface charge present, it is still possible to achieve normally OFF regrown channel without DIBL effect, as shown in Fig. 9. A thinner regrown channel and higher Mg concentration in the p-GaN could also mitigate the effect of the interface charge and increase $V_{th}$ [32]. Gupta *et al.* [20] employed

a Mg concentration of $3 \times 10^{19}$ cm$^{-3}$ in the p-GaN and a channel thickness of ∼5 nm in their MOCVD-regrown trench MOSFETs, in which $V_{th}$ of 3 V is achieved with no DIBL effect, even with an estimated $N_{int}$ around $8.5 \times 10^{12}$ cm$^{-2}$. In the absence of DIBL, much better breakdown characteristics are expected in the devices with the n$^+$ buried layer, since decent critical field strength of the MBE regrown channel has already been demonstrated in the device without the n$^+$ buried layer.

## V. Conclusion

GaN vertical trench-MOSFETs with MBE regrown UID-GaN channel are developed and investigated. The MBE regrowth avoids the need to reactivate the buried body p-GaN as is the case for MOCVD regrowth, while promises the same benefit on channel mobility. From a respectable BV of 600 V, decent critical field strength (>1.6 MV/cm) of the regrown channel is demonstrated. Mg incorporation in the lateral channel is identified as the limiting factor for $I_{on}$ and $R_{on}$ and could be much reduced if the p$^{++}$ capping layer is removed before the channel regrowth, or alternatively with an n$^+$ buried layer under the lateral channel. Excellent $I_{on}$ of 130 mA/mm and $R_{on}$ of 6.4 mΩ · cm$^2$ are demonstrated in the device incorporating the n$^+$ buried layer. However, prominent DIBL effect is observed and the BV is limited as a result. Device simulations help identify the major cause of the DIBL effect: the presence of interface charge beyond a critical value (∼$6 \times 10^{12}$ cm$^{-2}$) at the vertical regrowth interface. This paper provides valuable insights on how normally-OFF and DIBL-free vertical regrown channel can be achieved in MBE-regrown trench-MOSFETs, where simultaneous achievement of low ON-resistivity and high BV is expected.

## References


[1] I. C. Kizilyalli, T. Prunty, and O. Aktas, "4-kV and 2.8-mΩ-cm$^2$ vertical GaN p-n diodes with low leakage currents," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1073–1075, Oct. 2015.

[2] K. Nomoto *et al.*, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ-cm$^2$: A record high figure-of-merit of 12.8 GW/cm$^2$," in *IEDM Tech. Dig.*, Dec. 2015, pp. 7–9.

[3] K. Nomoto *et al.*, "1.7-kV and 0.55-mΩ·cm$^2$ GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016.

[4] H. Ohta *et al.*, "Vertical GaN p-n junction diodes with high breakdown voltages over 4 kV," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1180–1182, Nov. 2015.

[5] A. M. Armstrong *et al.*, "High voltage and high current density vertical GaN power diodes," *Electron. Lett.*, vol. 52, no. 13, pp. 1170–1171, Jun. 2016.

[6] D. Mauch *et al.*, "Ultrafast reverse recovery time measurement for wide-bandgap diodes," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9333–9341, Dec. 2017.

[7] Z. Hu *et al.*, "Near unity ideality factor and Shockley-Read-Hall lifetime in GaN-on-GaN *p-n* diodes with avalanche breakdown," *Appl. Phys. Lett.*, vol. 107, no. 24, p. 243501, 2015.

[8] W. Li *et al.*, "Design and realization of GaN trench junction-barrier-Schottky-diodes," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1635–1641, Apr. 2017.

[9] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and depletion mode AlGaN/GaN CAVET with Mg-ion-implanted GaN as current blocking layer," *IEEE Electron Device Lett.*, vol. 29, no. 6, pp. 543–545, Jun. 2008.

[10] S. Mandal *et al.*, "Dispersion free 450-V p GaN-gated CAVETs with Mg-ion implanted blocking layer," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 933–936, Jul. 2017.

[11] H. Nie *et al.*, "1.5-kV and 2.2-mΩ-cm$^2$ vertical GaN transistors on bulk-GaN substrates," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 939–941, Sep. 2014.

[12] H. G. Xing *et al.*, "Unique opportunity to harness polarization in GaN to override the conventional power electronics figure-of-merits," in *Proc. 73rd Annu. IEEE Device Res. Conf. (DRC)*, Jun. 2015, pp. 51–52.

[13] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates," *Appl. Phys. Exp.*, vol. 1, no. 1, pp. 011105-1–011105-3, Jan. 2008.

[14] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Exp.*, vol. 7, no. 2, p. 021002, 2014.

[15] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8mΩ cm$^2$ vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Exp.*, vol. 8, no. 5, p. 054101, 2015.

[16] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/1.7 Ω normally-off GaN vertical trench metal–oxide–semiconductor field-effect transistor," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1466–1469, Nov. 2016.

[17] C. Gupta *et al.*, "Comparing electrical performance of GaN trench-gate MOSFETs with a-plane and m-plane sidewall channels," *Appl. Phys. Exp.*, vol. 9, no. 12, p. 121001, 2016.

[18] M. Okada *et al.*, "Novel vertical heterojunction field-effect transistors with re-grown AlGaN/GaN two-dimensional electron gas channels on GaN substrates," *Appl. Phys. Exp.*, vol. 3, no. 5, pp. 054201-1–054201-3, Apr. 2010.

[19] D. Shibata *et al.*, "1.7 kV/1.0 mΩ cm$^2$ normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *IEDM Tech. Dig.*, Dec. 2016, pp. 1–10.

[20] C. Gupta *et al.*, "In situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET) on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 353–355, Mar. 2017.

[21] D. Ji *et al.*, "Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices," in *IEDM Tech. Dig.*, Dec. 2017, pp. 4–9.

[22] W. Li *et al.*, "600 V GaN vertical V-trench MOSFET with MBE regrown channel," in *Proc. 75th Annu. IEEE Device Res. Conf. (DRC)*, Jun. 2017, pp. 1–2.

[23] M. Sun, Y. Zhang, X. Gao, and T. Palacios, "High-performance GaN vertical fin power transistors on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 38, no. 4, pp. 509–512, Apr. 2016.

[24] Y. Zhang *et al.*, "1200 V GaN vertical fin power field-effect transistors," in *IEDM Tech. Dig.*, Dec. 2017, pp. 9.2.1–9.2.4.

[25] Z. Hu *et al.*, "GaN vertical nanowire and fin power MISFETs," in *Proc. 75th Annu. IEEE Device Res. Conf. (DRC)*, Jun. 2017, pp. 1–2.

[26] H. Xing *et al.*, "Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapor deposition," *Jpn. J. Appl. Phys.*, vol. 42, no. 1R, p. 50, 2003.

[27] Z. Hu *et al.*, "1.1-kV vertical GaN pn diodes with p-GaN regrown by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1071–1074, Aug. 2017.

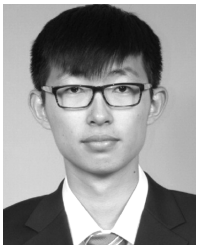
[28] C. Gupta, S. H. Chan, A. Agarwal, N. Hatui, S. Keller, and U. K. Mishra, "First demonstration of AlSiO as gate dielectric in GaN FETs; applied to a high performance OG-FET," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1575–1578, Nov. 2017.

[29] H. Xing, D. Jena, M. J. W. Rodwell, and U. K. Mishra, "Explanation of anomalously high current gain observed in GaN based bipolar transistors," *IEEE Electron Device Lett.*, vol. 24, no. 1, pp. 4–6, Jan. 2003.

[30] Y. Zhang *et al.*, "Origin and control of OFF-state leakage current in GaN-on-Si vertical diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015.

[31] Y. Zhang *et al.*, "Trench formation and corner rounding in vertical GaN power devices," *Appl. Phys. Lett.*, vol. 110, no. 19, p. 193506, May 2017.

[32] C. Gupta, S. H. Chan, Y. Enatsu, A. Agarwal, S. Keller, and U. K. Mishra, "A novel device design to lower the on-resistance in GaN trench MOSFETs," in *Proc. 74th Annu. IEEE Device Res. Conf. (DRC)*, Jun. 2016, pp. 1–2.



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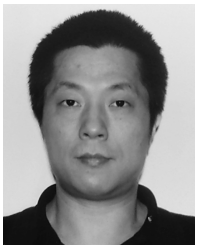

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