Steep Sub-Boltzmann Switching in AlGaN/GaN Phase-FETs With ALD VO_2

Amit Verma, Bo Song, Brian Downey, Virginia D. Wheeler, David J. Meyer, Huili Grace Xing, *Senior Member, IEEE*, and Debdeep Jena, *Senior Member, IEEE*

***Abstract*— We report the first demonstration of ultralow leakage AlGaN/GaN MOS-HEMTs on silicon substrates loaded at the source with atomic layer deposition (ALD)-grown VO_2 metal–insulator transition (MIT) material resistors. The resulting GaN phase-transition FET (phase-FET) shows steep sub-Boltzmann switching in its transfer characteristics in both sweep directions with slopes of ∼9.9 and ∼28.2 mV/decade at 60 °C. The control MOS-HEMTs and the phase-FETs show more than 12-order on/off ratio with ultralow off-state leakage. Because of the MIT, the drain current and the transconductance also show unconventional behavior. This first demonstration of ultralow leakage steep switching in GaN phase-FETs using integration-friendly ALD VO_2 opens the door to introducing new functionalities in nitride low-power digital devices, microwave circuits, photonic devices, and power electronics in the GaN-on-silicon platform.**

***Index Terms*— Atomic layer deposition (ALD), Boltzmann limit, GaN, hyper-FETs, phase-transition FET (phase-FETs), steep switching.**

I. Introduction

TO CONTINUE the march of Moore's law, an increasing number of non-Si materials such as high-k gate dielectrics and strained SiGe are now used in traditional CMOS technology [1], [2]. The III–V semiconductor heterostructures and 2-D materials are being explored for the next-generation devices and circuits [3]–[6]. Transition-metal oxide materials are also being investigated because they host many forms of electronic, structural, and magnetic phase transitions. Such phase transitions offer the potential to realize new device architectures and can help to overcome some of the fundamental limitations of traditional transistors, such as the ∼60 mV/decade Boltzmann limit of subthreshold switching at room temperature [7], [8]. Steep switching is currently being investigated by combining ferroelectric materials in the gate-stack of FETs to realize negative-capacitance FETs [9]. Another method is by loading the source electrode of Boltzmann FETs with materials exhibiting reversible metal–insulator transitions (MITs) to realize phase-transition FETs (phase-FETs/hyper-FETs) [10], [11]. Phase-FETs with steep switching and enhanced ON currents were proposed and demonstrated in 2015 by combining molecular beam epitaxy grown VO_2 with Si FETs [10].

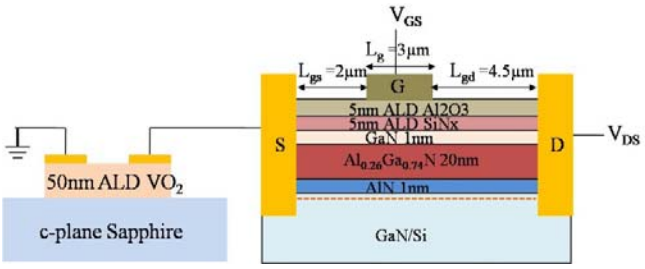

Fig. 1. Schematic of realized phase-FET. AlGaN/GaN MOS-HEMT on Si (right) loaded at the source with ALD VO_2 resistor (left: 2 μm × 100 μm).

VO_2 is an oxide material that undergoes a reversible temperature-driven structural and electronic MIT at ∼67 °C accompanied with up to five orders of magnitude change in resistivity [12]. This phase transition can also be induced electronically through an applied bias, or optically by excitation from a photonic source [10], [13]. Recently, we demonstrated steep switching in GaN FETs by combining atomic layer deposition (ALD) VO_2 with AlGaN/GaN HEMTs [14]. ALD VO_2 has the advantage of precise thickness control, film uniformity over large areas and conformal coating of complex 3-D surfaces [15]. Our initial demonstration had shown a marginal improvement in the slope of the transfer curves of GaN HEMTs with a slope of ∼59 mV/decade compared to the Boltzmann limit of ∼66 mV/decade at ∼60 °C, and suffered high gate leakage current under forward bias because of the use of Schottky gates. In addition, we had obtained sub-Boltzmann switching only in one scan direction of the gate bias [14]. In this paper, we overcome all these limitations by using AlGaN/GaN MOS-HEMTs with ultralow leakage fabricated on Si platform, loaded with ALD VO_2 resistor at the

Manuscript received October 4, 2017; revised December 3, 2017 and January 13, 2018; accepted January 15, 2018. Date of publication February 5, 2018; date of current version February 22, 2018. This work was supported in part by the Center for Low Energy Systems Technology, one of the six SRC STARnet centers sponsored by MARCO and DARPA, and in part by ONR MURI programs monitored by P. Maki and B. Bennett. The work at NRL was supported by the ONR. The review of this paper was arranged by Editor S. Rajan. *(Corresponding author: Amit Verma.)*

A. Verma was with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA. He is now with the Department of Electrical Engineering , IIT Kanpur, Kanpur 208016, India (e-mail: amitkver@iitk.ac.in).

B. Song is with the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA.

B. Downey, V. D. Wheeler, and D. J. Meyer are with the U.S. Naval Research Laboratory, Washington, DC 20375 USA.

H. G. Xing and D. Jena are with the Department of Materials Science and Engineering, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2018.2795105

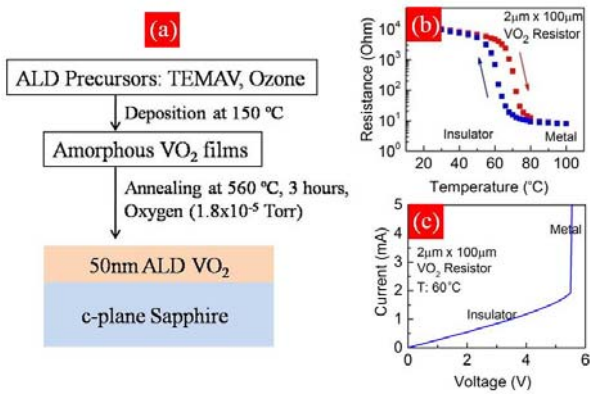

Fig. 2. (a) ALD process for VO_2. (b) Temperature-driven MIT of the ALD-grown VO_2 showing a >3-order change in resistance at ~67 °C with the direction of hysteresis indicated. (c) Applied bias-driven MIT in 2-μm-long, 100-μm-wide VO_2 resistor measured at 60 °C, showing a current threshold of ~2 mA for the insulator–metal phase transition.

source (Fig. 1). Because of the low leakage current, we are able to demonstrate steep switching in both sweep directions with slopes of ~9.9 and ~28.2 mV/decade at ~60 °C, far below the Boltzmann limit (~66 mV/decade), using ALD VO_2.

In Section II, we present the growth, fabrication, and characterization details of VO_2 resistors and AlGaN/GaN MOS-HEMTs. The device characteristics of the control MOS-HEMTs and the phase-FETs are presented and discussed in a comparative fashion in Section III. In Section IV, we present the summary of this paper and offer our perspectives on the prospects of this technology for new functionalities in GaN-based low-power and high-power electronics, RF electronics, and photonics.

II. ALD VO_2 Resistors and Nitride MOS-HEMTs

VO_2 thin films used in this paper were grown by ALD using Tetrakis-ethylmethylamino-vanadium (TEMAV) and ozone as the precursors, as shown in Fig. 2(a). Films of 50-nm thickness were grown on c-plane sapphire substrates. The as-deposited films were amorphous, but were crystallized upon annealing. More details about ALD VO_2 growth process and optimization can be found in [15] and [16]. Optical lithography was used to pattern the VO_2 resistors. Ti/Au ohmic contacts were deposited using e-beam evaporation followed by mesa-isolation using SF_6-based dry etching. VO_2 resistors of 100-μm width and lengths varying from 2–20 μm were fabricated. The measured temperature-driven MIT in the 2 μm × 100 μm VO_2 resistor is shown in Fig. 2(b). More than three-order change in resistance was measured when the layer went through the phase transition. The transition temperature was quite close to the bulk VO_2 MIT temperature (~67 °C) [12]. The measured applied bias-driven MIT in the 2 μm × 100 μm VO_2 resistor at 60 °C is shown in Fig. 2(c). The transition happens at an applied electric field of ~27 kV/cm and a current threshold of ~20 μA/μm. Though this transition can be achieved at room temperature, an elevated temperature of 60 °C was used to keep the transition voltage lower.

For the fabrication of the AlGaN/GaN MOS-HEMTs, the following epilayer structure (Fig. 1) was used: 1-nm GaN cap/20-nm $Al_{0.26}Ga_{0.74}N$ barrier/1-nm AlN spacer and a GaN channel on 1.3-μm semiinsulating GaN buffer grown on (111) Si substrates [17]. Ti/Al/Ni/Au (20/100/40/50 nm) metal stack annealed at 890 °C for 20 s in nitrogen ambient was used as the ohmic contact. The alloyed ohmic contacts showed low contact resistance of ~0.3 $\Omega \cdot$ mm. After mesa isolation (~300 nm), a gate dielectric stack of 5-nm SiN_x/5-nm Al_2O_3 was deposited using ALD followed by gate lithography and gate metal (40-nm Ni/100-nm Au) deposition. After the MOS-HEMT fabrication, a 2-D electron gas density of ~6.2×10^{12} cm^{-2} and electron Hall mobility ~1760 cm^2/V · s were measured at room temperature. The circuit symbol for MOS-HEMT device denoting the source (S), gate (G) and drain (D) terminals is shown in Fig. 3(a). The measured I_D–V_{GS} transfer characteristics and I_D–V_{DS} characteristics of this MOS-HEMT device at 60 °C are shown in Fig. 3(b)–(e). The pinch-off voltage in Fig. 3(b) is measured to be −5 V, and ON/OFF ratio of more than 12 orders was achieved as shown in Fig. 3(c). Gate leakage current was below the measurement limit. The subthreshold slope of the MOS-HEMTs at low current levels is ~90 mV/decade, not far from the Boltzmann limit of 66 mV/decade at 60 °C. Fig. 3(d) shows good current saturation in MOS-HEMTs and current densities of ~0.4 mA/μm.

III. Nitride Phase-FETs

To realize the GaN phase-FET, a 200-μm-wide MOS-HEMT with 3-μm gate length, 2-μm gate–source separation, and 4.5-μm gate–drain separation were used. The source of the GaN MOS-HEMT was loaded with the 2 μm × 100 μm VO_2 resistor, as shown in Fig. 1 and Fig. 3(f). The measured transfer characteristics of the phase-FET are shown in Fig. 3(g) and (h), and the I_D–V_{DS} characteristics are shown in Fig. 3(i). As mentioned earlier, all measurements were taken at 60 °C to keep the voltage threshold for VO_2 MIT low. Steep switching corresponding to the VO_2 insulator–metal transition (IMT) in the forward V_{GS} scan and the MIT in the reverse V_{GS} scan is clearly observed. Hysteresis is also observed in the transfer characteristics, as well as in the I_D–V_{DS} characteristics of the phase-FET because of the VO_2 phase transition.

The drain current is suppressed in the phase-FETs compared to MOS-HEMTs at low gate and drain bias. This can be clearly observed on comparing log(I_D) versus V_{DS} curves for MOS-HEMT and phase-FET devices, as shown in Fig. 3(e) and (j). This behavior is expected because of the additional source resistance. When VO_2 source resistor is in the insulating state, effective V_{GS} bias of MOS-HEMT ($V_{GS'}$) is reduced, leading to suppression of drain current. Even when the VO_2 resistor is in the metallic state at high drain/gate bias, it adds a small parasitic source resistance, reducing the intrinsic $V_{GS'}$ and $V_{DS'}$ bias, leading to reduction in the drain current. For example, at $V_{GS} = +2$ V and $V_{DS} = 10$ V, drain current in the MOS-HEMT is 427 μA/μm while in the phase-FET; the drain current value under these bias conditions decreases to 337 μA/μm. These results are consistent with the first demonstration of phase-FETs [10]. The apparent increase in the drain current of the phase-FET in [10] compared to the bare FET is because the results are plotted assuming iso-OFF condition (matched OFF-state current between bare FET and

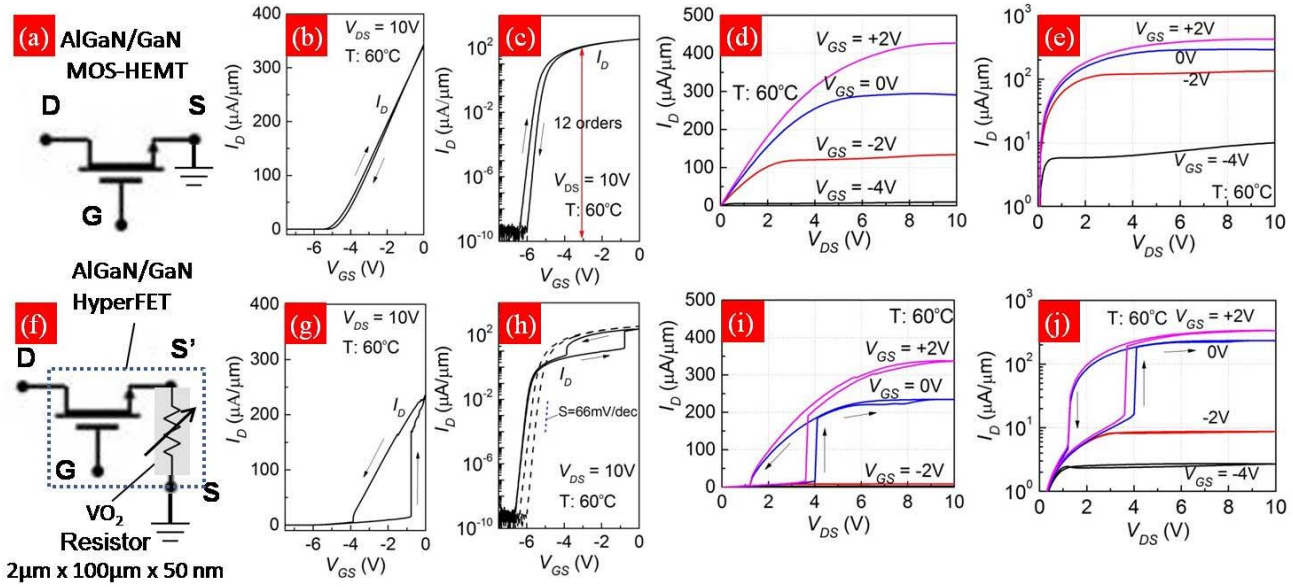

Fig. 3. (a) Circuit symbol for the stand-alone AlGaN/GaN MOS-HEMT device. The source is grounded, and control voltages are applied to the gate and drain contacts. (b) Linear I_D–V_{GS} transfer characteristics showing a threshold of ~ -5 V. (c) Logarithmic I_D–V_{GS} transfer characteristics showing 12-order on/off ratio. (d) and (e) Output I_D–V_{DS} characteristics of the MOS-HEMT device at 60 °C showing saturation. (f) Schematic circuit diagram of the VO_2 resistor-loaded MOS-HEMT device or the GaN phase-FET. (g) Linear I_D–V_{GS} transfer characteristics show a steep switching accompanied by hysteresis. (h) Logarithmic I_D–V_{GS} transfer characteristics show the appearance of the sub-Boltzmann switching regimes, and the ultralow off-state leakage of the GaN phase-FET. The transfer characteristics of the control MOS-HEMT structure is shown in dashed lines for comparison. (i) and (j) Output I_D–V_{DS} characteristics of the phase-FET device at 60 °C, showing that there is a threshold drain voltage for the drain current turn on with steep characteristics.

the phase-FET). The FETs used in [10] have a small ON/OFF ratio of ~2–3 orders of magnitude, thus adding VO_2 resistor in source lowers OFF current, and artificially gives enhanced drain currents when assuming iso-OFF condition (matched OFF-state current). The GaN MOS-HEMTs used in this paper have a large ON/OFF ratio of more than ~12 orders and extremely low OFF currents (less than $\sim 10^{-10}\mu$A/μm), thus adding VO_2 resistor in source has no effect on the OFF current.

In Fig. 3(i), beyond $V_{DS} = 4$ V, it can be observed that drain currents do not perfectly overlap in the forward and reverse sweeps even though VO_2 has transitioned into the metallic state. This behavior arises because VO_2 IMT/MIT is a first-order transition involving nucleation and growth of the opposite phase. During IMT transition metallic (rutile phase) domains nucleate and grow in size inside the insulating (monoclinic) phase matrix [18]–[20]. Once a conducting path is formed for current flow, VO_2 resistance falls sharply. At this stage, some insulating domains can still be present in VO_2, which gradually convert to metallic phase with increasing bias. During the reverse sweep, most of the sample is metallic, leading to lower resistance/higher current (compared to forward voltage scan) and gradually insulating domains nucleate and grow to cause the MIT. This phenomena lead to nonoverlapping forward and reverse sweep currents.

In the subthreshold region of the MOS-HEMT, small hysteresis can be observed depending on the V_{GS} sweep direction [Fig. 3(c)]. This hysteresis is not present in the phase-FET [Fig. 3(h)] which is likely because the gate oxide is stressed differently in the phase-FET during forward and reverse scans compared to the MOS-HEMT. Due to large voltage drop

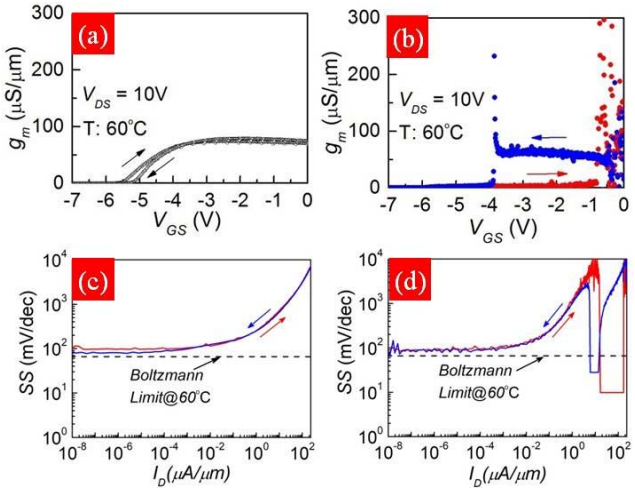

Fig. 4. Measured transconductance of (a) GaN MOS-HEMT and (b) GaN phase-FET as a function of gate bias. The GaN phase-FET has a much flatter g_m with hysteresis and peaks. The measured SS as a function of the drain current for (c) GaN MOS-HEMT and (d) GaN phase-FET device at 60 °C. The GaN MOS-HEMT has an SS larger than the Boltzmann limit. The GaN phase-FET shows sub-Boltzmann switching at high currents with I_D well in excess of 1 μA/μm.

across the VO_2 resistor in the insulating state (forward scan), the intrinsic $V_{GS'}$ is more negative compared to the intrinsic $V_{GS'}$ in the reverse scan when VO_2 is in the metallic state. This asymmetric gate oxide stress conditions can lead to different hysteresis behaviors in the phase-FET compared to the MOS-HEMT. Detailed investigation is needed for better understanding of this behavior.

Fig. 4(a) and (b) shows the measured transconductance (g_m) of both the GaN MOS-HEMT and the GaN phase-FET. The phase-FET shows a nearly square-shaped g_m with hysteretic behavior, and sharp peaks at the sub-Boltzmann gate voltage points. Square-shaped g_m is obtained in the phase-FET for positive to negative V_{GS} sweep as VO_2 MIT truncates the typical nonlinear part of the g_m curve near pinch off. The switching slopes (SSs) for the GaN MOS-HEMT and the phase-FET are shown in Fig. 4(c) and (d), respectively. While the MOS-HEMT SS remains above the Boltzmann limit, very steep slopes of ~9.9 and ~29.2 mV/decade are measured in the phase-FET in forward and reverse V_{GS} scans, respectively. These values are significantly lower than the Boltzmann limit of 66 mV/decade at 60 °C. SS values for the MOS-HEMT at similar drain current levels are ~720 mV/decade ($I_D \sim 10\ \mu A/\mu m$) and ~3200 mV/dec ($I_D \sim 100\ \mu A/\mu m$). The phase-FET sub-Boltzmann SS values represent a decrease of ~25× at $I_D = 10\ \mu A/\mu m$ and a decrease of more than ~300× at $I_D = 100\ \mu A/\mu m$. This experimental result is an initial proof of concept to access sub-Boltzmann limit modulation using ALD VO_2. To move the steep transition gate voltages to the subthreshold regime for low-power digital switching, and potentially for memory-logic hybrids, it will be necessary to match the device geometries and the VO_2 impedance [21]. This will also enable shaping of the hysteresis. The GaN phase-FET exhibits a record high $\sim 10^{12}$ ON/OFF ratio, which is attractive for low OFF-state leakage.

IV. Conclusion

In conclusion, we have demonstrated steep switching in ultralow leakage GaN phase-FETs realized by combining AlGaN/GaN MOS-HEMTs on Si with ALD VO_2. On-wafer integration of ALD VO_2 with GaN FETs [22], reducing hysteresis in phase-FETs, reducing VO_2 phase transition voltages at room temperature, and obtaining steep switching over larger drain current range will be the next steps toward realizing low-power GaN digital systems. VO_2 phase transition voltages can be reduced by scaling the lengths of VO_2 resistors to submicrometer regime [14], using strained VO_2 [23], [24] or by doping VO_2 [25], [26]. Several GaN device technologies beyond low-power digital can also benefit significantly from the technology demonstrated here. For example, low insertion loss, wideband VO_2 RF switches can directly be integrated with microwave transmission lines based on a GaN RF circuit platform [27], [28]. Integration with nitride LEDs and lasers can offer exciting potential for photonic triggering, reconfigurable mirrors, and plasmonics [29]–[31]. Finally, it can also enable new functionalities in GaN power electronics by offering new ways to realize lower ON-resistances and enhanced ON currents [10], [11].

References

[1] G. He and Z. Sun, *High-k Gate Dielectrics for CMOS Technology*. Hoboken, NJ, USA: Wiley, 2012.

[2] S. Datta *et al.*, "Advanced Si and SiGe strained channel NMOS and PMOS transistors with high-*k*/metal-gate stack," in *Proc. IEEE Meeting Bipolar/BiCMOS Circuits Technol.*, Sep. 2004, pp. 194–197, doi: 10.1109/BIPOL.2004.1365778.

[3] R. Chau, S. Datta, and A. Majumdar, "Opportunities and challenges of III–V nanoelectronics for future high-speed, low-power logic applications," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSIC)*, Oct./Nov. 2005, pp. 1–4, doi: 10.1109/CSICS.2005.1531740.

[4] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[5] F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," *Nanoscale*, vol. 7, pp. 8261–8283, Apr. 2015, doi: 10.1039/C5NR01052G.

[6] M. Chhowalla, D. Jena, and H. Zhang, "Two-dimensional semiconductors for transistors," *Nature Rev. Mater.*, vol. 1, Aug. 2016, Art. no. 16052, doi: 10.1038/natrevmats.2016.52.

[7] C. H. Ahn, J.-M. Triscone, and J. Mannhart, "Electric field effect in correlated oxide systems," *Nature*, vol. 424, no. 6952, pp. 1015–1018, 2003.

[8] Y. Zhou and S. Ramanathan, "Correlated electron materials and field effect transistors for logic: A review," *Critical Rev. Solid State Mater. Sci.*, vol. 38, no. 4, pp. 286–317, 2013, doi: 10.1080/10408436.2012.719131.

[9] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2007.

[10] N. Shukla *et al.*, "A steep-slope transistor based on abrupt electronic phase transition," *Nature Commun.*, vol. 6, Aug. 2015, Art. no. 7812, doi: 10.1038/ncomms8812.

[11] J. Frougier *et al.*, "Phase-transition-FET exhibiting steep switching slope of 8 mV/decade and 36% enhanced ON current," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573445.

[12] L. A. Ladd and W. Paul, "Optical and transport properties of high quality crystals of V_2O_4 near the metallic transition temperature," *Solid State Commun.*, vol. 7, no. 4, pp. 425–428, 1969, doi: 10.1016/0038-1098(69)90888-6.

[13] M. F. Becker, A. B. Buckman, R. M. Walser, T. Lépine, P. Georges, and A. Brun, "Femtosecond laser excitation of the semiconductor-metal phase transition in VO_2," *Appl. Phys. Lett.*, vol. 65, no. 12, pp. 1507–1509, 1994, doi: 10.1063/1.112974.

[14] A. Verma *et al.*, "Demonstration of GaN HyperFETs with ALD VO_2," in *Proc. 74th Annu. Device Res. Conf. (DRC)*, Jun. 2016, pp. 1–2, doi: 10.1109/DRC.2016.7548397.

[15] M. J. Tadjer *et al.*, "Temperature and electric field induced metal-insulator transition in atomic layer deposited VO_2 thin films," *Solid-State Electron.*, vol. 136, pp. 30–35, Oct. 2017, doi: 10.1016/j.sse.2017.06.018.

[16] A. C. Kozen, H. Joress, M. Currie, V. R. Anderson, C. R. Eddy, Jr., and V. D. Wheeler, "Structural characterization of atomic layer deposited vanadium dioxide," *J. Phys. Chem. C*, vol. 121, no. 35, pp. 19341–19347, 2017, doi: 10.1021/acs.jpcc.7b04682.

[17] B. Song *et al.*, "Ultralow-leakage AlGaN/GaN high electron mobility transistors on Si with non-alloyed regrown ohmic contacts," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 16–19, Jan. 2016, doi: 10.1109/LED.2015.2497252.

[18] M. M. Qazilbash *et al.*, "Mott transition in VO_2 revealed by infrared spectroscopy and nano-imaging," *Science*, vol. 318, no. 5857, pp. 1750–1753, 2007, doi: 10.1126/science.1150124.

[19] J. G. Ramírez, A. Sharoni, Y. Dubi, M. E. Gómez, and I. V. Schuller, "First-order reversal curve measurements of the metal-insulator transition in VO_2: Signatures of persistent metallic domains," *Phys. Rev. B, Condens. Matter*, vol. 79, no. 23, p. 235110, 2009, doi: 10.1103/PhysRevB.79.235110.

[20] J. Kim, C. Ko, A. Frenzel, S. Ramanathan, and J. E. Hoffman, "Nanoscale imaging and control of resistance switching in VO_2 at room temperature," *Appl. Phys. Lett.*, vol. 96, no. 21, p. 213106, 2010, doi: 10.1063/1.3435466.

[21] A. Aziz, N. Shukla, S. Datta, and S. K. Gupta, "Steep switching hybrid phase transition FETs (hyper-FET) for low power applications: A device-circuit co-design perspective—Part II," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1350–1357, Mar. 2017, doi: 10.1109/TED.2016.2642884.

[22] B. P. Downey, V. D. Wheeler, and D. J. Meyer, "Localized phase change of VO_2 films grown by atomic-layer deposition on InAlN/AlN/GaN heterostructures," *Appl. Phys. Exp.*, vol. 10, no. 6, p. 061101, 2017, doi: 10.7567/APEX.10.061101.

[23] Y. Muraoka and Z. Hiroi, "Metal–insulator transition of VO_2 thin films grown on TiO_2 (001) and (110) substrates," *Appl. Phys. Lett.*, vol. 80, no. 4, pp. 583–585, 2002, doi: 10.1063/1.1446215.
[24] N. B. Aetukuri *et al.*, "Control of the metal–insulator transition in vanadium dioxide by modifying orbital occupancy," *Nature Phys.*, vol. 9, no. 10, pp. 661–666, 2013, doi: 10.1038/NPHYS2733.
[25] K. L. Holman *et al.*, "Insulator to correlated metal transition in $V_{1-x}Mo_xO_2$," *Phys. Rev. B, Condens. Matter*, vol. 79, no. 24, p. 245114, 2009, doi: 10.1103/PhysRevB.79.245114.
[26] H. Takami, T. Kanki, S. Ueda, K. Kobayashi, and H. Tanaka, "Filling-controlled mott transition in W-doped VO_2," *Phys. Rev. B, Condens. Matter*, vol. 85, no. 20, p. 205111, 2012, doi: 10.1103/PhysRevB.85.205111.
[27] F. D. Bouchiat, C. Champeaux, A. Catherinot, A. Crunteanu, and P. Blondy, "RF-microwave switches based on reversible semiconductor-metal transition of VO_2 thin films synthesized by pulsed-laser deposition," *Appl. Phys. Lett.*, vol. 91, no. 10, p. 223505, 2007, doi: 10.1063/1.2815927.
[28] S. D. Ha, Y. Zhou, A. E. Duwel, D. W. White, and S. Ramanathan, "Quick switch: Strongly correlated electronic phase transition systems for cutting-edge microwave devices," *IEEE Microw. Mag.*, vol. 15, no. 6, pp. 32–44, Sep./Oct. 2014, doi: 10.1109/MMM.2014.2332422.
[29] G. Seo, B.-J. Kim, H.-T. Kim, and Y. W. Lee, "Photo-assisted electrical oscillation in two-terminal device based on vanadium dioxide thin film," *J. Lightw. Technol.*, vol. 30, no. 16, pp. 2718–2724, Aug. 15, 2012, doi: 10.1109/JLT.2012.2199466.
[30] Z. Yang and S. Ramanathan, "Breakthroughs in photonics 2014: Phase change materials for photonics," *IEEE Photon. J.*, vol. 7, no. 3, Jun. 2015, Art. no. 0700305, doi: 10.1109/JPHOT.2015.2413594.
[31] Y. Abate *et al.*, "Control of plasmonic nanoantennas by reversible metal-insulator transition," *Sci. Rep.*, vol. 5, p. 13997, Sep. 2015, doi: 10.1038/srep13997.

Amit Verma received the integrated M.Tech. degree in engineering physics from IIT (BHU) Varanasi, Varanasi, India, in 2010, and the Ph.D. degree in electrical engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2015.

He held a post-doctoral position at Cornell University, Ithaca, NY, USA. He then joined IIT Kanpur, Kanpur, India, where he is currently an Assistant Professor with the Department of Electrical Engineering.

Bo Song received the Ph.D. degree from the School of Electrical and Computer Engineering, Cornell University, Ithaca, NY, USA, in 2016.

He is currently a Device Characterization and Modeling Engineer with Analog Devices, Norwood, MA, USA.

Brian Downey received the bachelor's degree in engineering science and the Ph.D. degree in materials science and engineering from Pennsylvania State University, State College, PA, USA, in 2006 and 2011, respectively.

He is currently an Electronics Engineer with the U.S. Naval Research Laboratory, Washington, DC, USA.

Virginia D. Wheeler received the B.S. and Ph.D. degrees in material science and engineering from North Carolina State University, Raleigh, NC, USA, in 2005 and 2009, respectively.

She is currently a Materials Research Engineer with the U.S. Naval Research Laboratory, Washington, DC, USA.

David J. Meyer received the B.S. degree in electrical engineering, the M.S. degree in engineering science, and the Ph.D. degree in materials science and engineering from Pennsylvania State University, State College, PA, USA, in 2003, 2004, and 2008, respectively.

In 2014, he was promoted to Head of the Wide Bandgap Materials and Devices Section, U.S. Naval Research Laboratory, Washington, DC, USA.

Huili Grace Xing (S'01–M'03–SM'14) received the Ph.D. degree from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2003.

She is currently a Professor with the School of Electrical and Computer Engineering and the School of Materials Science and Engineering, Cornell University, Ithaca, NY, USA.

Debdeep Jena (M'03–SM'14) received the Ph.D. degree in electrical and computer engineering from the University of California at Santa Barbara, Santa Barbara, CA, USA, in 2003.

He is currently a Professor with the School of Electrical and Computer Engineering and the School of Materials Science and Engineering, Cornell University, Ithaca, NY, USA.