

A New Holistic Model of 2-D Semiconductor FETs

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Abstract—An analytical compact model for 2-D crystal FETs is proposed. It provides an explicit expression for the drain current as a function of the gate and drain voltages considering Fermi–Dirac statistics and drift-diffusion transport. The model is applicable to n-type or p-type symmetric and asymmetric double gate devices as well as single gate transistors. It is validated against experimental results and can be used to explore in a simple but accurate fashion the physics and the performance limits of 2-D crystal FETs.

Index Terms—2-D semiconductors, compact modeling, drift-diffusion transport, Fermi–Dirac (FD) statistics, FET.

I. INTRODUCTION

ALITTLE over a decade after the first demonstration of free-standing atomic planes of graphene [1], the family of 2-D materials has grown and includes already several tens of synthesized members [2]. Some of them, such as transition metal dichalcogenides or phosphorene, have been recently used as channel materials in FETs, being promising candidates to replace and/or augment silicon and III-V compounds in the near future [3]–[6]. In this context, the development of compact models for 2-D crystal FETs is essential to help in interpreting the experimental results and to provide simple but accurate expressions in circuit-level simulations. However, despite the huge spotlight on 2-D materials and the advances in synthesis and fabrication, not many works have addressed the 2-D FET compact modeling problem [8]–[10]. And when it has been done, they have, with the exception of the model in [11] and [12]—which is built on the capacitance network proposed in [8]—simplified carrier densities by systematically neglecting Fermi–Dirac (FD) statistics.

Here, we contribute to the modeling of 2-D FET physics, deriving an expression for the carrier density as a function of

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the gate and drain voltages using FD statistics. This expression is then used to obtain a simple and compact formula for the drain current in the drift-diffusion approach. Although the ballistic regime is expected to be the final operational limit of very short channel length 2-D FETs, drift-diffusive models explain well the state-of-the-art experiments and are expected to keep on playing a role in compact modeling in the future years before the transistor really achieves free-of-scattering channel lengths. An interesting discussion on the survival of the drift-diffusion approximation is indeed pointed out in [7], whereas a theoretical discussion on the range of validity of both approaches can be found in [13].

This paper is structured as follows. In Sections II and III, we describe the mathematical procedure to determine the carrier density and the drain current in a symmetric double gate n-type 2-D crystal FET. The extension of the procedure to asymmetric double gate, single gate, and/or p-type FETs is treated in Appendix I. In Section IV, the model is validated against experimental results; we demonstrate the necessity of FD statistics to accurately model the carrier density in the 2-D FET channel; and we show the potential of the proposed model to explore the performance of 2-D FETs looking at figures of merit like the ON–OFF ratio, the intrinsic delay time, or the power delay product (PDP). Finally, Section V summarizes the main contributions of the proposed model.

II. 2-D FET ELECTROSTATICS

A schematic depiction of the modeled 2-D crystal FET is shown in Fig. 1(a). The channel dimensions are specified by its length L and width W . The gate and drain voltages with respect to the source are denoted by V_{gs} and V_{ds} . For the sake of clarity, we have derived here the expressions for a symmetric double gate n-type device; but the extension to asymmetric or single gate and/or p-type transistors is straightforward and is covered in Appendix I. The two gates are electrically isolated from the channel by two insulating barriers characterized by the thicknesses t_b and dielectric constant ϵ_b , defining a total barrier capacitance $C_b = 2\epsilon_b/t_b$, where the factor 2 accounts for the double gate geometry.

Let us assume first $V_{ds} = 0$ V, so the Fermi level, E_F , is uniform along the channel. From an examination of the band diagram along the z -axis [see Fig. 1(b)], we get

$$(E_F - E_c(x)) + \chi_s - qV_b(x) - \phi_m = qV_{gs} \quad (1)$$

where ϕ_m is the metal work-function, χ_s is the semiconductor electron affinity, V_b is the voltage drop in the insulator, and E_c is the conduction band edge. Sufficiently far from the edge of

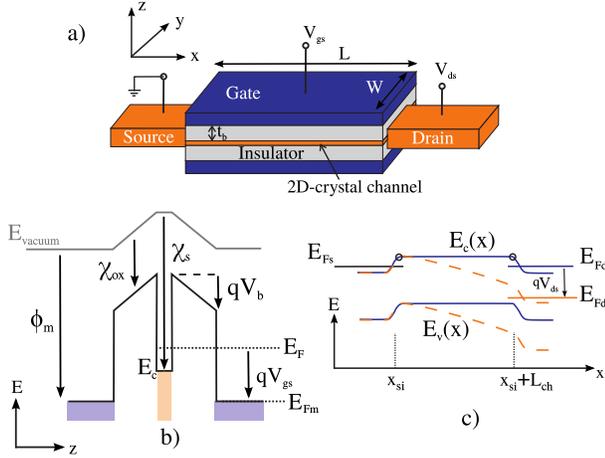


Fig. 1. (a) 2-D crystal semiconductor FET (b) Energy band diagram along the gate/insulator/channel direction (c) Energy band diagram along the source/channel/drain direction for different values of V_{ds} .

the source–channel and drain–channel junctions, the electric field is zero in-plane and purely vertical to the insulator. Thus, we can write $V_b(x) = \rho_s(x)/C_b$, where $\rho_s(x)$ is the local 2-D sheet charge density, given by $\rho_s(x) = -qn_s(x) + qp_s(x) + qN_d^+$, and n_s , p_s , and N_d^+ are the electron, hole, and ionized donor density. We can assume that all impurities are ionized and, therefore, $p_s(x) \ll n_s(x)$ in all regimes of operation. Substituting V_b in (1) and after some rearrangement, we get

$$q^2 n_s(x)/C_b + (E_F - E_c(x)) = qV_{gs} - qV_T \quad (2)$$

where the threshold voltage, identified as $V_T = \chi_s/q - \phi_m/q - qN_d^+/C_b$, accounts for the effect of the metal work function, the semiconductor affinity and the doping.

Then, if a nonzero V_{ds} is applied: 1) the Fermi level is no longer constant along the channel but becomes a position-dependent quasi-Fermi level E_{Fn} and 2) the conduction band edge bends down [see Fig. 1(c)], showing a maximum around the source–channel junction namely, at the source injection point (x_{si}). The source is, however, electron-rich and the current continuity with the channel requires that E_{Fn} change very little around x_{si} . As a consequence, $E_{Fn}(x_{si})$ can be assumed to be in equilibrium with the Fermi level at the source contact, E_{Fs} . In addition, if we assume a slow spatial charge variation along x compared with the insulator thickness, or equivalently that the control of the barrier capacitance, C_b , over n_s is much larger than the corresponding to the drain capacitance, we can still apply (2) to the right of x_{si} , i.e., to the channel. However, the gate-to-channel potential drop at a position x in the channel is no longer that of the source injection point ($qV_{gs} = E_{Fs} - E_{Fm}$), but a value $qV_{g-ch} = E_{Fn}(x) - E_{Fm}$. Therefore, (2) needs to be rewritten substituting qV_{gs} by qV_{g-ch} and E_{Fs} by $E_{Fn}(x)$. But we can easily write $qV_{g-ch} = qV_{gs} + E_{Fn}(x) - E_{Fs}$, what eventually allows us to write

$$q^2 n_s(x)/C_b + (E_{Fn}(x) - E_c(x)) = qV_{gs} - qV_T + E_{Fn}(x), \quad (3)$$

where the Fermi level at the source is assumed as reference for energies, i.e., $E_{Fs} = 0$. We can find an additional relation between n_s and $E_{Fn} - E_c$ from the 2-D crystal carrier density. Under a parabolic dispersion relationship modeled in the effective mass approximation using FD statistics

$$n_s(x) = D_0 kT \ln \left(1 + e^{\frac{E_{Fn}(x) - E_c(x)}{kT}} \right) \quad (4)$$

where $D_0 = g_v g_s (m_c^*/2\pi\hbar^2)$ is the 2-D density of states, with g_s and g_v the spin and valley degeneracies and m_c^* the conduction band effective mass. We can define a degenerated-quantum capacitance $C_{dq} = q^2 D_0$, that corresponds to the upper-limit achievable by the actual quantum capacitance, $C_q = dn_s/d(E_F - E_c)$, when the 2-D carrier density becomes heavily degenerated [16]. Accordingly, it is useful to define a degenerated-quantum carrier density: $n_q = C_{dq} V_{th}/q$, where $V_{th} = kT/q$ is the thermal voltage. Following a similar logic, we define a characteristic carrier density associated with the barrier capacitance: $n_b = C_b V_{th}/q$. Solving for $E_{Fn} - E_c$ in (4), using it in (3), and substituting the previous definitions of n_q and n_b , we can write after some algebra

$$e^{\frac{n_s(x)}{n_b}} \left(e^{\frac{n_s(x)}{n_q}} - 1 \right) = e^{\frac{V_{gs} - V_T + E_{Fn}(x)/q}{V_{th}}}. \quad (5)$$

This equation sets the relation between the carrier density, the gate voltage, and the quasi-Fermi level at point x in the channel, and we think of it as the heart of the compact modeling of 2-D crystal FETs. Although it is transcendental, it can be rewritten to a very good approximation to get explicit expressions for n_s in two limiting cases of V_{gs} .

For small values of V_{gs} , i.e., $[V_{gs} - V_T + E_{Fn}/q]/V_{th} \ll 0$, $n_s \ll n_b$, n_q , the exponential terms in the left-hand side of (5) can be expanded in the Taylor series, and retaining just the first-order n_s term, we get

$$n_{s,OFF}(x) \approx n_q e^{\frac{V_{gs} - V_T + E_{Fn}(x)/q}{V_{th}}} \quad (6)$$

resulting in the exponential relationship characteristic of the subthreshold regime. On the other hand, for large gate biases, i.e., $V_{gs} - V_T + E_{Fn}/q \gg V_{th}$, we get $n_s \gg n_q$, therefore, $e^{(n_s/n_q)} - 1 \simeq e^{(n_s/n_q)}$. Using the expressions for C_b and C_{dq} , and defining $C_g = (C_b^{-1} + C_{dq}^{-1})^{-1}$, (5) can be reformulated, after some algebra, as:

$$n_{s,ON}(x) \approx \frac{C_g}{q} [V_{gs} - V_T + E_{Fn}(x)/q] \quad (7)$$

establishing a linear relation between the carrier density in the channel and the gate voltage in the ON state.

III. DRAIN CURRENT MODEL

Equation (5) can be used to study the carrier transport in the device. In the diffusive regime, the current density is written as

$$J_d = -q n_s(x) \mu \frac{dE_{Fn}(x)/q}{dx} \quad (8)$$

where $\mu/q \cdot dE_{Fn}(x)/dx$ models the carrier velocity in the x -direction, with the mobility μ characterizing the scattering processes in the channel at low fields. Assuming that $dE_{Fn}(x)/dx$ is small compared with the vertical electric field,

the drain current can be written under the gradual channel approximation. If we neglect any changes in L having to do with the band-bending near the source–channel or drain–channel junctions and integrating with respect to x on both the sides of (8), we write

$$I_d = -q\mu \frac{W}{L} \int_{x_{si}}^{x_{si}+L} n_s(x) \frac{dE_{Fn}(x)}{q}. \quad (9)$$

Differentiating (5) with respect to n_s , we can write dE_{Fn}/q in terms of dn_s , and substituting it into (9), we get

$$I_d = -q\mu \frac{W}{L} V_{th} \int_{n_{s,si}}^{n_{s,di}} \left[\frac{\left(\frac{1}{n_b} + \frac{1}{n_q}\right) e^{\frac{n_s(x)}{n_q}} - \frac{1}{n_b}}{e^{\frac{n_s(x)}{n_q}} - 1} \right] n_s(x) \cdot dn_s(x) \quad (10)$$

where the integral limits $n_{s,si}$ and $n_{s,di}$ denote $n_s(x_{si})$ and $n_s(x_{si} + L)$, respectively. Equation (10) is analytically integrable (see Appendix II) and, after some algebra, results in a compact expression for I_d

$$I_d = q^2 \mu \frac{W}{L} \left[\left(\frac{n_{s,si}^2 - n_{s,di}^2}{2C_g} \right) + \frac{n_q^2}{Cdq} \left(e^{-\frac{n_{s,di}}{n_q}} - e^{-\frac{n_{s,si}}{n_q}} \right) \right] \quad (11)$$

where $n_{s,si}$ and $n_{s,di}$ can be obtained by solving (5) for $E_{Fn}(x_{si}) = 0$ and $E_{Fn}(x_{si} + L) = -qV_{ds}$, where following an equivalent reasoning as for the source contact, $E_{Fn}(x_{si} + L)$ is assumed to be equilibrium with the Fermi level at the drain contact, $E_{Fd} = -qV_{ds}$.

We can get even simpler expressions of I_{ds} in the OFF and ON states by using the explicit formulas for the carrier density calculated in Section II. Let us first consider the OFF state, defined as $V_{ds} \gg 0$ and $V_{gs} - V_T \ll 0$. Substituting (6) into (9) and neglecting the exponential term evaluated at $E_{Fn}(x_{si} + L) = -qV_{ds}$, we get

$$I_{ds}^{OFF} = q\mu V_{th} \frac{W}{L} n_q e^{\frac{V_{gs}-V_T}{V_{th}}} \quad (12)$$

which taking into account (6) can also be written as: $I_{ds}^{OFF} = q\mu V_{th}(W/L)n_{s,OFF}(x_{si})$. This formula could have also been derived from (11) by neglecting the quadratic terms and expanding in the Taylor series the exponential term. The OFF current is minimum when the crossover between n -type and p -type populations occurs in the channel. If the Fermi level is deep inside the bandgap (E_g), and $E_g \gg kT$, the 2-D carrier density can be approximated by $n_s \approx n_q e^{-E_g/2kT}$ [16], and therefore, the minimum achievable OFF current becomes $I_{ds}^{OFF,min} = q\mu V_{th}(W/L)n_q e^{-E_g/2kT}$. This, of course, assumes the source/drain contacts couple as efficiently to the holes in the valence band as to the electrons in the conduction band. Because this is in general not the case, the $I_{ds}^{OFF,min}$ above is a worst scenario, meaning the actual $I_{ds}^{OFF,min}$ will be lower than this value if gate leakage does not kick in.

The ON state is defined for $V_{ds} = V_{gs} - V_T \gg 0$. Using (7) in (9) and integrating it, the ON current reads

$$I_{ds}^{ON} = \mu \frac{W}{L} C_g (V_{gs} - V_T)^2. \quad (13)$$

Equivalently, from (7): $I_{ds}^{ON} = q^2 \mu (W/L)n_{s,ON}(x_{si})^2/2C_g$ that could have also been obtained from (11) by neglecting the exponential terms and using $n_{s,si} \gg n_{s,di}$.

IV. RESULTS AND DISCUSSION

The proposed model has been validated using the experimental results of the 2-D crystal FET presented by Fang *et al.* [4]. The reported device consisted of a p -type monoatomic channel of WSe₂ on 270 nm of SiO₂ isolating it from a doped-Si back-gate, and covered by 17.5 nm of ZrO₂ acting as a barrier of a top Pd gate. The extension of the equations presented in Sections II and III to an asymmetric p -type device is straightforward and is discussed in Appendix I. As reported in the experimental work, we assumed $12.5\epsilon_0$ and $3.9\epsilon_0$ as the dielectric constants of ZrO₂ and SiO₂, respectively (with ϵ_0 the vacuum permittivity), and a constant hole mobility in the WSe₂ channel of $235 \text{ cm}^2/\text{Vs}$, whereas a back-gate voltage of -40 V was applied [4]. $V_{Tt} = 1.4 \text{ V}$ and $V_{Tb} = 0 \text{ V}$ threshold voltages have been considered for the top and back gates, respectively. The channel length is $L = 9.4 \mu\text{m}$ and the current is normalized by the channel width. The maximum of the valence band of WSe₂ happens to be at the K point of the hexagonal Brillouin zone of WSe₂ with an effective mass of $m_v^* = 0.44 m_0$ [14], with m_0 the electron mass.

Fig. 2 shows the model (lines) and experiment (symbols) transfer and output characteristics for several values of V_{ds} and V_{gs} . The model is able to reproduce to a very good agreement the experimental results. In the transfer characteristic, the nearly ideal subthreshold swing (SS) of the experimental device is captured by the model without the necessity of traps modeling. Indeed, one of the most promising advantages of 2-D material channels FETs is the expected low density of dangling bonds due to the weak Van der Waals interactions between the 2-D channel and the deposited oxides [15]. Some approaches have been proposed for the inclusion of interface traps and their degrading effects on the SS in compact modeling (and could be applied to the proposed model), but they lead to numerical integrations of the current [9]. In the output characteristic, the model explains the experimental results accurately in both linear and saturation regions. For $V_{gs} = 1.7 \text{ V}$, the model slightly overestimates the drain current, what can be explained by the degradation of the experimental mobility due to ionized impurities or phonons [17], [18] not considered in the model. The mobility dependence on the gate and drain electric fields can be included in the model by semiempirical approaches as those proposed in [12] at the cost of introducing numerical calculations.

The proposed model can, therefore, be of help for experimentalists by providing them rigorous but concise theoretical support and for compact modeling designers by giving simple but accurate expressions for the drain current. In addition, it provides insights into the physics and the theoretical performance limits of devices. For example, one can determine the variation of the carrier density, the conduction band (or valence band) edge, and the Fermi level along the channel. To do it, given V_{gs} and V_{ds} , first I_{ds} and $n_{s,si}$ are determined

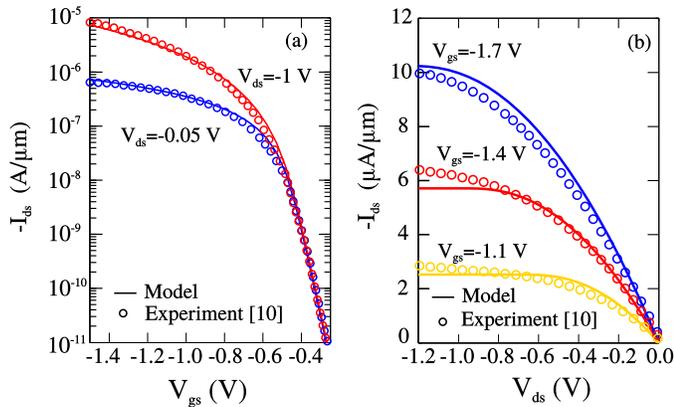


Fig. 2. Validation of the 2-D FET model results against the experimental device built by Fang *et al.* in [4]. (a) Transfer characteristic for $V_{ds} = -0.05$ V and $V_{gs} = -0.01$ V. (b) Output characteristic for several values of V_{gs} : -1.1 V, -1.4 V, -1.7 V.

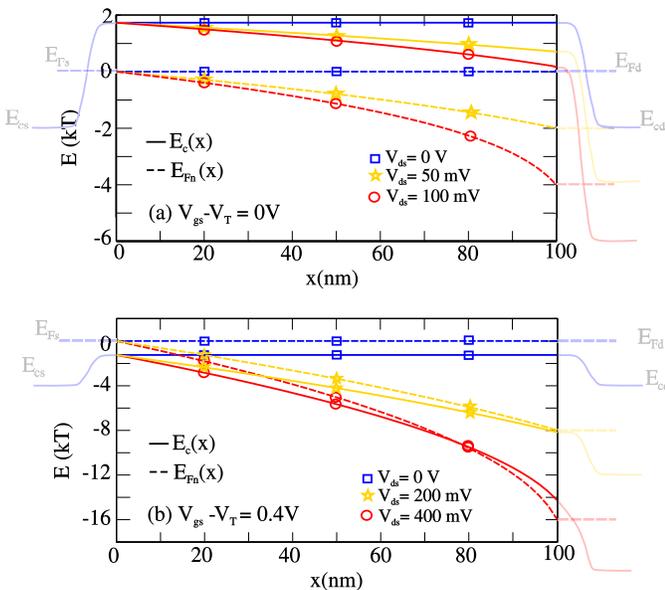


Fig. 3. Conduction band edge, E_c , (solid lines) and quasi-Fermi level, E_{Fn} , (dashed lines) along the channel for: (a) $V_{gs} - V_T = 0$ V and (b) $V_{gs} - V_T = 0.4$ V, and different values of V_{ds} , for a double gate n -type FET with $m_c = 0.5m_0$, $g_v = 2$, $t_b = 2$ nm, $\epsilon_b = 3.9\epsilon_0$, $\mu = 200$ cm²/Vs, and $L = 100$ nm. The drain and source regions are just depicted as a guide for the eyes in lighter colors assuming doping concentrations in these regions of $N_d = 2.1 \times 10^{13}$ cm⁻².

using (11) and (5). The current continuity in the channel imposes that I_{ds} must be constant even if the integral limits in (10) are modified, meaning that $I_{xs} = I_{ds}$, where I_{xs} stands for the current integrated between $x_{s,si}$ and x . I_{xs} would read as I_{ds} in (11) by substituting $L \rightarrow x$ and $n_{s,di} \rightarrow n_s(x)$. Since $I_{xs} = I_{ds}$ and $n_{s,si}$ are known, the modified (11) can then be used to find $n_s(x)$ for any given x along the channel. Once $n_s(x)$ is determined, (5) can be solved for $E_{Fn}(x)$, and finally $E_c(x)$ can be calculated with (4). In Fig. 3 we have applied this procedure to determine $E_c(x)$ and $E_{Fn}(x)$ along the channel of a 2-D crystal double gate symmetric n -type FET with $m_c = 0.5m_0$, $g_v = 2$, $t_b = 2$ nm, $\epsilon_b = 3.9\epsilon_0$, $\mu = 200$ cm²/Vs, and $L = 100$ nm at two different gate biases: 1) $V_{gs} - V_T = 0$ V and 2) $V_{gs} - V_T = 0.4$ V. Several values of V_{ds} has been considered in each case. The drain

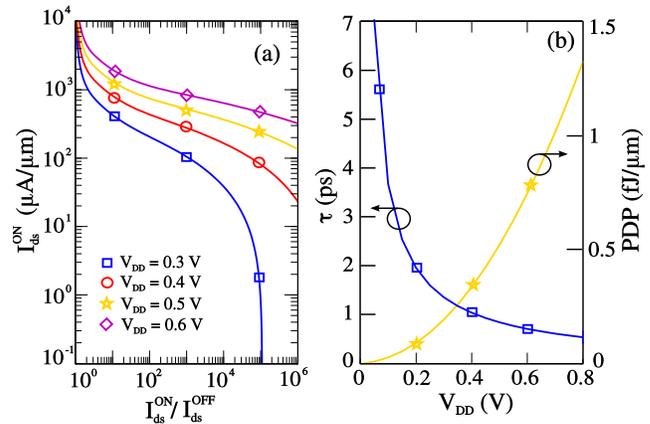


Fig. 4. $I_{ON} - I_{OFF}$ ratio versus I_{ON} current for different supply voltages, V_{DD} , and (b) PDP and intrinsic delay time (τ) versus supply voltage for a double gate n -type FET with $m_c = 0.5m_0$, $g_v = 2$, $t_b = 2$ nm, $\epsilon_b = 3.9\epsilon_0$, $\mu = 200$ cm²/Vs, and $L = 100$ nm.

and source regions have been sketched in light colors just as a guide for eyes, assuming a source/drain doping density of $N_d = 2.1 \times 10^{13}$ cm⁻². From Fig. 3 it can be stated that Maxwell-Boltzmann (MB) distribution is valid in the sub-threshold regime with $E_{Fn}(x) \ll E_c(x)$ by several kT values. But MB is inaccurate above threshold, where $E_{Fn}(x) \gg E_c(x)$, making it mandatory to use FD statistics as proposed in this paper (for $E_{Fn} = E_c$, MB already overestimates the real FD occupation by a factor of 2). The need of the FD distribution has been checked for a wide variety of insulator barriers and semiconductor materials and gate voltages. Increasing the gate electrostatic control by augmenting C_b results in a deeper movement of the Fermi level inside the conduction band and makes even more indispensable the use of correct FD statistics.

Regarding the application of the model to explore the performance of 2-D crystal FETs, it can be used to get estimations of the most relevant figures of merit of the transistor, and therefore to identify the design constraints related to, e.g., the device switching immunity, power consumption, or speed. Fig. 4 exemplifies this possibility showing: 1) the $I_{ds}^{ON} - I_{ds}^{OFF}$ ratio versus I_{ON} current for different supply voltages, V_{DD} , and 2) the PDP and intrinsic delay time (τ) versus V_{DD} , for the double gate symmetric FET discussed before. In Fig. 4(a), I_{ds}^{ON} is defined as I_{ds} at $V_{ON} = V_{OFF} + V_{DD}$, and I_{ds}^{OFF} is I_{ds} for a varying $V_{gs} = V_{OFF}$. The intrinsic delay time and the PDP are defined as $\tau = (Q_{ON} - Q_{OFF})/I_{ds}^{ON}$ and $PDP = V_{DD} I_{ds}^{ON} \tau$, where Q_{ON} and Q_{OFF} are the total carrier concentration in the channel in the ON and OFF states that can be obtained, as previously explained, integrating $n_s(x)$ along the channel length and multiplying by the width W . For the proposed example, due to the low carrier mobility considered, the device comply only partially with the ITRS requirements for high-performance applications in the 2021 node, set to $I_{ON}/I_{OFF} \geq 2.9 \times 10^4$ A/A at $I_{ON} = 2.9$ mA/ μ m, $\tau \leq 1.29$ ps, and $PDP \leq 2.44$ fJ/ μ m [19]. Thus, the model allows to find quick but quantitative insight into the physics of 2-D crystal FETs, as well as to easily evaluate them against the demands of the future technology nodes.

V. CONCLUSION

We have presented, in a simple mathematical procedure, a new compact equation governing the electrostatics of 2-D crystal FETs. This equation has then be used to obtain an analytical explicit expression of the drain current under drift-diffusion transport. The necessity of using FD statistics for the proper modeling of the carrier density in the channel in 2-D transistors has been demonstrated. The model has been validated with experimental results showing excellent agreement. It can be helpful to the experimental as well as to the compact modeling communities to gain easy insight in the 2-D crystal FET physics and to identify the main design constraints in these devices.

APPENDIX I

For asymmetric-double-gate 2-D FETs as well as for single-gate 2-D FETs, a few changes must be considered in the electrostatic model. To guide the derivation, Fig. 5 shows the energy band diagram across the top-gate/top-insulator/channel/bottom-insulator/bottom-gate structure of a n -type asymmetric-double-gate FET. We have also depicted in Fig. 5 the sheet carrier densities at the gates and at the 2-D crystal channel. The different variables defined in the figure keep the notation introduced in the main text, but they include t or b subindices to denote the top and bottom part, respectively.

In order to preserve the charge neutrality in the device, we must write

$$n_s = p_{tg} + p_{bg} \quad (14)$$

where p_{tg} and p_{bg} stand for the sheet carrier densities at the top and back gates. Assuming that the electric field is zero in-plane and purely vertical to the insulator: $qp_{tg} = V_{bt}\epsilon_{bt}/t_{bt}$ and $qp_{bg} = V_{bb}\epsilon_{bb}/t_{bb}$. From an examination of the band diagram in Fig. 5(b) and following the same reasoning as in the main text to derive (1) and (3), we can write at a point x in the channel:

$$\begin{aligned} (E_{Fn}(x) - E_c(x)) + \chi_s - qV_{bt}(x) - \phi_{tm} &= qV_{tg} + E_{Fn}(x) \\ (E_{Fn}(x) - E_c(x)) + \chi_s - qV_{bb}(x) - \phi_{bm} &= qV_{bg} + E_{Fn}(x). \end{aligned} \quad (15)$$

Solving (15) for V_{bt} and V_{bb} , using them in p_{tg} and p_{bg} , and substituting into (14), it reads

$$\begin{aligned} n_s = \frac{C_{bt} + C_{bb}}{q^2} [E_{Fn}(x) - E_c(x)] + \frac{C_{bt}}{q} \left(V_{tg} - V_{Tt} + \frac{E_{Fn}(x)}{q} \right) \\ + \frac{C_{bb}}{q} \left(V_{bg} - V_{Tb} + \frac{E_{Fn}(x)}{q} \right) \end{aligned} \quad (16)$$

where we have introduced the top, $C_{bt} = \epsilon_{bt}/t_{bt}$, and back, $C_{bb} = \epsilon_{bb}/t_{bb}$, barrier capacitances, and the top and back gate threshold voltages, $V_{Tt} = \chi_s/q - \phi_{tm}/q$, and $V_{Tb} = \chi_s/q - \phi_{bm}/q$. As in the main body, we can make use of (4), to write

$$\begin{aligned} q \frac{n_s(x)}{C_{bt} + C_{bb}} = V_{th} \ln(e^{n_s(x)/n_q} - 1) + \frac{C_{bt}}{C_{bt} + C_{bb}} (V_{tg} - V_{Tt}) \\ + \frac{C_{bb}}{C_{bt} + C_{bb}} (V_{bg} - V_{Tb}) + \frac{E_{Fn}(x)}{q} \end{aligned} \quad (17)$$

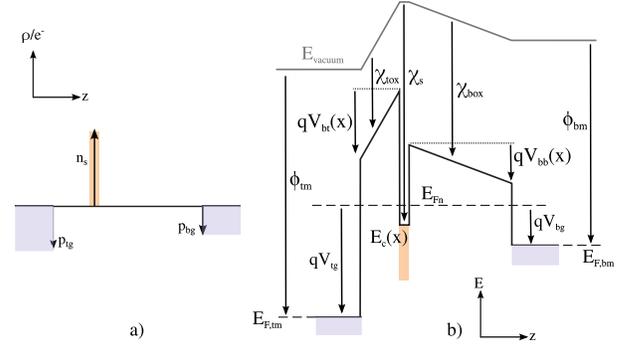


Fig. 5. Sheet carrier densities and conduction band energy diagram along the top-gate/top-insulator/channel/bottom-insulator/bottom-gate direction for n -type asymmetric double gate FET.

where we recall the definition of the degenerated-quantum carrier density, n_q . Similarly, defining a characteristic carrier density associated with the top and bottom barrier capacitances: $n_{bt} = C_{bt}V_{th}/q$ and $n_{bb} = C_{bb}V_{th}/q$, and after some algebra

$$e^{\frac{n_s(x)}{n_{bt} + n_{bb}}} \left(e^{\frac{n_s(x)}{n_q}} - 1 \right) = e^{\alpha \left(\frac{V_{tg} - V_{Tt}}{V_{th}} \right) + \beta \left(\frac{V_{bg} - V_{Tb}}{V_{th}} \right) + \frac{E_{Fn}(x)}{qV_{th}}} \quad (18)$$

where for the sake of clarity, we write $\alpha = (C_{bt}/(C_{bt} + C_{bb}))$, and $\beta = (C_{bb}/(C_{bt} + C_{bb}))$. Equation (18) is the equivalent to (5) in the case of asymmetric double gate 2-D FETs. It reduces to (5) if $C_{bt} = C_{bb}$, $V_{Tt} = V_{Tb}$, and both gates are shortcut. For a single gate 2-D FET, (18) is also valid with $C_{bb} = 0$ and therefore $n_{bb} = 0$, $\alpha = 1$, and $\beta = 0$.

For a p -type channel FET, the mathematical derivation is equivalent. Fig. 6 shows the valence band energy diagram across the top-gate/top-insulator/channel/bottom-insulator/bottom-gate structure. Note that V_{tg} and V_{bg} are assumed to be negative raising the gates Fermi levels with respect to the Fermi energy of the channel. For the sake of brevity, we will derive only the main steps.

From the band diagram and following a similar reasoning as in the main text, at a point x in the channel, we can write:

$$\begin{aligned} (E_v(x) - E_{Fp}(x)) - \phi_{tm} + qV_{bt}(x) + (\chi_s + E_g) \\ = -qV_{tg} - E_{Fp}(x) \\ (E_v(x) - E_{Fp}(x)) - \phi_{bm} + qV_{bb}(x) + (\chi_s + E_g) \\ = -qV_{bg} - E_{Fp}(x). \end{aligned} \quad (19)$$

The preservation of charge neutrality and Gauss' law allow us to write $p_s = n_{tg} + n_{bg} = V_{bt}/C_{bt} + V_{bb}/C_{bb}$, with p_s the hole density in the channel, n_{tg} and n_{bg} the electron sheet densities at the top and bottom gates, and C_{bt} and C_{bb} defined earlier. Inserting (19) in the previous equality, we can write

$$\begin{aligned} p_s = \frac{C_{bt} + C_{bb}}{q^2} [E_v(x) - E_{Fp}(x)] + \frac{C_{bt}}{q} (-V_{tg} + V_{Tt}) \\ + \frac{C_{bb}}{q} (-V_{bg} + V_{Tb}) - \frac{E_{Fp}(x)}{q} \end{aligned} \quad (20)$$

where the threshold voltages $V_{Tt} = (\phi_{tm} - \chi_s - E_g)/q$, and $V_{Tb} = (\phi_{bm} - \chi_s - E_g)/q$ have been introduced. From the 2-D hole density $p_s = p_q \ln(1 + \exp[(E_v - E_{Fp})/kT])$; where

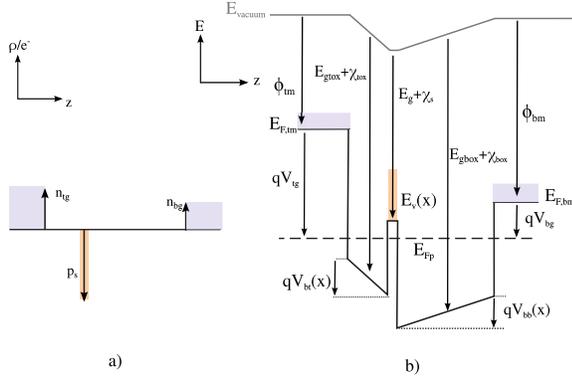


Fig. 6. Sheet carrier densities and valence band energy diagram along the top-gate/top-insulator/channel/bottom-insulator/bottom-gate direction for p -type asymmetric double gate FET.

$p_q = g_v g_s m_v^* kT / 2\pi \hbar^2$ is defined (m_v^* being the valence band effective mass) and after some algebra, we can write

$$e^{\frac{p_s(x)}{p_{bt} + p_{bb}}} \left(e^{\frac{p_s(x)}{p_q}} - 1 \right) = e^{\alpha \left(\frac{-V_{tg} + V_{Tl}}{V_{th}} \right) + \beta \left(\frac{-V_{bg} + V_{Tb}}{V_{th}} \right) - \frac{E_{Fp}(x)}{qV_{th}}} \quad (21)$$

with $p_{bt} = C_{bt} V_{th} / q$ and $p_{bb} = C_{bb} V_{th} / q$, characteristic hole densities associated with the top and bottom barrier capacitances, and β and α previously defined.

The drain current derivation is completely equivalent to the case discussed in the main text except for the sign of the carrier charge, meaning $J_d = +q p_s(x) \mu dE_{Fp}(x)/dx/q$, therefore leading to

$$I_d = -q^2 \mu \frac{W}{L} \left[\left(\frac{p_{s,si}^2 - p_{s,di}^2}{2C_g} \right) + \frac{p_q^2}{C_{dq}} \left(e^{-\frac{p_{s,di}}{p_q}} - e^{-\frac{p_{s,si}}{p_q}} \right) \right] \quad (22)$$

where $p_{s,si}$ and $p_{s,di}$ stand for hole sheet densities at the source, $E_{Fp}(x_{si}) = 0$, and at the drain, $E_{Fp}(x_{si} + L) = -qV_{sd}$.

APPENDIX II

This section evaluates the integral in (10). Using the definition $u = (n_s/n_q)$, it can be written as

$$I_d = -q\mu \frac{W}{L} V_{th} n_q^2 \int_{u(x_{si})}^{u(x_{si}+L)} \left[\frac{\left(\frac{1}{n_b} + \frac{1}{n_q} \right) e^u - \frac{1}{n_b}}{e^u - 1} \right] u du \quad (23)$$

and therefore

$$I_d = -q\mu \frac{W}{L} V_{th} n_q^2 \int_{u(x_{si})}^{u(x_{si}+L)} \left[\frac{u}{n_b} + \frac{1}{n_q} \frac{ue^u}{e^u - 1} \right] u du. \quad (24)$$

The exact solution of the previous integral is given by

$$I_d = q\mu \frac{W}{L} V_{th} n_q^2 \left[\frac{1}{n_b} \frac{u^2}{2} + \frac{u \ln(1 - e^{-u})}{n_q} + \frac{\mathcal{L}i_2(e^{-u})}{n_q} \right]_{u_d}^{u_s} \quad (25)$$

where $u_d = u(x_{si} + L)$ and $u_s = u(x_{si})$, and $\mathcal{L}i_2$ denotes the polylogarithm function of second order [20]:

$$\mathcal{L}i_2(y) = \begin{cases} \sum \frac{y^k}{k^2}, & \text{for } |y| \leq 1 \\ \frac{\pi^2}{3} - \frac{1}{2} \ln(y)^2 - \sum_k \frac{1}{y^k k^2} - i\pi \ln(y), & \text{for } y > 1 \end{cases} \quad (26)$$

with i the imaginary unit. Since $u = n_s/n_q > 0$, then $y = e^{-u} > 1$, and we must use the second case in (26) to write

$$I_d = q\mu \frac{W}{L} V_{th} n_q^2 \left[\frac{1}{n_b} \frac{u^2}{2} + \frac{u \ln(1 - e^{-u})}{n_q} - \frac{1}{n_q} \frac{u^2}{2} - \frac{1}{n_q} \sum_k \frac{e^{-ku}}{k^2} - \frac{1}{n_q} i\pi u \right]_{u_d}^{u_s} \quad (27)$$

where the constant factor $\pi^2/3$ is canceled out when evaluating the integral limits. We can simplify (27) by grouping the first and third terms, and utilizing $i\pi = \ln(-1)$ to group the second and fifth terms

$$I_d = q\mu \frac{W}{L} V_{th} n_q \left[\left(\frac{n_q}{n_b} - 1 \right) \frac{u^2}{2} + u \ln(e^u - 1) - \sum_{k=1}^{u_d} \frac{e^{-ku}}{k^2} \right]_{u_s}^{u_d} \quad (28)$$

that is the exact simple solution for I_d . Equation (28) can be further simplified by making two approximations: 1) for $u \gg 1$, $u \ln(e^u - 1) \approx u^2$ and 2) for $u \rightarrow 0$, the dominant term is the sum of exponentials that we can truncate into the first term. The simplified expression of I_d reads

$$I_d = q\mu \frac{W}{L} V_{th} n_q \left[\left(1 + \frac{n_q}{n_b} \right) \left(\frac{u_s^2 - u_d^2}{2} \right) + (e^{-u_d} - e^{-u_s}) \right]. \quad (29)$$

Undoing the change of variable $u = n_s/n_q$, and using the definitions of $C_g^{-1} = (1/C_{dq} + 1/C_b) = (V_{th}/qn_q + V_{th}/qn_b)$ and $n_q = C_{dq} V_{th}/q$ proposed in Section II, we get

$$I_d = q^2 \mu \frac{W}{L} \left[\left(\frac{n_{s,si}^2 - n_{s,di}^2}{2C_g} \right) + \frac{n_q^2}{C_{dq}} \left(e^{-\frac{n_{s,di}}{n_q}} - e^{-\frac{n_{s,si}}{n_q}} \right) \right] \quad (30)$$

where we have used the notation $n_{s,si} = n_s(x_{si})$ and $n_{s,di} = n_s(x_{si} + L)$.

To conclude, let us discuss the accuracy of the approximated expression in (29). Fig. 7 shows the error, defined as $\epsilon_{I_d} = |I_d - I_d^*|/I_d$ [with I_d and I_d^* corresponding to the drain current expressions in (28) and (29)] as a function of the integral limits u_s and u_d . $m_c^* = 0.5m_0$, $g_v = 2$, $t_b = 1.5$ nm, and $\epsilon_b = 5\epsilon_0$ are considered resulting in $n_q = 1.1 \times 10^{13}$ cm $^{-2}$ and $n_b = 9.52 \times 10^{11}$ cm $^{-2}$.

ϵ_{I_d} is negligible for large values of u_s and/or u_d where the quadratic factor is dominant in (29) and it approximates well the logarithmic term in (28). The error also tends to zero for small values of u_s and u_d where the current is determined

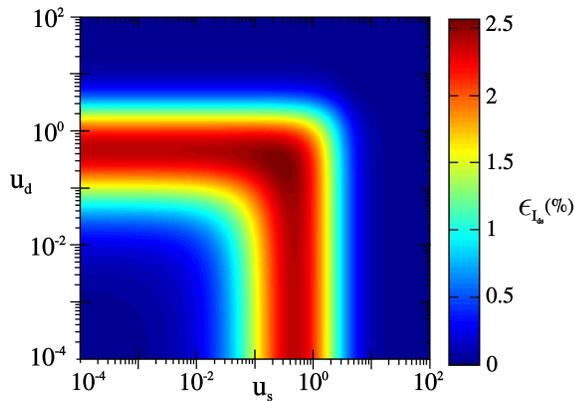


Fig. 7. $\epsilon_{I_d} = |I_d - I_d^*|/I_d$, with I_d and I_d^* corresponding to the drain current expressions of (28) and (29), as function of the integral limits u_s and u_d .

by the exponential factor. For these values, the higher order exponential terms in (28) go with $1/k^2$ and tend to cancel when evaluated at both integral limits. When u_s and/or u_d are in the range $[0.05, 2.5]$, the quadratic and the sum truncation approximations behave slightly worse, and ϵ_{I_d} reaches 1% – 2.5%. Different values of n_q and n_b have been studied and result in quantitatively similar ϵ_{I_d} behavior. The error peak as well as the width of the error stripe (defined at half of the peak amplitude) decrease with the n_q/n_b ratio decreasing.

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