Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV

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***Abstract*—**We demonstrate record-high performance in normally-off single and multi-fin β-Ga_2O_3 vertical power transistors. The effective channel mobility is significantly improved up to ~130 $cm^2/V{\cdot}s$ with a post-deposition annealing process. With a fin-channel width of 0.15 μm, true normally-off operation is achieved with a threshold voltage of >1.5 V; a record-high breakdown voltage of 2.66 kV (at V_{gs}=0 V) and a specific on-resistance of 25.2 $m\Omega{\cdot}cm^2$ are obtained in multi-fin devices, corresponding to a Baliga's figure-of-merit of 280 MW/cm^2, which is the highest among all Ga_2O_3 transistors. Devices with (100)-like fin-channel sidewalls exhibit the lowest interface trapped charge density and a significantly higher current than other fin orientations. These findings offer important insights on the development of Ga_2O_3 MOSFETs and show great promise of Ga_2O_3 vertical power devices.

I. Introduction

Owing to the availability of high-quality melt-grown substrates, an ultra-high breakdown field of 6-8 MV/cm and a decent electron mobility up to 200 $cm^2/V{\cdot}s$, β-Ga_2O_3 is an attractive material for the development of cost-effective, high performance power devices [1]. To date, lateral transistors with a breakdown voltage (*BV*) up to 2.32 kV have been demonstrated [2-4]. For high voltage and high current applications, vertical devices are generally preferred. Last year, we demonstrated vertical Ga_2O_3 trench Schottky barrier diodes with a *BV* of 2.44 kV [5]. To realize normally-off vertical transistors, a submicron fin-channel structure can be utilized without the need for p-type doping [6]. With this device concept, normally-off single-fin Ga_2O_3 vertical transistors with a *BV* of up to 1.6 kV have been demonstrated [7-9].

Despite promising advancements, the present Ga_2O_3 power transistors face two main challenges. First, the effective channel mobility is much lower than that in the bulk. In, but not restricted to, vertical fin transistors, the effective channel mobility is found to be hampered by etch damage and sidewall depletion due to interface-trapped charge, resulting in an effective channel mobility of only 30 $cm^2/V{\cdot}s$ [8]. Second, the very high-field operation required for achieving high-performance Ga_2O_3 devices post challenges on electric-field management. We have demonstrated recently that a source-connected field-plate can greatly boost the *BV* by mitigating the edge field crowding [9].

In this work, we demonstrate significantly improved fin channel mobility with post-deposition annealing (PDA) in normally-off single-fin transistors. The dependence of sidewall interface trapping on the fin orientation is explicitly revealed. In addition, multi-fin transistors are realized for the first time, allowing for (i) unambiguous evaluation of the specific on-resistance ($R_{on,sp}$), which reveals a record-high performance among all Ga_2O_3 power transistors, and (ii) demonstration of scalability toward large-area devices.

II. Device Design and Fabrication

The epitaxial wafer consists of a 10-μm n^--Ga_2O_3 drift layer grown by halide vapor phase epitaxy on a (001) n^+-Ga_2O_3 substrate (**Fig. 1**). The net doping concentration in the drift layer below the fin region was determined to be ~2×10^{15} cm^{-3} from capacitance-voltage measurements. An n^+ layer was formed on the top surface by Si-implantation at Hosei and activated at 1000 °C to facilitate the source ohmic contact. Submicron fin channels were defined by electron beam lithography and formed by dry etching using a BCl_3/Ar mixture. The resultant fin channels have a near vertical sidewall profile (**Fig. 2**). After dry etching, the Cr/Pt etch mask was removed by Cr etchant and the wafer was treated with HF for 23 min to remove plasma damage. Next, the drain contact (Ti/Au) was deposited before the deposition of the gate stack, consisting of a 35-nm Al_2O_3 gate dielectric by atomic layer deposition (ALD) and a 50-nm Cr gate by sputtering. The gate stack and thick ALD Al_2O_3 spacer was patterned by photoresist planarization and self-aligned etching processes detailed in our previous reports [7-9]. The source electrode (Ti/Al/Pt) was deposited by sputtering after the spacer formation, simultaneously forming the source-connected field-plate (**Fig. 1**). The devices were tested before and after a PDA at 350 °C for 1 min under N_2 to improve the interface quality [10]. **Fig. 3** shows top views of the fabricated single-fin and multi-fin devices. *The default orientation of all fin channels is along the [010] direction length-wise with (100)-like sidewalls, and the device characteristics discussed are all after PDA and threshold voltage stabilization, unless otherwise specified.*

The effect of PDA on the output characteristics is captured in **Fig. 4**. A significant increase in current density is observed after PDA. The source contact resistance is improved, as expected [11]. Besides, sidewall depletion in fin channels due to interface trapped charges is also reduced. This is because the

percentage improvement in the on-resistance (R_{on}) of devices with smaller fin width (W_{fin}) is much higher than with large W_{fin}.

III. Single-fin Transistors

The dependence of transistor transfer characteristics and threshold voltage (V_{th}) on the fin width is shown in **Fig. 5** and **Fig. 6**. By analytical modeling of the threshold voltage [6], the channel doping concentration was determined to be ~1.9×10^{16} cm^{-3}. The existence of negative interface charges (with a density of $|N_{it}|$) is found to be responsible for the higher-than-expected V_{th} values. After a fresh upward transfer *I-V* sweep, V_{th} increased by ~0.5 V and then stabilized. This is due to the increase of $|N_{it}|$ during the fresh transfer *I-V* sweep from its initial value of ~9×10^{11} cm^{-2} to ~1.5×10^{12} cm^{-2}.

Fig. 7 shows the extracted and simulated R_{on} at a fixed gate voltage of 3 V as a function of W_{fin}. Since the current spreads laterally up to 50 μm in the n^+ substrate [12], the substrate resistance (R_{sub}) can be neglected. From simulation and fitting with the experimental data, the fin channel mobility is found to be ~130 $cm^2/V\cdot s$. In **Fig. 8**, $R_{on,sp}$ is normalized to the n^+ source area to help evaluate the specific fin channel resistance ($R_{fin,sp}$), which is found to be nearly constant with W_{fin}, indicating that near flat-band condition at V_{gs}=3 V is achieved—an improvement over our prior works [7][8]. Since current spreading is substantial in the drift layer (see inset in **Fig. 8**), $R_{on,sp}$ normalized to the n^+ source area alone (0.52 $m\Omega\cdot cm^2$ with W_{fin}=0.15 μm) *grossly overestimates the transistor figure-of-merit (11.6 GW/cm² with a BV of 2460 V)*; using an effective conduction width of ~10 μm, the $R_{on,sp}$ is re-normalized to be 35.2 $m\Omega\cdot cm^2$ with W_{fin}=0.15 μm.

The impact of fin channel orientation is shown in **Fig. 9** and **Fig. 10**. A monotonic decrease in V_{th} is observed when the channel is aligned toward the [010] direction, indicating that $|N_{it}|$ is lowest on the (100)-like sidewalls. The most significant fixed charge trapping is found on devices with (010)-like sidewalls. **Fig. 11** shows the off-state characteristics of devices with W_{fin}=0.35 μm. The high $|N_{it}|$ in devices with (010)-like sidewalls eliminates the drain-induced barrier lowering (DIBL) effect otherwise seen in devices with (100)-like sidewalls, leading to a much higher *BV* of 2370 V. In devices with W_{fin}=0.15 μm, DIBL is not observed even with (100)-like sidewalls due to the higher channel aspect ratio as discussed in Ref. 8, as a result, a *BV* of 2460 V can be measured at V_{gs}=0 V.

IV. Multi-fin Transistors

Fig. 12 and **Fig. 13** show the stabilized *I-V* characteristics of a multi-fin device with W_{fin}~0.15 μm. A subthreshold slope of ~100 mV/dec was extracted, corresponding to an interface trap density (D_{it}) of ~9.1×10^{11} $cm^{-2}eV^{-1}$ [8]. The device has an on-off ratio of >10^8 and a V_{th} of ~1.8 V at 0.1 A/cm^2. The $R_{on,sp}$ is determined to be 25.2 $m\Omega\cdot cm^2$ from DC measurements. From pulsed *I-V* measurements, a smaller $R_{on,sp}$ of 23.2 $m\Omega\cdot cm^2$ is extracted, likely due to reduced self-heating and charge trapping effects under pulsed conditions [5][13].

The statistics of the extracted $R_{on,sp}$ as a function of the fin area ratio is shown in **Fig. 14**. As expected, $R_{on,sp}$ reduces with increasing fin area ratio. Using a simple model, the specific fin channel resistance is determined to be ~0.9 $m\Omega\cdot cm^2$, corresponding to an effective channel mobility of ~40 $cm^2/V\cdot s$. The lower channel mobility than single-fin devices is attributed to rougher sidewalls resulting from plasma-loading effects during dry etch for the formation of closely-spaced fin channels.

Fig. 15 shows the off-state *I-V* characteristics. By comparison with the MOS-capacitors, the device breakdown is found to be limited by the device edge termination. A highest *BV* of 2655 V is measured at V_{gs}=0 V in a multi-fin device with a fin width of 0.15 μm and a pitch size of 1.7 μm.

Fig. 16 and **Fig. 17** shows the statistics of the *BV*. In devices with DIBL effects ($W_{fin}\geq$0.25 μm), a negative V_{gs} was applied to evaluate the hard breakdown. As expected, the *BV* is limited by the edge termination and does not show dependence on either the pitch size or W_{fin} if the DIBL was successfully suppressed, as in the case of W_{fin}=0.25 μm under V_{gs}=-5 V.

Fig. 18 shows the benchmark plot of Ga_2O_3 power transistors. For a fair comparison, the $R_{on,sp}$ of single-fin transistors is calculated using the effective conduction width of ~10 μm considering current spreading in the drift region (see inset in **Fig. 8**). Single and multi-fin transistors with W_{fin}=0.15 μm in this work exhibit record-high *BV*s (2460 V & 2655 V, respectively). The multi-fin device reaches a Baliga's figure-of-merit of 280 MW/cm^2, the highest among all Ga_2O_3 transistors.

V. Conclusions

High performance single-fin and multi-fin Ga_2O_3 normally-off vertical power transistors are demonstrated. A 350°C PDA process is found to significantly improve the transistor R_{on} and an effective fin channel mobility of ~130 $cm^2/V\cdot s$ is extracted. Sidewall interfaces with (100)-like orientation show the highest interface quality. A $R_{on,sp}$ of 25.2 $m\Omega\cdot cm^2$ and a record-high *BV* of 2.66 kV was achieved in multi-fin devices, marking a significant step forward in the development of high performance Ga_2O_3 power transistors.

Acknowledgment

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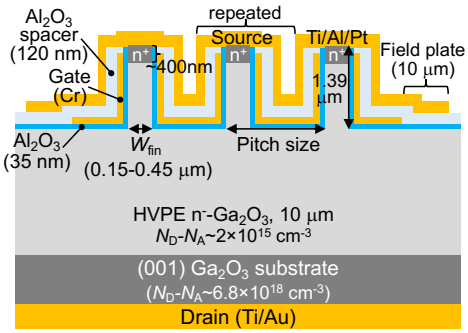

Fig. 1. Schematic cross-section of the Ga_2O_3 vertical fin transistors with multiple fins. Fin channel widths of 0.15-0.45 μm and pitch sizes ranging from 1.2 μm to over 2 μm were designed. A source-connected field-plate was implemented.

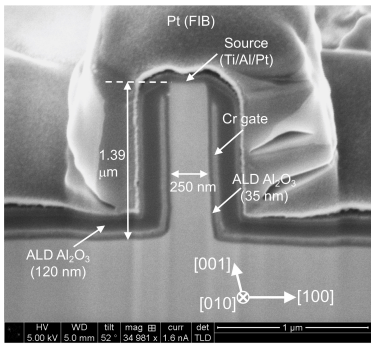

Fig. 2. Scanning electron microscopy (SEM) cross-section image of a fin channel with a 0.25-μm fin channel width (W_{fin}).

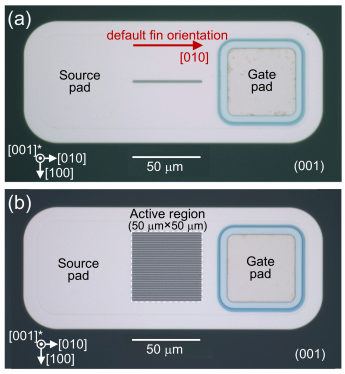

Fig. 3. Optical image of (a) a single-fin and (b) a multi-fin device. The multi-fin devices have an active region area of 50 μm×50 μm, which is used for calculation of the current density.

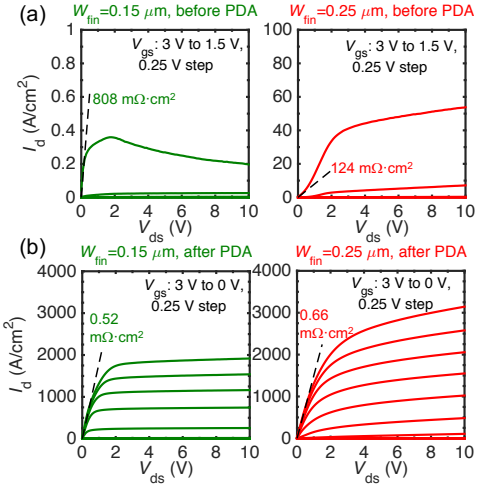

Fig. 4. Output *I-V* characteristics of single-fin transistors with a W_{fin} of 0.15 μm and 0.25 μm (a) before post-deposition annealing (PDA) and (b) after PDA. The current was normalized to the n^+ source area (W_{fin}×50 μm).

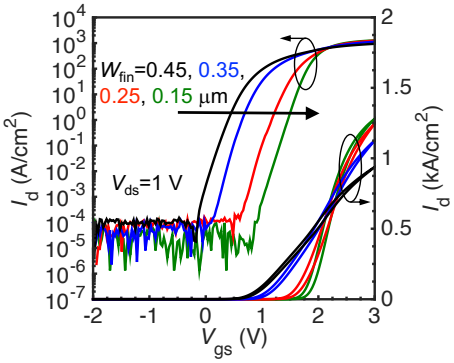

Fig. 5. Transfer *I-V* characteristics of the single-fin transistors with different fin channel widths. The current is normalized to the n^+ source area. A clock-wise hysteresis of ~120 mV is observed for all fin widths.

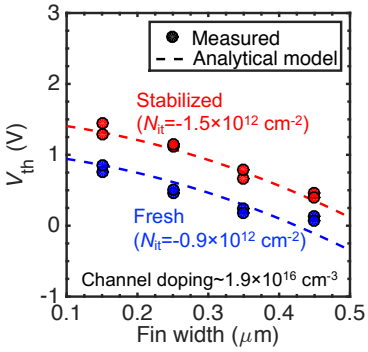

Fig. 6. Extraction and modeling of the threshold voltage (V_{th}) as a function of the fin width at I_{ds}=1 A/cm². The fresh V_{th} values were extracted from the 1st upward transfer *I-V* sweeps. V_{th} stabilized after the 1st sweep. An interfacial *fixed* charge density (N_{it}) for both cases is extracted.

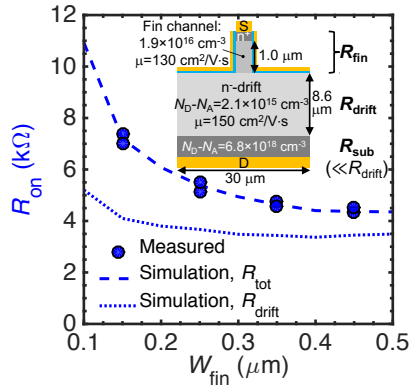

Fig. 7. Measured and simulated on-resistance (R_{on}) of the single-fin transistors. Inset shows the parameters used in the simulation and the breakdown of the R_{on} components. The substrate resistance (R_{sub}) and the contact resistance are neglected. Electron accumulation at the fin channel sidewall is not considered.

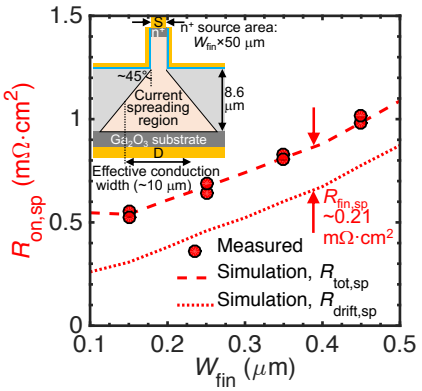

Fig. 8. Measured and simulated specific on-resistance ($R_{on,sp}$) of the single-fin transistors, normalized to the n^+ source area. The reduction of specific drift region resistance ($R_{drift,sp}$) with decreasing W_{fin} indicates that this normalization method underestimates the R_{drift} as a result of the current spreading (inset). An effective spreading angle of ~45° and an effective conduction width of ~10 μm in the drift region were determined from simulation.

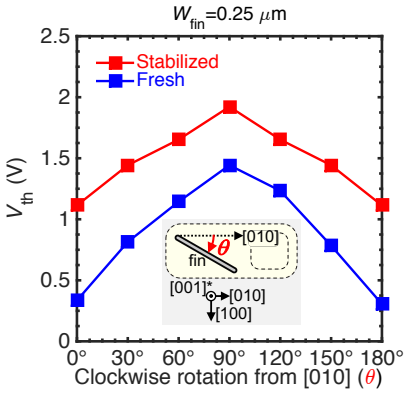

Fig. 9. Dependence of the V_{th} on the fin channel orientation in single-fin devices with a fin width of 0.25 μm. The V_{th} was extracted at a current level of 0.1 A/cm². Inset shows the definition of the rotation angle for the fin channel orientation. The lowest V_{th} was found in fin channels along [010] direction with (100)-like sidewall, indicating a lowest $|N_{it}|$.

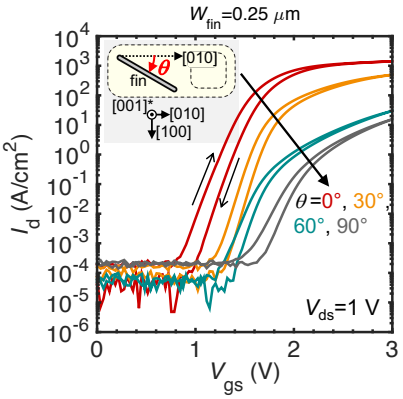

Fig. 10. Transfer *I-V* characteristics of the single-fin vertical transistors with different channel orientations and W_{fin}=0.25 μm.

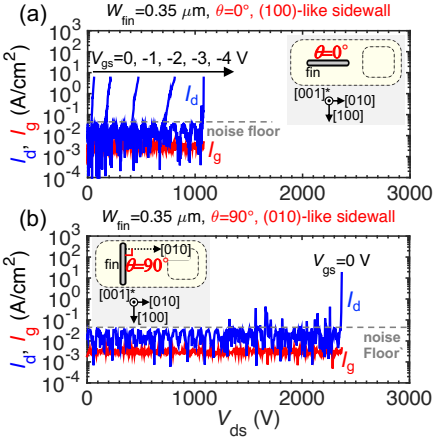

Fig. 11. 3-terminal breakdown test on single-fin transistors with (a) (100)-like sidewall and (b) (010)-like sidewall. The fin width is 0.35 μm. The current was normalized to the source contact area.

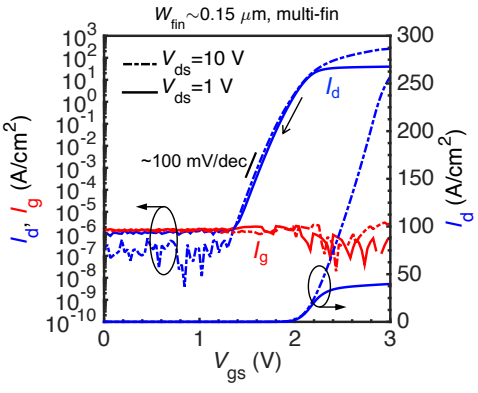

Fig. 12. Transfer *I-V* characteristics of a multi-fin transistor with a fin width of ~0.15 μm and a pitch size of 1.7 μm. The current was normalized to the total active region area (50 μm×50 μm).

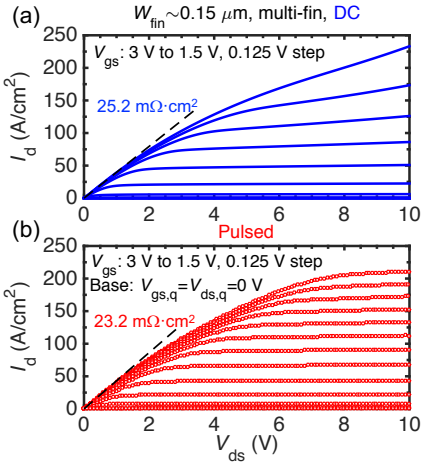

Fig. 13. Output *I-V* characteristics of the multi-fin transistor shown in Fig. 12. (a) DC and (b) Pulsed *I-V* measurements. A pulse width of 6 μs and a duty cycle of 0.06% is used.

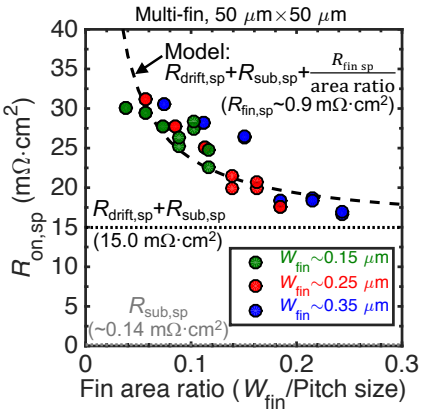

Fig. 14. Statistics of the extracted $R_{on,sp}$ of the multi-fin transistors. $R_{on,sp}$ *vs.* the fin area ratio can be roughly fitted by a simple model, from which an effective specific fin channel resistance of ~0.9 mΩ·cm^2 is extracted.

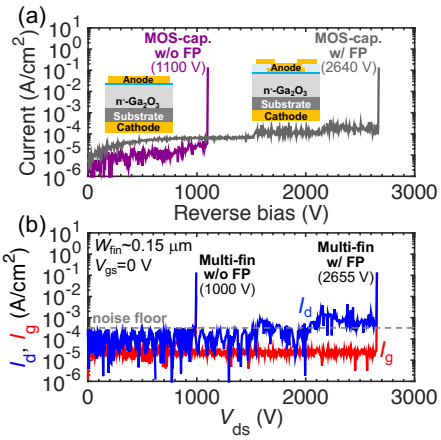

Fig. 15. Off-state breakdown measurements of (a) MOS-capacitors and (b) multi-fin transistors with a fin width of 0.15 μm. *BV* is much higher in the presence of the field-plate.

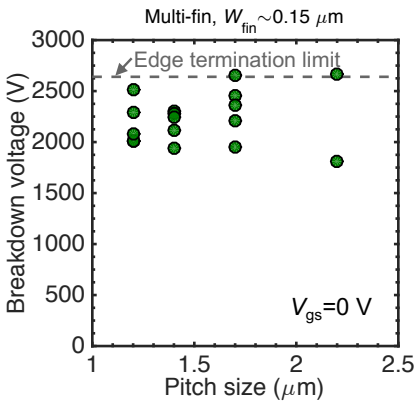

Fig. 16. Breakdown voltage statistics *vs.* the pitch size in multi-fin transistors with W_{fin}=0.15 μm. The *BV*s are all measured at V_{gs}=0 V. The edge termination limit is taken from the *BV* of the MOS-capacitor test structure with a field-plate (Fig. 15(a)).

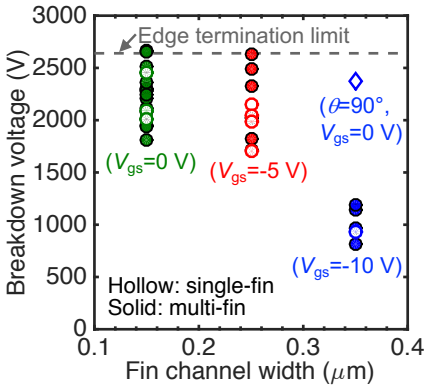

Fig. 17. Breakdown voltage statistics *vs.* fin channel width for both single-fin and multi-fin transistors. In devices with DIBL effects (W_{fin}≥0.25 μm), a negative V_{gs} was applied to evaluate the hard breakdown. The transistor *BV* with W_{fin}=0.35 μm is limited by DIBL.

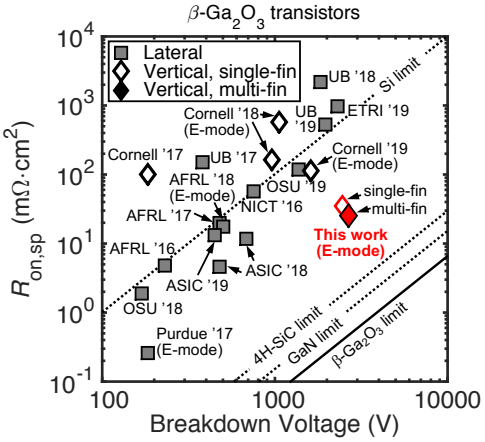

Fig. 18. Benchmark plot of Ga_2O_3 transistors. For a fair comparison, the R_{on} of single-fin vertical transistors (including our prior results) is normalized using the effective conduction width of ~10 μm (see inset in Fig. 8), since $R_{on,sp}$ normalized to the n^+ source contact area grossly overestimates the figure-of-merit of these vertical devices.