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Modeling and Circuit Design of Associative Memories With Spin–Orbit Torque FETs

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ABSTRACT This article introduces a circuits model for a proposed spin-based device called a spin–orbit torque field-effect transistor (SOTFET) that can operate as a nonvolatile memory and logic device. The SOTFET utilizes an FET structure with a ferromagnetic-multiferroic (MF) gate-stack that enables read/compute and write functions to be isolated. This is achieved by a combination of a ferromagnetic layer that is programmable via spin–orbit torque coupled to an MF layer that also couples into the gate of a traditional FET. Additionally, this device has logic gate-like behavior and can be designed to operate in either AND or OR gate mode. We begin with a physics-based model of this device and derive a SPICE level model that can be integrated into the Cadence toolset. Using such a device we demonstrate MRAM, content addressable memories (CAM), and ternary CAM (TCAM) functionality with 3 to 5 transistors, a significant decrease over the CMOS alternative circuits, showing that such a device can enable low cost and compact associative memories not currently feasible with CMOS devices.

INDEX TERMS Beyond CMOS, compact models, ferroelectric field-effect transistor (FeFET), logic-in-memory, multiferroics (MFs), nonvolatile memory, spin–orbit torque (SOT), spin–orbit torque field-effect transistor (SOTFET), spintronics.

I. INTRODUCTION

FOR THE past decade, semiconductor device research has focused on finding ways to extend the scaling path of the semiconductor industry (i.e., Moore's law) through the development of post-CMOS devices. Ideally, these devices would not only replace CMOS switches, but they would also enable faster and more energy-efficient computing. It is now apparent that keeping Moore's Law alive is nontrivial, and as devices shrink to quantum physical limits, a combination of device, circuit, and architectural innovation is necessary. While many alternative devices have been proposed, achieving a switch that is better and more scalable than a CMOS switch while retaining all the characteristics required of CMOS devices (i.e., power gain, small geometry, fan-out, speed) is extraordinarily elusive.

Many of these emerging devices instead exhibit unique characteristics that make them advantageous for specific applications. For example, several memory devices, including ferroelectric field-effect transistors (FeFET) [1], resistive RAM (RRAM) [2], phase change RAM (PCRAM) [3], and magnetic-tunnel-junction-based RAM (MTJ-MRAM) [4] have been developed. Of these technologies, FeFETs and two types of MTJ-MRAMs, switched by spin-transfer torque (STT-MRAM) or spin–orbit torque (SOT-MRAM), have shown promise in demonstrating nonvolatile, reliable and relatively low power performance, and have made the most progress toward commercialization. In FeFETs, a ferroelectric material is used in the gate-stack of an FET. In both types of MTJ-MRAMs, the storage element is an MTJ with two magnetic layers. The resistance of the MTJ varies according to the magnetization of one of the layers called the free layer. The SOT-MRAM conceivably improves on the STT-MRAM by separating the read and write paths, thereby improving the endurance of the device by avoiding

wearing out the MTJs from the high currents required for writing.

However, both MRAM technologies still suffer from a low tunneling magnetoresistance ratio (TMR) with the highest reported in the literature at room temperature of about 600% [5]. This low TMR makes it difficult to read the output signal. In addition, these devices, by nature, do not hold promise as logic devices due to lack of input–output isolation and gain.

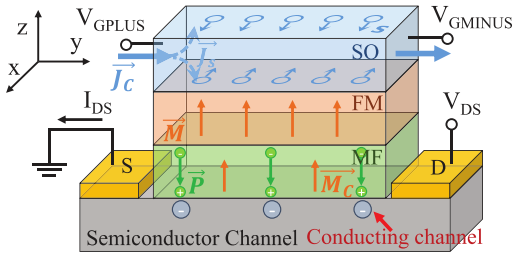

FIGURE 1. Device structure and working principle of the SOTFET. SOTFET resembles a MOSFET with a unique gate-stack composed of a SO layer, an FM layer, and an MF layer stacked on a semiconductor channel. Charge current flows through the SO layer, and spins accumulate on the surfaces of the SO layer. The spins switch the magnetization of the FM through SOT, which in turn switches the polarization P in the MF due to exchange coupling. Effectively switching P gates the semiconductor channel.

As an alternative, we consider the concept of a multifunctional SOT device that incorporates both memory and logic functions and can enable more functionality in a power-efficient and compact package. The proposed SOTFET, or SOT FET, as shown in Fig. 1, will use SOT to write the magnetization of the ferromagnet (FM) and will read out the device state through a multiferroic (MF) (ferroelectric) FET gate-stack. In this way, we expect to boost the on–off ratio to a value typical for an FET, on the order of or greater than 10^5.

Although this device has not been realized experimentally, it is inspired by recent advances in SOT and MF materials. In this article, we explore the potential of this device for interesting circuit behavior. We describe our compact circuit model for the device and show example circuit memory arrays built using our compact model.

We also demonstrate several unique circuit characteristics of the SOTFET that can be exploited for compact and efficient associative memories. Foremost of these characteristics is the AND/OR functionality built into single devices. This logic-in-memory behavior enables the construction of three transistor content addressable memories (CAM) and five transistor ternary CAM (TCAM) that are increasingly important blocks for applications in machine learning.

The organization of the rest of this article is as follows: In Section II, we describe the device structure and principle of operation; in Section III, we describe our circuit-level compact model; in Section IV, we present the device as a logic device whose logic function depends on three major parameters; in Section V, we introduce RAM, CAM, and TCAM topologies, which are verified using our compact model; Section VI discusses the results, points out some limitations and compares to both standard CMOS and FeFET equivalent circuits; Section VII concludes.

II. DEVICE STRUCTURE AND WORKING PRINCIPLE

The SOTFET device described here operates as both a memory and a logic device with gain and input–output isolation. The device structure of a SOTFET resembles a conventional MOSFET, but with a unique gate-stack, as shown in Fig. 1. The SOTFET gate-stack comprises three layers from top to bottom, a spin–orbit (SO) layer, an FM and an MF layer. The SOTFET gate-stack is then placed on a semiconductor channel with an ordinary FET layout.

The working principle of the SOTFET is described as follows with the help of Fig. 1. When a charge current flows through the SO layer, transverse spin currents with different spin polarization separate and spins accumulate at the surfaces of the SO layer due to spin-momentum coupling [6]. The spins accumulated at the SO/FM interface switch the magnetization ($\boldsymbol{M}$) of the FM through SOT [7]. Due to the exchange coupling between the FM and the MF [8], the magnetic dipole of the MF is also switched together with the $\boldsymbol{M}$ in the FM. Since the $\boldsymbol{M}$ and electric polarization ($\boldsymbol{P}$) are strongly coupled in the MF material due to the Dzyaloshinskii–Moriya interaction (DMI) [9], the electric dipole in the MF switches in tandem. The resulting switching of $\boldsymbol{P}$ in the MF gates the semiconductor channel as in FeFETs and NCFETs [10], [11]. The semiconductor channel acts as the read-out component, offering a high on–off-ratio. Successful SOTFET operation will require achieving a hierarchy of energy couplings such that the magnetic exchange and DMI are stronger than the coercive forces that resist switching of $\boldsymbol{P}$; an experimental group at Cornell is working toward this goal. A more detailed introduction and explanation of the physics of SOTFET can be found in the work by Li *et al.* [12], where they explored switching polarization through magnetization in an MF with a large magnetization, and moderate polarization where $\boldsymbol{M}$ and $\boldsymbol{P}$ are strongly coupled.

In this article, we consider a topological insulator (TI) as the SO layer to provide an enhanced spin Hall efficiency [13], [14]. The FM layer is chosen to have perpendicular magnetic anisotropy (PMA). A strong exchange coupling at the FM/MF interface is assumed so that the magnetic moments in FM and MF are directly coupled with each other. More detailed assumptions in the model will be introduced in Section III.

III. SOTFET CIRCUITS MODEL

We introduce two levels of models for the SOTFET structure proposed above: a compact physics-based model, including its implementation in the Cadence Virtuoso circuits simulator, and a high-level conceptual model with a focus on how the device's functional behaviors depend on key parameters. In this section, we describe the physics-based circuits model.

In the device described in Section II, an injected charge current through the gate terminals V_{GPLUS} and V_{GMINUS} generates a spin current, which switches the magnetization $\boldsymbol{m}$ of the FM layer through an SOT. For all simulations, we define the

state of the device to be m_z. The magnetization is in turn coupled to the polarization in the MF, which alongside the voltage applied to the gate, can modulate the channel of the FET. The model describes writing the device state by switching the FM layer's magnetization and reading the state through the device current through the FET channel. The FM layer's magnetization dynamics is modeled using a single-domain Landau–Lifshitz–Gilbert–Slonczewski (LLGS) equation; we assume direct coupling between the FM's magnetization and the MF's magnetization and polarization; finally, the device current is modeled as a function of the MF layer's polarization, charge-voltage relationship and a self-consistent solution of the MOSFET's charge-voltage relationship.

A. LLGS MODEL

The magnetization $\boldsymbol{m}$ of the FM is modeled using the LLGS equation, which models the change in the magnetization in response to the total torque, including the antidamping torque contribution from the spin current generated in the TI. The LLGS equation is given by [15]

$$\frac{d\vec{\boldsymbol{m}}}{dt} = -\gamma\mu_0 \boldsymbol{m} \times \boldsymbol{H}_{\text{eff}} + \alpha\left(\boldsymbol{m} \times \frac{d\boldsymbol{m}}{dt}\right) + \frac{\gamma}{M_s}\boldsymbol{\tau}_{\text{sot}} \quad (1)$$

where $\boldsymbol{m}$ is the normalized magnetization, γ is the electron gyromagnetic ratio, μ_0 is the vacuum permeability, $\boldsymbol{H}_{\text{eff}}$ is the effective magnetic field acting on $\boldsymbol{m}$, α is the Gilbert damping parameter, M_s is the saturation magnetization and $\boldsymbol{\tau}_{\text{sot}}$ is the SOT term.

We include both anti-damping $\boldsymbol{\tau}_{\mathbf{AD}}$ and field-like $\boldsymbol{\tau}_{\boldsymbol{FL}}$ torques in the SOT term $\boldsymbol{\tau}_{\text{sot}}$ given by

$$\boldsymbol{\tau}_{\text{sot}} = \frac{\hbar}{2\text{e}}\frac{J_c}{t}(\theta_{AD}\boldsymbol{m}\times(\boldsymbol{m}\times\boldsymbol{m_p}) + \theta_{FL}\boldsymbol{m}\times\boldsymbol{m_p}) \quad (2)$$

where $\boldsymbol{m}_p$ is the normalized spin polarization, $\hbar$ is the reduced Planck constant, e is the electron charge, J_c is the charge current density flowing through the TI layer terminals V_{GPLUS} and V_{GMINUS}, t is the thickness of the FM material, θ_{AD} and θ_{FL} are the spin Hall angles of the antidamping and field-like torques.

The effective magnetic field $\boldsymbol{H}_{\text{eff}}$ includes the anisotropy field $\boldsymbol{H}_k$ [16], the demagnetization field $\boldsymbol{H}_{\boldsymbol{demag}}$ [17] and an external magnetic field $\boldsymbol{H}_{\text{ext}}$, which is a globally applied external magnetic field. In the work presented in this article, $\boldsymbol{H}_{\text{ext}}$ is assumed to be in the y-direction. A more advanced physics-based model, including an explicit treatment of the DMI interactions, is presented in [12] which includes analysis showing that the external magnetic field is not necessary under certain circumstances. In this article, the sign of $\boldsymbol{H}_{\text{ext}}$ serves to determine the polarity of switching in response to the SOT.

Further details of our circuit simulation framework for the LLGS equation, including the simulation parameters are available in the supplementary material.

Fig. 2(a) is a transient simulation of the FM's m_z switch from $+1$ to -1 for two current densities. Fig. 2(b) is a quasi-static simulation of the final state of m_z when a constant spin current density is applied for 2 ns with external magnetic fields in $+\hat{y}$ and $-\hat{y}$ directions. The polarity of the spin current, which switches the magnetization to the $+z$ plane is determined by the direction of the magnetic field. For both figures, the magnitude of H_{ext} is $0.2|H_k|$ and the polarization of the spin current is in the $+\hat{x}$ direction, as shown in Fig. 1.

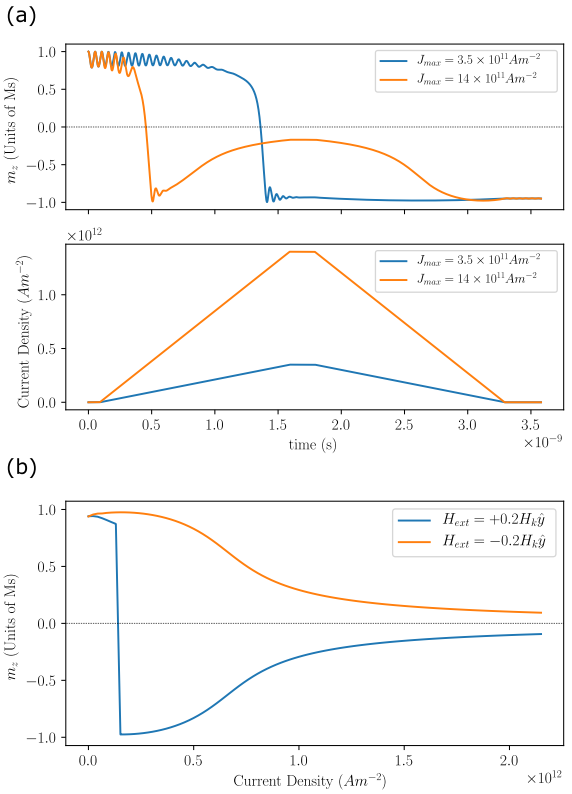

FIGURE 2. FM magnetization dynamics for high and low current densities. (a) Transient simulation of m_z showing magnetization switch from $m_z = +1$ to $m_z = -1$ for two current densities. (b) Quasi-static simulation of m_z as a function of the current density J when a constant spin current density is applied for 2 ns with external magnetic fields in $+\hat{y}$ and $-\hat{y}$ directions. Each data points represents m_z 2 ns after changing the current density. The polarity of the spin current which switches the magnetization to the $+z$ plane is determined by the direction of the external magnetic field.

Fig. 2 also shows that the magnetization does not switch until the current density is higher than a critical current density for which the magnetization (m_z) completely switches from $+1$ to -1. Further increase in the current density above the critical current switches m_z to an intermediate state closer to the $m_z = 0$ axis which eventually relaxes to -1 or $+1$ when the switching current is ramped down. Additional simulations show that for these high current density intermediate states close to the $m_z = 0$ axis, the eventual relaxation after the write current is switched off is less deterministic and sensitive to the slope of the current ramp-down, which is a potential source of write errors.

B. FM MAGNETIZATION TO MF POLARIZATION

It has already been experimentally demonstrated that the exchange coupling between ferromagnetic and MF materials can be strong enough that switching of the MF using an electric field switches the FM [8]. We assume here that materials parameters may also be chosen to achieve the converse—that manipulation of the FM will drive the switching of the

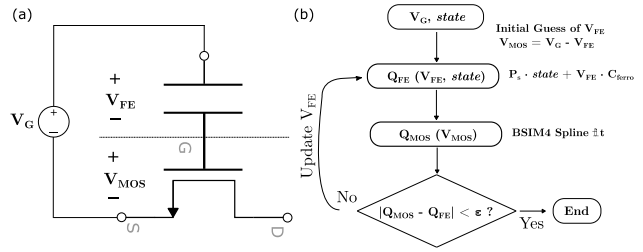

FIGURE 3. Block diagram showing (a) equivalent circuit diagram of SOTFET with applied voltages labeled and (b) iterative evaluation process to determine V_{MOS} and V_{FE} as a function of the gate voltage V_G and state.

MF. Though this has not been achieved yet, recent experiments have demonstrated switching of electric polarization in response to an applied magnetic field in homogeneous low-temperature MF materials [18], [19].

Thus, a linear relation between magnetization in FM and polarization in MF is assumed in this article. We model the interaction of FM and MF through a saturation polarization P_s, which we define to be the polarization at $|m_z| = 1$. We then define the MF's polarization as a function of the m_z state to be

$$P = P_s m_z.$$

We do not directly model the dynamics of the magnetization to polarization coupling since the polarization switching delay is estimated to be in the pico-second range [20], much smaller than the delay time-scale for the magnetization to switch. The switching dynamics of P have been explicitly analyzed in [12].

C. MF POLARIZATION TO DEVICE CURRENT

The MF induces a charge in the channel both due to its polarization (from magnetization) and from the voltage V_{FE} across it as a capacitor. We calculate the total channel charge as the sum of the polarization charge from the MF and the capacitive charge from the voltage across it

$$Q_{FE}(V_{FE}) = P_s \cdot \text{state} + V_{FE} \cdot C_{ferro} = Q_{MOS}(V_{MOS}). \quad (3)$$

We define the gate voltage V_G as the average of the voltage across the gate i.e., $(V_{GPLUS} + V_{GMINUS}/2)$. V_G is also the sum of the voltage across the MF V_{FE} and the voltage across the MOSFET V_{MOS}. Using a similar approach to that in [21], we iteratively solve for V_{FE} and V_{MOS} until the charge from the MF Q_{FE} is equal to the expected gate charge Q_{MOS} from V_{MOS} calculated using the industry standard BSIM4 MOSFET model [22], as shown in Fig. 3.

Our Cadence implementation models the FET readout using a transistor from a 28-nm process development kit (PDK) whose gate voltage V_{MOS} is a function of the device state, and V_G as portrayed in Fig. 4. V_{pol} is the gate voltage V_{MOS} at which the gate charge equals the saturation polarization P_s. The iterative solver is implemented in C++ and imported into the Cadence simulator using Verilog-A. We start with a one-time dc operating point characterization of the MOSFET gate charge as a function of the gate voltage for the selected PDK transistor. For subsequent simulations, we interpolate the characterization data to resolve V_{MOS} as

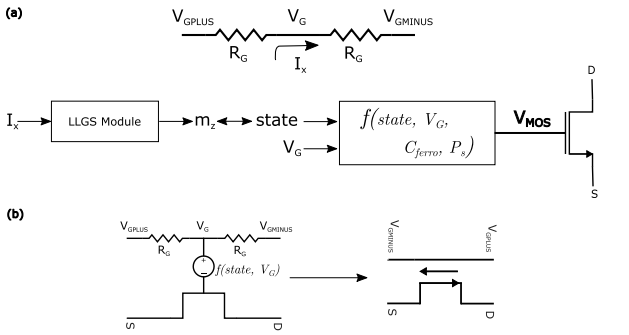

FIGURE 4. Equivalent circuit block diagrams and symbols for SOTFET. (a) Full model showing the main components. The gate is driven by dual voltage inputs V_{GPLUS} and V_{GMINUS} which generate current I_x across gate resistor R_G and average voltage V_G. I_x generates spin current which controls m_z. m_z and V_G are inputs to generate effective gate voltage V_{MOS}. (b) Circuit representation and symbol showing the Drain D, Source S, and gate terminals V_{GPLUS} and V_{GMINUS}.

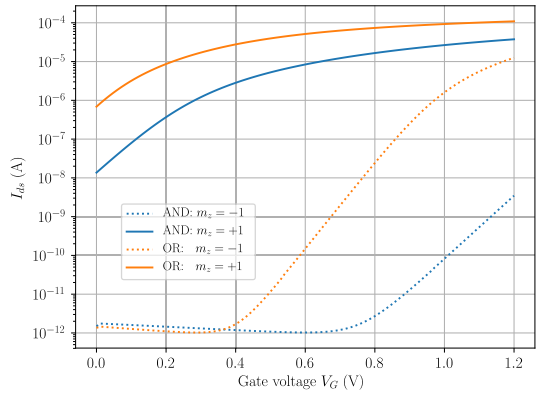

FIGURE 5. Drain current versus gate voltage for the two magnetization states and two sets of parameter values of C_{ferro} and V_{pol} corresponding to AND and OR mode functions. The AND mode parameters are $C_{ferro} = 0.5C_{ox}$, $V_{pol} = 0.13$ V; the OR mode parameters are $C_{ferro} = 2C_{ox}$, $V_{pol} = 0.34$ V.

a function of Q_{MOS} and solve (3) subject to the condition $V_G = V_{FE} + V_{MOS}$ for the given state and V_G circuit conditions. We then apply the calculated V_{MOS} as the gate voltage to the transistor.

Fig. 5 is a plot of the device current versus gate voltage for $m_z = +1$ and $m_z = -1$.

The overall block diagram of the physics-based model is shown in Fig. 4.

IV. SOTFET CONCEPTUAL MODEL

Our conceptual model highlights and extracts the most important parameters from the physics-based model to build a first-order circuit model that captures the behavior of the device. This conceptual model is used to obtain truth tables that are reused for analyzing the proposed circuits in Section V.

The magnetization dynamics of the FM is modeled as a memory device whose state switches with the direction of the write current through the device gate. For write currents above the critical current, the state (1 for $m_z = +1$, 0 for $m_z = -1$) of the device is programmed based on the polarity of the direction of current through the V_{GPLUS} and V_{GMINUS} terminals.

To capture the MF polarization to device current behavior, we emphasize three parameters from the physics model, which are as follows.

1) C_{ferro}: This is the capacitance of the MF. It captures how much control the gate voltage has over the channel charge.
2) V_{pol}: This is the MOSFET gate voltage V_{MOS} at which the gate charge equals the saturation polarization P_s.
3) V_{TH}: This is the threshold voltage of the underlying MOSFET used in the physics model.

Given that the MF has two possible states after a write, the overall qualitative logical function of the SOTFET can also be defined in terms of two threshold voltages: $V_{\text{TH,LOW}}$ the threshold voltage for $m_z = +1$ and $V_{\text{TH,HI}}$, the threshold voltage for $m_z = -1$. $V_{\text{TH,LOW}}$ is primarily a function of V_{POL} and V_{TH}; decreasing with increasing V_{POL} and decreasing with decreasing V_{TH}. $V_{\text{TH,HI}}$ is a function of all three of C_{ferro}, V_{pol} and V_{TH} and decreases with increasing C_{ferro}.

TABLE 1. Qualitative SOTFET behaviors.

	$V_{TH,LOW} > 0$	$V_{TH,LOW} < 0$
$V_{TH,HI} < V_{DD}$	FET Gate voltage dominates MF	SOTFET-OR Conducts if either V_G or MF turn on
$V_{TH,HI} > V_{DD}$	SOTFET-AND Conducts only if both V_G and MF turn on	SOTFET-MEM MF dominates gate voltage

Table 1 shows four possible qualitatively different digital behaviors based on the values of $V_{\text{TH,LOW}}$ and $V_{\text{TH,HI}}$ relative to 0 and V_{DD}, respectively. These values are determined during fabrication to implement the desired functions. We identify the four behaviors as follows.

A. SOTFET-MEM

In this mode, V_{pol} is so high that the device turns on when state $=$ 1 and changing V_{G} has negligible effect on the device current such that the device behaves as a pure memory device. Such a device can be used as a drop-in replacement for traditional MTJ-based circuits with the advantage of a very high on–off ratio.

B. SOTFET-AND

When C_{ferro} and V_{pol} are so low that inverting the channel requires both state $=$ 1 and $V_{\text{G}} = V_{\text{DD}}$, the device behaves like an AND logic device. Fig. 5 shows the simulated device current as a function of the gate voltage for both state $=$ 0 and state $=$ 1 with $C_{\text{ferro}} = 0.5C_{\text{ox}}, V_{\text{pol}} = 0.13$ V, V_{TH} is the nominal PDK threshold voltage (about 0.5V) and C_{ox} is the nominal oxide capacitance of the characterized PDK FET. The stored state serves as one input and the applied gate voltage V_{G} serves as the second input. Such a single device AND-mode logic gate has been simulated and measured for FeFETs in [23]. Table 2 shows the truth table for the four logical combinations of state and V_{G}.

C. SOTFET-OR

When C_{ferro} is high enough that the gate voltage can independently invert the channel regardless of the device state, and

TABLE 2. SOTFET truth table.

m_z	State	V_G	I_D			
			MEMORY	AND	OR	FET
−1	0	0	0	0	0	0
−1	0	1	0	I_{leak}	I_{large}	I_{large}
+1	1	0	I_{large}	I_{leak}	I_{medium}	0
+1	1	1	I_{large}	I_{large}	I_{large}	I_{large}

V_{pol} is also high enough that the channel is almost at the edge of inversion even when $V_{\text{G}} = 0$, the device behaves like an OR logic device. Fig. 5 shows the simulated device current as a function of the gate voltage for both state $=$ 0 and state $=$ 1 with $C_{\text{ferro}} = 2C_{\text{ox}}$, $V_{\text{pol}} = 0.34$ V and V_{TH} is also about 0.5 V. Breyer *et al.* [23] also demonstrates such a single gate FeFET based OR gate.

D. FET

In this mode, both V_{pol} and C_{ferro} are so low that the state of the FM has very negligible effect on the channel charge. The device behaves like a regular FET with both $V_{\text{TH,LOW}} \approx V_{\text{TH,HI}} \approx V_{\text{TH}}$. This mode is not useful for any novel application not already achievable with a regular FET.

V. SOTFET CIRCUITS

The logic-in-memory functionality of the SOTFET can be exploited to build compact memories. In this section, we propose some circuit topologies for RAM, CAM, and TCAM. These memory designs have the advantage of being nonvolatile and area efficient e.g., 16-transistor (16T) conventional CMOS TCAM design versus the 2-SOTFET + 3-Transistor (2SF-3T) SOTFET-based designs. They are also energy efficient from the smaller memory array and nonvolatility.

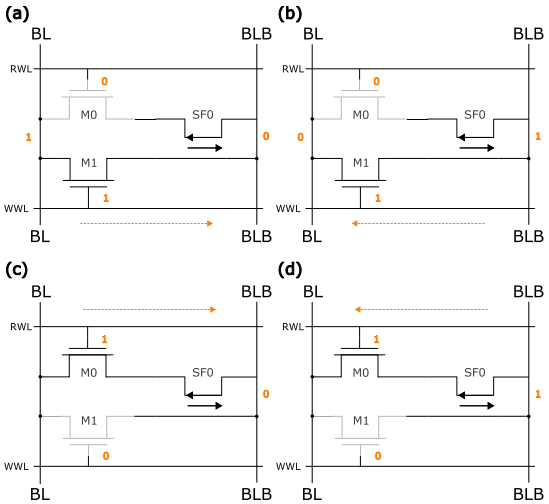

FIGURE 6. Schema of the 1SF-2T MRAM showing read and write operations to (a) write 1: enable WWL, set BL = 1, BLB = 0. Current flows left to right and (b) write 0: enable WWL, set BL = 0, BLB = 1. Current flows right to left. (c) SOTFET-OR MRAM read: enable RWL, precharge BL for readout, set BLB = GND. (d) SOTFET-AND MRAM read, set BLB = V_{DD}, sense current on BL.

A. SF-MRAM

Fig. 6 shows a 1SF-2T SF-MRAM. It consists of one SOTFET device and two MOSFETs. To write to the SF-MRAM, the write word-line (WWL) is set to V_{DD}, the bitline BL is set to the write DATA and BLB is set to $\overline{DATA}$ (the complement of DATA) such that the direction of current flow determines the written state of SF0.

Reading the MRAM is simpler and faster than reading traditional MTJ MRAMs since we no longer use a resistive readout. For reading the data, the read word-line (RWL) is set to V_{DD}. All three of SOTFET-MEM, AND and OR mode devices can be used in SF-MRAMs with appropriate V_G setting. For example, for the SOTFET-AND, the BLB is set to V_{DD} while for the SOTFET-OR, the BLB is set to ground. With the appropriate V_G set, no current flows for state = 0, whereas for state = 1, current flows through SF0 and the transistor M0.

B. SERIES-CAM (SCAM)

Fig. 7 shows the schematic of the SCAM. The SCAM uses two SOTFET-OR cells and one write transistor. For writing to the SCAM, the WWL signal is set to V_{DD}, BL is set to DATA and BLB is set to $\overline{DATA}$. For search operations, the matchline ML is initially precharged to V_{DD} and then BL is set to DATA and BLB to $\overline{DATA}$. Fig. 7(b) and (c) indicate that the matchline only discharges when there is a mismatch; whereas read operations are not directly supported for this topology, the CAM can also be used alongside the SF-MRAM in full-associative nonvolatile cache architectures.

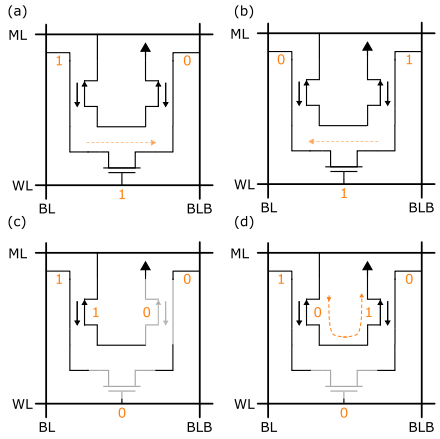

FIGURE 7. Schematic of the 2SF-1T SCAM using SOTFET-OR showing write and search operations. (a) Write 1 by enabling WL and pulling BL high and BLB low. Current flows from left to right. (b) Write 0 by enabling WL and pulling BL low and BLB high. Current flows from right to left. (c) Search 1 when state = 1 by disabling WL (WL = 0), precharging ML, and setting BL = 1, BLB = 0. ML stays high because no current flow. (d) Alternatively, searching 1 when state = 0 causes discharge of ML because of current flow through the SOTFETS.

C. PARALLEL CAM (PCAM)

Fig. 8 shows the schema of the PCAM. The PCAM uses two SOTFET-AND cells and one write transistor. Writing to the PCAM is identical to writing in the SCAM topology. However, since the matchline discharges when a match is detected as shown, the gate polarity is switched during writes such that the two transistors are written to the opposite states

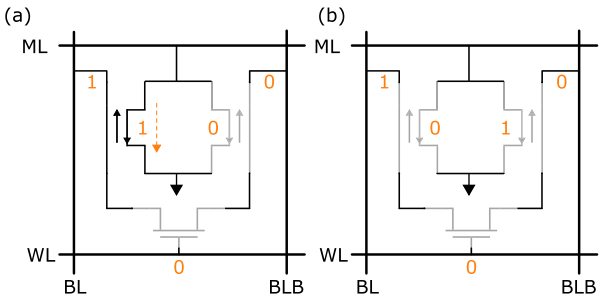

FIGURE 8. Schematic of a PCAM using SOTFET-AND showing search operations with WL set to 0. (a) Search 1 by setting BL = 1, BLB = 0 when state = 1 results in current flow and discharge of precharged ML. (b) Search 1 (BLB = 1, BL = 0) when state = 0 results in no current flow and no discharge of ML.

when compared to the transistor states of the SCAM for the same inputs. The polarity can also be switched during searches such that $\overline{DATA}$ is on BL and DATA is on BLB.

D. TCAM (SERIES AND PARALLEL)

Fig. 9 shows the schemas of both series and parallel TCAMs. The TCAMs work identically to their corresponding SCAM and PCAM counterparts during search operations. Two more transistors enable writing independent data to the SOTFETs. Writing 0 and 1 data require the same operations as in the CAMs. To write ternary data to the series TCAM, CLR is set to V_{DD} and both BL and BLB are set to V_{DD} to effectively write 1's to both SOTFET cells. Likewise, to write ternary data to the parallel TCAM, both BL and BLB are set to V_{DD} (for the configuration which does not switch the gate polarity) to effectively write 1's to both SOTFET cells.

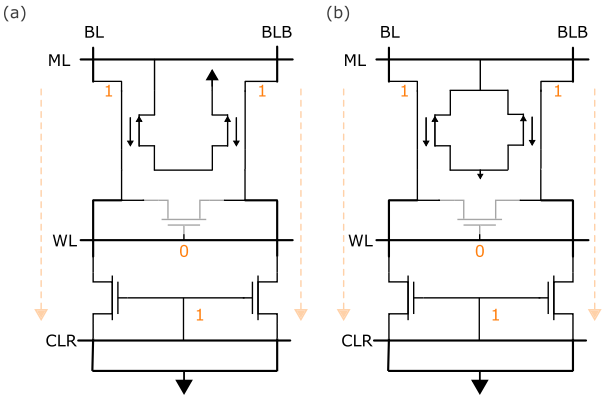

FIGURE 9. TCAM cell can be realized with addition of "don't care" state. This requires adding ability to program both SOTFET magnetization states to "1." Schematic of TCAM showing (a) write operation for "1-1" state on Series TCAM using SOTFET-OR and (b) write operation for "1-1" state on parallel TCAM using SOTFET-AND.

VI. DISCUSSION

The proposed device has the advantage of providing a nonvolatile, low-power, logic-in-memory device with input–output isolation. Simulation results of the proposed circuits using the described model show promise in achieving a truly multifunctional device that incorporates both memory and logic functions.

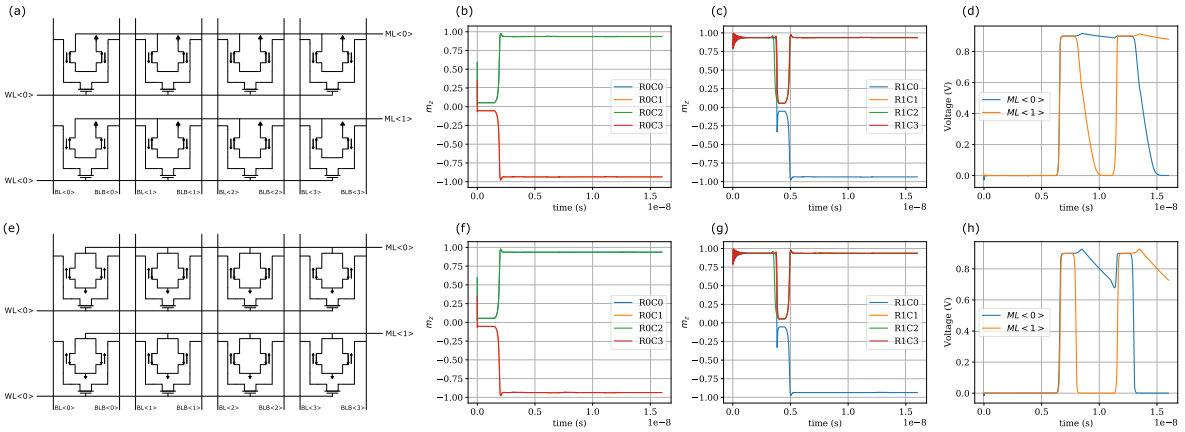

FIGURE 10. Schema and simulation of SCAM and PCAM arrays. Magnetization state is shown for the left SOTFET of each cell. Simulations show writing data = "0101" at $t = 0$ to row 0, writing data = "1110" at $t = 3$ ns to row 1, then searching data = "0101" at $t = 7.5$ ns and searching data = "1110" at $t = 12.5$ ns. (a) SCAM array schematic. (b) Magnetization state for SCAM row 0. (c) Magnetization state for SCAM row 1. (d) SCAM matchline for rows 0 and 1. (e) PCAM array schematic. (f) Magnetization state for PCAM row 0. (g) Magnetization state for PCAM row 1. (h) PCAM matchline for rows 0 and 1.

A. SIMULATION RESULTS

Fig. 10 shows the full operation of associative memories based on both the OR and AND flavors of SOTFETS. As noted earlier, there are significant potential advantages to these SOTFET-based CAM arrays. They are composed of three devices, in comparison to an SRAM-based CAM, which requires ten CMOS devices. This is a potential area savings of up to 3.3X, as suggested by Fig. 11. Additionally, the SOTFET state is nonvolatile, and can be powered down without loss of data, reducing the power dissipation from leakage.

Fig. 10(a)–(d) shows write and search operations for the SCAM, at $t = 0$, WL$\langle 0 \rangle$ is asserted and the write data is set to "0101" to program the first row; at $t = 3$ ns, the WL$\langle 1 \rangle$ is asserted and the write data is set to "1110" to program the second row. Fig. 10(b) and (c) show the states of the left SOTFET for each column in rows 0 and 1, respectively, showing that the desired data is written to the CAM cells. At $t = 7.5$ ns, a search operation for the "0101" sequence is conducted with Fig. 10(d) showing a match for the ML$\langle 0 \rangle$ matchline only. At $t = 12.5$ ns, a search operation for "1110" is conducted with Fig. 10(d) also showing a match for the ML$\langle 1 \rangle$ matchline only.

The same operations are run for the PCAM array with Fig. 10(e)–(g) showing the simulation results. While search operations are faster than for the SCAM case, the line will slowly discharge in the mismatch state due to the nonzero off current of the AND device. Note that both PCAM and SCAM simulations use the nominal V_{TH} of the PDK. Decreasing V_{TH} should reduce search time for SCAM, and increasing the V_{TH} should reduce the discharge rate for the PCAM.

We have also run simulations demonstrating the functionality of the MRAM topology shown in Fig. 6 using both SOTFET-OR and SOTFET-s. Activating WWL switches the state depending on the values of BL and BLB and activating RWL after precharging discharges one of BL or BLB depending on the previously written state.

B. COMPARISON TO CMOS ALTERNATIVES

The current state of the art in associative memories and on-chip memory, in general, are CMOS-based circuits. The most

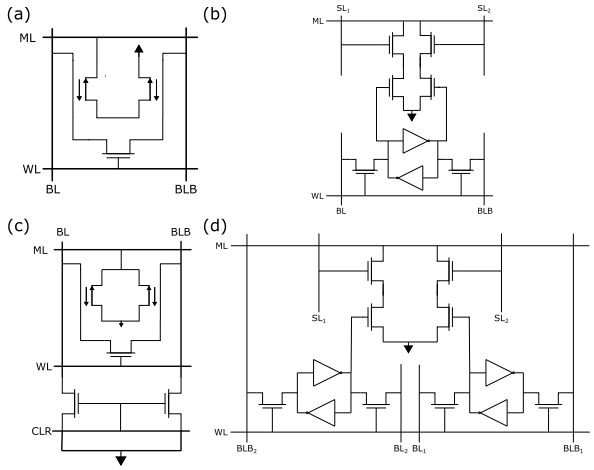

FIGURE 11. CMOS and SOTFET-based CAM and TCAM circuit schematics showing area and complexity advantages of SOTFET-based circuits. (a) 2SF-1T CAM. (b) 10T CMOS CAM. (c) 2SF-3T TCAM. (d) 16T CMOS TCAM.

obvious potential advantages of the presented SOTFET-based alternatives are in the more compact size and the reduced static power from leakage enabled by nonvolatility. In fact, CMOS-based CAMs are not widely used due to the relatively large cell size. Fig. 11 compares both SOTFET and CMOS-based CAM and TCAM circuits with the CMOS alternatives requiring up to 3X transistors and area. These expected area savings should also translate to potential energy savings from driving smaller bit-lines and word-lines. Furthermore, the static power consumption due to leakage has been estimated to contribute to more than 60% of the total power consumption in modern CMOS SRAM arrays [24], [25]. We, therefore, expect significant energy savings courtesy of the SOTFET's nonvolatility.

Like other emerging technologies, such as the FeFET, RRAM, and MTJs, we expect the SOTFET to provide additional benefits over CMOS alternatives in building reconfigurable circuits, such as lookup tables (LUTs), field-programmable gate arrays (FPGA), and hardware neural network accelerators. Some of these application areas

aim to bridge density-speed gaps in memory hierarchies and are currently being explored using other emerging devices as in [26]–[28]. We expect similar and sometimes better performance from the SOTFET with potential advantages, such as those outlined in the comparison to the FeFET in Section VI-C.

Our simulations demonstrate the high-level functionality of the SOTFET-based CAM commensurate with the much larger CMOS-based cell. Detailed comparisons and benchmarking in the application are a subject of future work.

C. COMPARISON TO FeFET

Among emerging post-CMOS devices, the SOTFET is most similar to the FeFET in offering the possibility of single device logic-in-memory [11]. A similar 2-FeFET-based CAM design has been published in [29]. For a single device, we expect similar search/read energy and delay as the FeFET and similar write energy and delay as SOT-MTJ-based devices. While write delay and energy for SOT-based switching are dependent on the spin Hall efficiency, we estimate the write delay to be about 1 ns and the write energy to be about 12 fJ based on the parameters in the table in the Supplementary Material. The write delay and energy are about 1 ns and 1 fJ, respectively, for the FeFET [30]. We also expect a slightly larger area due to the presence of the additional gate contact for each SOTFET.

However, the FeFET does not offer enough input–output isolation since both reads and writes are done through voltages on the device gate. The SOTFET, on the other hand, writes through currents and reads through voltages, offering the possibility of independently optimizing the read and write paths to minimize crosstalk.

Another well-known issue with the FeFET is the cycling endurance [31]. We propose that this may be less of an issue in the SOTFET because the electronic polarization switching mechanism is fundamentally different in these two types of devices. In FeFET, the external electric field from V_G that overcomes the coercive field and leads to the displacive motion of atoms is often very large ($>$0.1 MV/cm) and has long been speculated to be the leading cause of charge injection and long-distance atom motion, and therefore fatigue in ferroelectrics. In the SOTFET, the electric-polarization switching is driven by coupling to the magnetic layer rather than by a large external electric field, which should reduce the tendency for charge injection or long-distance atom motion. Furthermore, when the layers are not being switched, this same coupling has the potential to help stabilize the electric polarization to maximize nonvolatility. The demonstration of these effects is actively being pursued by the experimental team at Cornell.

D. POTENTIAL PITFALLS

Interesting potential pitfalls and focus points for device innovation have arisen from our simulations that are worth discussing. The primary considerations in the co-design of device and circuits for associative memories are: the energy and time required for writes and reads, the accuracy of reads and writes, the ability to hold state, and the array density or area of the cells.

First, the model confirms that the critical current and energy needed for writes is determined by the spin Hall angle (modeled by θ_{AD} and θ_{FL}) and resistivity (modeled by R_G) of the TI through current shunting through the FM layer as in SOT-MTJ devices. Further materials research, such as the recent results in [32], which demonstrated a TI with both large spin Hall angle and high conductivity, is needed to further reduce the critical currents and write energy.

Furthermore, the device parameters of C_{ferro} and V_{pol}, which indicate how much control the gate voltage has on the channel, are critical in determining the logic function of the device. We have shown that for the OR logic device, the device current for the state $= 1$, $V_G = 0$ logic combination determines the output current, and hence, sensing speed for the MRAM, CAM, and TCAM. This indicates that a SOTFET designed for OR mode operation will need to maximize the output current for this combination. On the other hand, in devices designed for AND mode operation, the output current for the state $= 1$, $V_G = 0$ logic combination will need to be minimized.

Finally, our simulations show the impact of the switching dynamics on the reliability of stored states during search operations. SOTFETs, as described in the CAM structures simplify array circuitry by using their bit lines for both write and search operations. Ideally, searches do not over-write stored states because write and search operations use distinct electrical signals: voltage to search, current to write. However, our simulations indicate that under dynamic conditions, such crosstalk is possible. During a search, when voltages are exerted on the bit lines, they must charge up the gate capacitance of the SOTFETs, and parasitic capacitance of the write-enable transistor. Because this charging must happen through the gate resistance of the SOTFETs, a transient current will appear on the gate. If this transient current is large enough, and on the same timescale as the switching time of the FM, the SOTFET's state may be altered. Therefore, some care must be taken to avoid such unwanted switching.

We are also developing more-detailed physics-based device models that can account for depolarization in MF and thermal effects, since joule heating at high current densities may modify the switching current [33].

Though it is yet to be experimentally demonstrated that it is possible to switch the electronic polarization in a multiferroic material by magnetic exchange coupling at room by magnetic exchange coupling, which is key to a SOTFET, this article represents the first exploration of the potential pros and cons of a SOTFET.

VII. CONCLUSION

This article presented a preliminary circuits model for the proposed SOTFET device. Using this model, we introduced and simulated some RAM and CAM circuit architectures and identified important materials parameters for optimal circuit performance. The developed model can be leveraged for further circuit and architecture level exploration for use in applications, such as processing in memory.

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