SiC Substrate-Integrated Waveguides for High-Power Monolithic Integrated Circuits Above 110 GHz

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Abstract—Substrate-integrated waveguides (SIWs) of different geometry are designed, fabricated, and measured on a SiC wafer, along with SIW-based resonators, SIW-based filters, grounded coplanar waveguides (GCPWs), GCPW-SIW transitions, and calibration structures. Two-tier calibration is used to extract the intrinsic SIW characteristics from GCPW-probed scattering parameters. The resulted D-band (110–170 GHz) SIWs exhibit a record low insertion loss of 0.22 ± 0.04 dB/mm, which is four times better than that of the GCPWs. A 3-pole filter exhibits a 1.0-dB insertion loss and a 25-dB return loss at 135 GHz, which represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. These results show the promise of SIWs for integrating HEMTs, filters, antennas, and other circuit elements on the same SiC chip. 

Keywords—cavity resonators, microwave filters, millimeter wave integrated circuits, semiconductor waveguides

I. INTRODUCTION

Conventional microwave monolithic integrated circuits (MMICs) are based on coplanar or microstrip transmission lines, which suffer from high loss, significant crosstalk, and limited power capacity. However, substrate-integrated waveguides (SIWs) have recently gained attention due to their attractive properties, such as high power capacity, low loss, and high gain. SIWs are attractive because SiC is high in dielectric constant, electrical resistivity, breakdown strength, mechanical toughness, and thermal conductivity, but low in loss tangent and thermal expansion coefficient [3]–[6].

Despite the attractiveness of SIWs, to date there are few reports of SIWs above 110 GHz on Si [7]–[11] or SiC [12], [13]. In this paper, we demonstrate D-band (110–170 GHz) SiC SIWs with an insertion loss of 0.22 ± 0.04 dB/mm. Also fabricated on the same wafer is a 3-pole SIW filter with a 1.0-dB insertion loss and a 25-dB return loss at 135 GHz. These record performances (Table I and Table II) make SIW promising for monolithic integration of high-quality SIW filters, edge-firing SIW antennas [14], and GaN HEMTs [15] (Fig. 1).

II. DESIGN, FABRICATION, AND MEASUREMENT

Guided by analytical equations [16] and numerical simulations (HFSS), D-band SIWs are designed, fabricated and measured on 100-μm-thick 6H-SiC wafers with > 10^6 Ω·cm resistivity. Each SIW has two parallel rows of through-substrate vias (TSVs) that are 40 μm in diameter and 100 μm apart center-to-center [Fig. 2(a)]. The rows are 520 μm apart center-to-center to cut off the fundamental TE_{10} mode below 110 GHz. Additionally, SIW resonators and filters of different geometry are designed (Fig. 3).
To facilitate wafer probing, each SIW is transitioned \[17\], \[18\] to a grounded coplanar waveguide (GCPW) \[19\] at both the input and output. Each transition is 578-μm long, including a 175-μm GCPW section, a 353-μm tapered section, and a 50-μm SIW section [Fig. 2(a)]. In the GCPW section, the center electrode is 30-μm wide with a 16-μm gap from the ground electrodes. In the tapered section, the center electrode is linearly widened to 155 μm while the gap is linearly widened to 158 μm. To extract the intrinsic SIW characteristics, through-reflect-line (TRL) calibration structures \[20\], \[21\] are laid out [Fig. 2(b)] and fabricated on the same SiC wafer as the SIWs. Composite layouts are shown in Fig. 2(b) because they are more informative than chip micrographs as shown in Fig. 2(a).

Fabrication starts with frontside (Si face of SiC) metallization by 100-nm-thick Ni and 700-nm-thick Al, before the SiC wafer is flip-mounted on a sapphire carrier for TSV etching. Similar to \[22\], TSVs are etched in an Oxford PlasmaPro 100-380 COBRA inductively-coupled plasma etcher with 50-sccm SF₆ and 10-sccm O₂ under 10-mTorr pressure and cryogenic cooling. RF powers of 2000 W and 50 W at 2 MHz are applied to the plasma and substrate, respectively. The etch rate of SiC through a 5-μm-thick Ni mask is 15 μm/h with a 50:1 selectivity over Ni. Backside metallization consists of 100-nm-thick Ni and 2-μm-thick Al.

Lacking D-band frequency extenders, the fabricated SIWs are characterized by a Keysight E8361C VNA equipped with VDI F-band frequency extenders for 110‒140 GHz and OML G-band frequency extenders for 140‒170 GHz (Fig. 4). For each band, Formfactor Infinity probes with ground, signal, and ground tips at 50-μm pitch are used. Two-tier calibration is applied sequentially. Tier-1 calibration shifts reference planes from the VNA to the probe tips, using the load-reflect-reflect-match (LRRM) method \[23\] and a Formfactor 138-356 impedance-standard substrate. Tier-2 calibration shifts reference planes past the GCPW-SIW transitions to the intrinsic SIW section, using the TRL method and the calibration structures of Fig. 2(b). Despite stitching errors at 140 GHz, the general trend of the measured data is consistent with the simulated results across the D band.

### III. RESULTS AND DISCUSSION

Fig. 5 shows the measured and simulated magnitudes of the reflection and transmission coefficients, \(S_{11}\) and \(S_{21}\), for an SIW with a length of 620 μm, 860 μm, or 1100 μm. \(S_{11}\) is normalized by the SIW length. \(S_{21}\) is normalized by the SIW length.
hence, not shown.) Agreements are evident between measurement and simulation, and between different lengths. From 110 GHz to 170 GHz, the insertion loss is 0.22 ± 0.04 dB/mm and the return loss is greater than 17 dB. The insertion loss is four times lower than that of GCPWs fabricated on the same SiC wafer. Microstrip transmission lines would have even higher loss than GCPWs above 110 GHz [7]. The SIW loss could be further reduced by better metallization, as simulation indicates the loss is mainly in the conductor rather than the dielectric, in agreement with [8]. Presently, the GCPW section at the expense of higher transition loss. In any case, it is challenging to measure an insertion loss as small as 0.2 dB and SIWs much longer than 1 mm should be used to more precisely characterize their insertion loss.

Fig. 6 shows the measured and simulated magnitude of $S_{11}$ for one-port resonators comprising a GCPW-SIW transition and an SIW cavity 400-μm, 500-μm, or 600-μm long.

IV. CONCLUSION

D-band SiC SIWs, resonators, and filters are designed, fabricated, and measured. The SIWs, with a record low insertion loss of 0.22 ± 0.04 dB/mm, have four times lower loss than GCPWs fabricated on the same SiC wafer. The three-pole filter, with an insertion loss of 1.0 dB, represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. With further improvements, SIWs could be used to efficiently interconnect HEMTs, filters, antennas, and other circuit elements on the same SiC chip for high-power monolithic integrated circuits above 110 GHz.

The adaptation of SiC SIWs could be rapid, taking advantage of available technology. SiC substrates are commonly thinned down to 100 μm in high-power GaN MMICs to facilitate heat dissipation. TSVs similar to those in SIWs are commonly used to reduce the source inductance and are available in commercial GaN foundries [25]. Although TSVs in an SIW are of much higher density, wafer breakage is usually not an issue because SiC is mechanically tough. It can be seen in Fig. 3 that the TSVs are uniform, the yield is high, and the design is robust.

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